



VL-FS-TLM-L120FTH-01 REV. A
(TLM-L120FTH-01)

MAY/2005

PAGE 1 OF 26

DOCUMENT NUMBER AND REVISION




**VL-FS-TLM-L120FTH-01 REV. A
(TLM-L120FTH-01)**

**DOCUMENT TITLE:
SPECIFICATION**

OF

LCD MODULE TYPE

MODEL NO.: TLM-L120FTH-01

DEPARTMENT	NAME	SIGNATURE	DATE
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DISTRIBUTION LIST: MARKETING



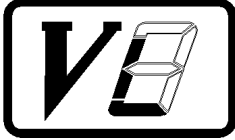
DOCUMENT REVISION HISTORY 1:

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VARITRONIX LIMITED

Specification of LCD Module Type Model No.: TLM-L120FTH-01

1. General Description

Color LTPS TFT 128 x RGB x 160 LCD Panel:

- 128xRGBx160 dots 65 K/262K LTPS (low temperature poly silicon) TFT transfective LTPS dot matrix LCD module.
- Display size (diagonal): 1.2 inch.
- Driving IC: 'TOPPOLY Optoelectronics corp.' TP020A ASIC or equivalent.
- Driving IC: 'TOPPOLY Optoelectronics corp.' TP021A level shift(13ch),DC/DC converter, 2 mode power save or equivalent.
- Logic voltage: 2.7V.
- Viewing angle: 6 o'clock.
- FPC for module and FPC for backlight.
- White LED02 backlight.
- Normally white.
- Low power.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	25.6(W) x 39.5(H) x 7.2(D)	mm
Color TFT 128 x RGB x 160	Active area	19.01(W) x 23.76(H)
	Display format	128 x RGB x 160
	Color configuration	R.G.B. stripe
	Dot pitch	0.1485(W) x 0.1485(H)
Weight	Approx. 5.0	grams

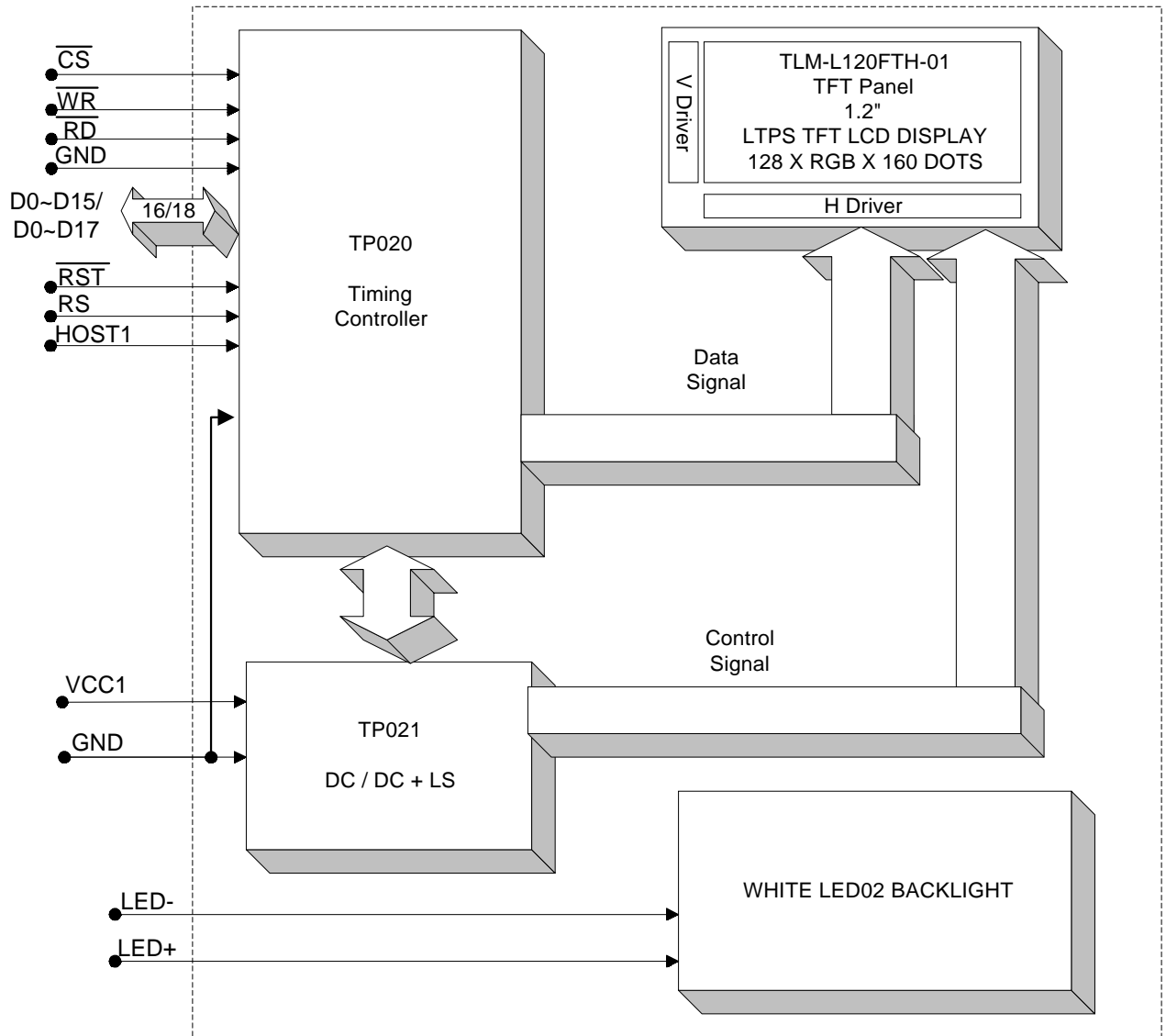
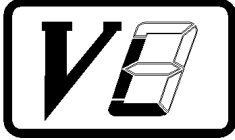


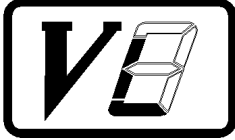
Figure 2: Block Diagram.



3. Interface signals

Table 2: Pin assignment

Pin No.	Symbol	Description
1	VCC1	Power supply 1 for a logic circuit.
2	\overline{CS}	Chip select input pin. Data input/output is enables only when \overline{CS} ($\overline{CS1}$) is low and CS2 is high. When chip select is non-active, D17 to D0 will be high impedance.
3	\overline{WR}	When interfacing to a 6800-series MPU, read/write is enabled at; \overline{WR} = "H": read. \overline{WR} = "L": write. When interfacing to an 8080-series MPU, \overline{WR} is enabled at low. The signals on the data bus are latched at the rising edge of the \overline{WR} signal.
4	\overline{RD}	When interfacing to a 6800-series MPU: Active High. This pin is used as an enable clock input pin of the 6800-series MPU. When interfacing to a 8080-series MPU: Active Low. This pin is connected to the \overline{RD} signal of the 8080-series MPU. While this signal is Low, data bus output is enabled.
5	GND	Ground for the logic side. GND = 0V.
6	D0	18-bit bi-directional data bus. When chip select is not active, D17 to D0 will be high impedance.
7	D1	
8	D2	
9	D3	
10	D4	
11	D5	
12	D6	
13	D7	
14	D8	
15	D9	
16	D10	
17	D11	
18	D12	
19	D13	
20	D14	
21	D15	
22	D16	
23	D17	
24	\overline{RST}	Hardware reset input pin. When \overline{RST} is "L", initialization is executed.
25	RS	Register select input pin. RS="High": Indicates that D17 to D0 are display data. RS="Low": Indicates that D17 to D0 are control data.
26	LED-	LED cathode.
27	HOST1	Select CPU interface (0:180, 1:M68).
28	LED+	LED power supply.
29	NC	Not connected.
30	NC	Not connected.



4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings – For IC Only

Table 3:Electrical Maximum Ratings for TP021A

Parameter	Symbol	Min.	Max.	Unit
Supply voltage (VCC1)	VCC1-GND	-0.3	+4.0	V
Supply voltage (GND)	GND	-0.3	+0.3	V
Supply voltage (VOUT2)	VOUT2	-0.3	+11.5	V
Input voltage	Vin	-0.3	VCC1+0.3	V

- Note: 1.) The modules may be destroyed if they are used beyond the absolute maximum ratings.
2.) All voltage values are referenced to GND = 0V.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+40°C	-10°C	+60°C	Dry, 240 hours
Humidity	90% max. RH for Ta=25°C				No condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration: 11 ms Peak acceleration: $981 \text{ m/s}^2 = 100\text{g}$ Number of shocks: 3 shocks in 3 mutually perpendicular axes.				3 directions



5. Electrical Specifications

5.1 Typical Electrical Characteristics

At $T_a = 25\text{ }^\circ\text{C}$, $V_{CC1} = 2.7\text{V}$, $GND = 0\text{V}$.

Table 5: Typical Electrical Characteristics for TP021A

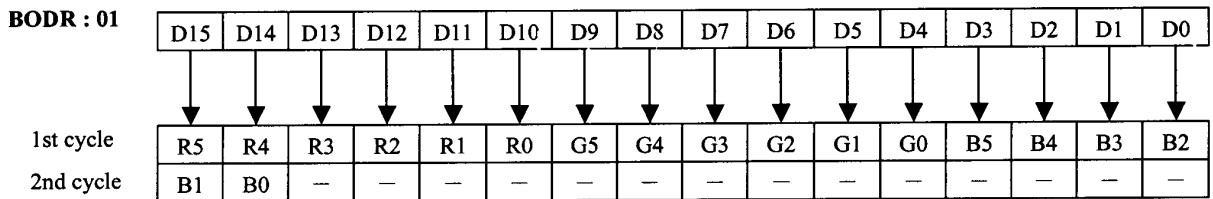
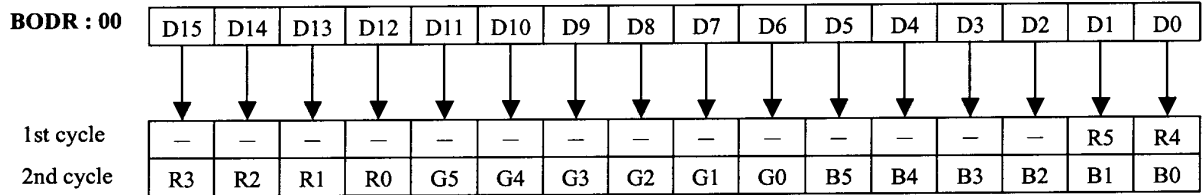
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (logic)	VCC1-GND		-	2.7	3.0	V
Input signal voltage	Vin_H	“H” level	2.7	2.8	3.0	V
	Vin_L	“L” level	0	-	0.25	V
Supply current (Logic & LCD)	ICC1	$V_{CC1} = 2.7\text{V}$	-	3.95	-	mA
Supply voltage of white LED02 backlight	VLED	Forward current =15 mA Number of LED dies=1	3.1	3.3	3.5	V
Brightness of backlight (on the backlight surface)			1,600	2,000	-	cd/m ²
Uniformity	100x (Minimum/ Maximum)		80	-	-	%

Note (1): There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

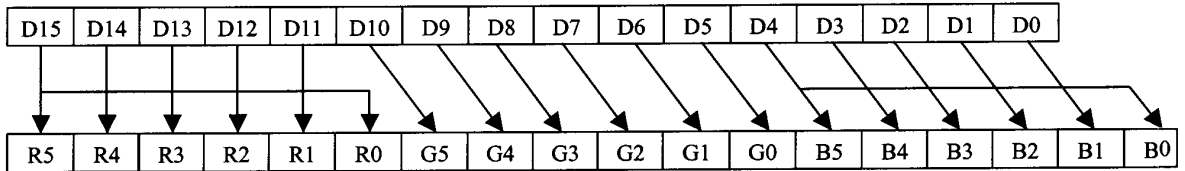


5.2 CPU Interface 16 bit mode for TP020

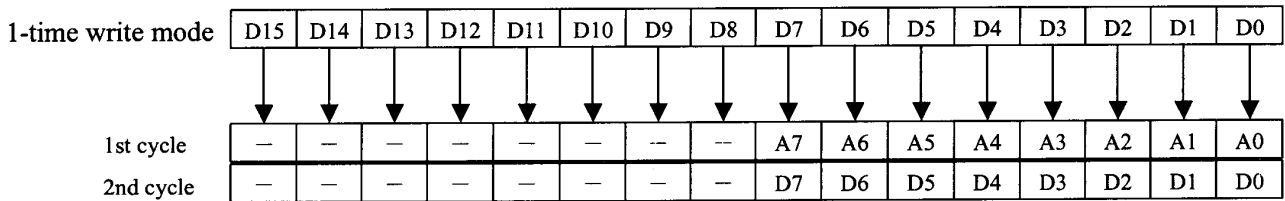
1. Signal data



BODR : 1x



2. Command data

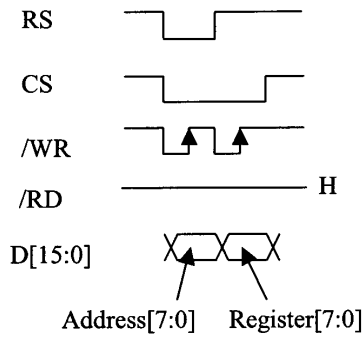




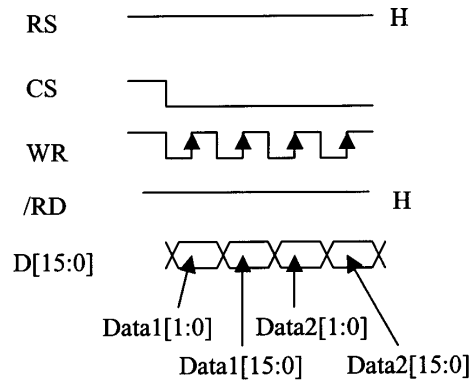
3. Input timing waveform

BODR:00
i80 System

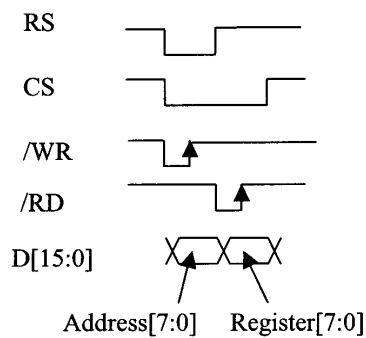
1)command (Write mode)



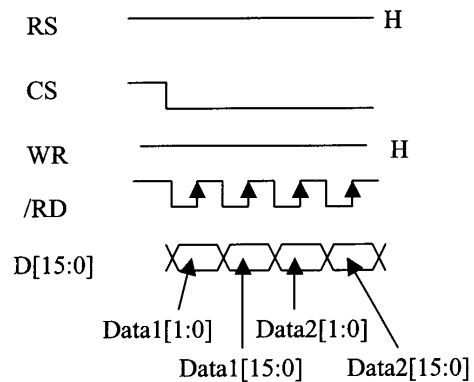
2)data (Write mode)



3)command (Read mode)

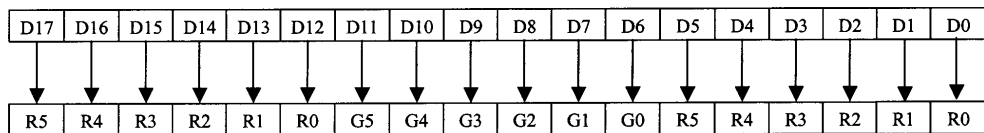


4)data (Read mode)



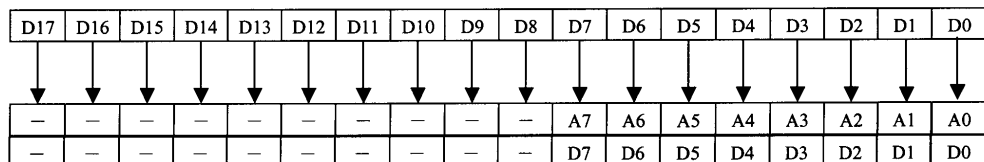
CPU Interface 18 bit mode for TP020

1. Signal data



2. Command data

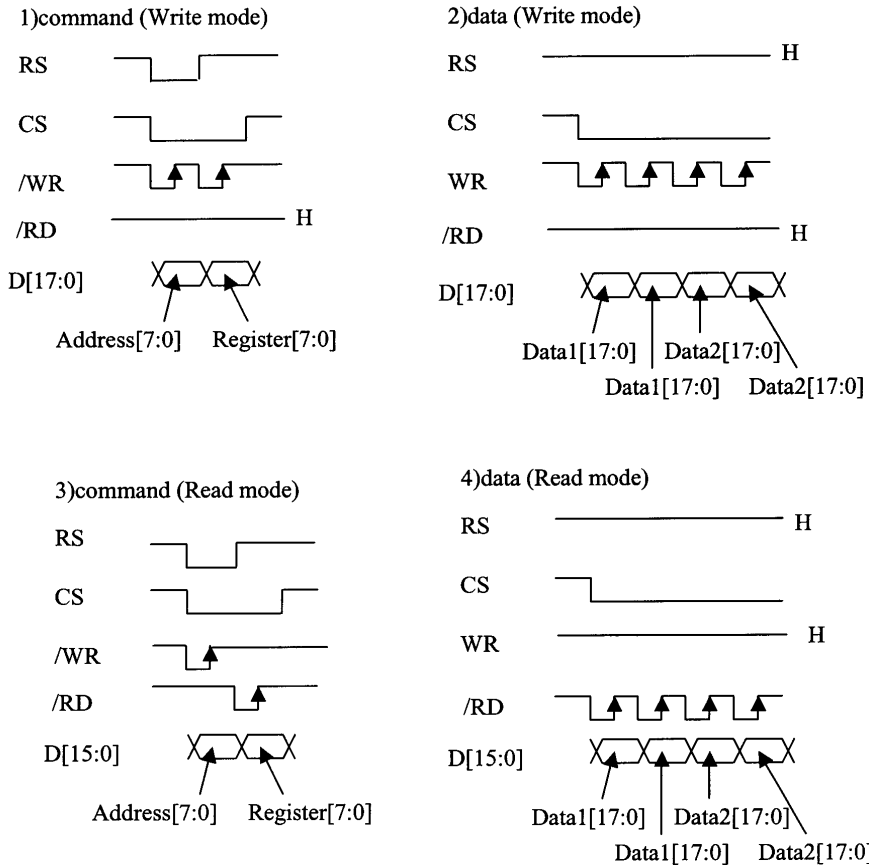
1-time write mode





3. Input timing waveform

i80 System



Input Timing Characteristics for TP020

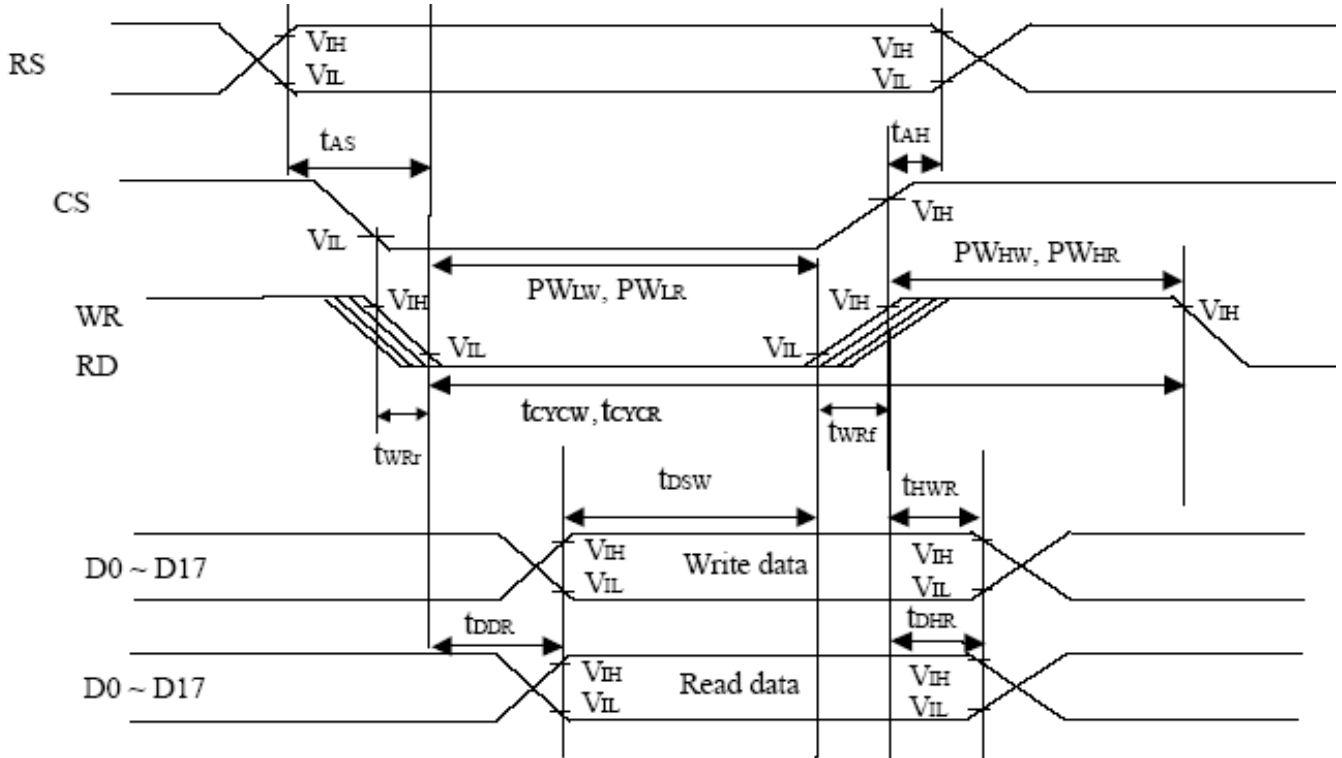
128 x 160

	R0	G0	B0	R1	G1	B1	.	R126	G126	B126	R127	G127	B127	
	D17		.D0		D17		.D0		D17		.D0		D17	
L1	"0000"H		"0001"H		"0001"H		.		"007E"H		"007F"H			
L2	"0100"H		"0101"H		"0101"H		.		"017E"H		"017F"H			
L3	"0200"H		"0201"H		"0201"H		.		"027E"H		"027F"H			
L4	"0300"H		"0301"H		"0301"H		.		"037E"H		"037F"H			
L5	"0400"H		"0401"H		"0401"H		.		"047E"H		"047F"H			
													
L155	"9A00"H		"9A01"H		"9A01"H		.		"9A7E"H		"9A7F"H			
L156	"9B00"H		"9B01"H		"9B01"H		.		"9B7E"H		"9B7F"H			
L157	"9C00"H		"9C01"H		"9C01"H		.		"9C7E"H		"9C7F"H			
L158	"9D00"H		"9D01"H		"9D01"H		.		"9D7E"H		"9D7F"H			
L159	"9E00"H		"9E01"H		"9E01"H		.		"9E7E"H		"9E7F"H			
L160	"9F00"H		"9F01"H		"9F01"H		.		"9F7E"H		"9F7F"H			



5.3 CPU Interface input timing

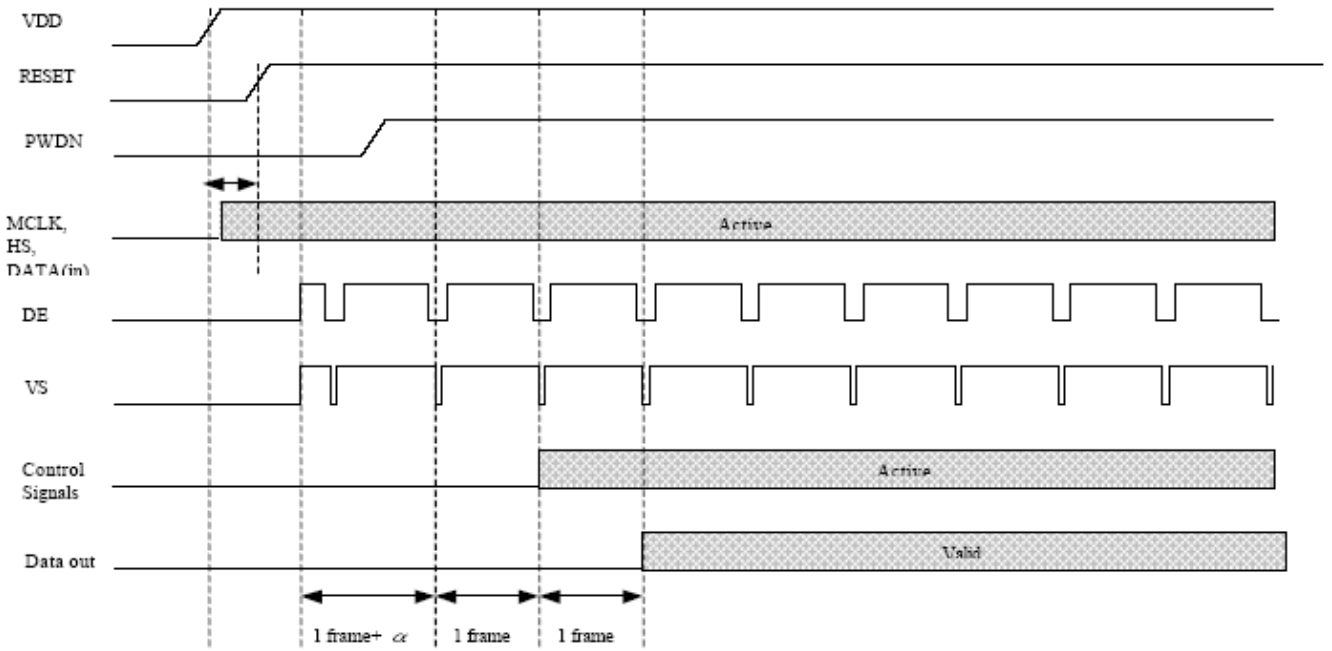
5.3.1 i80 System CPU Interface



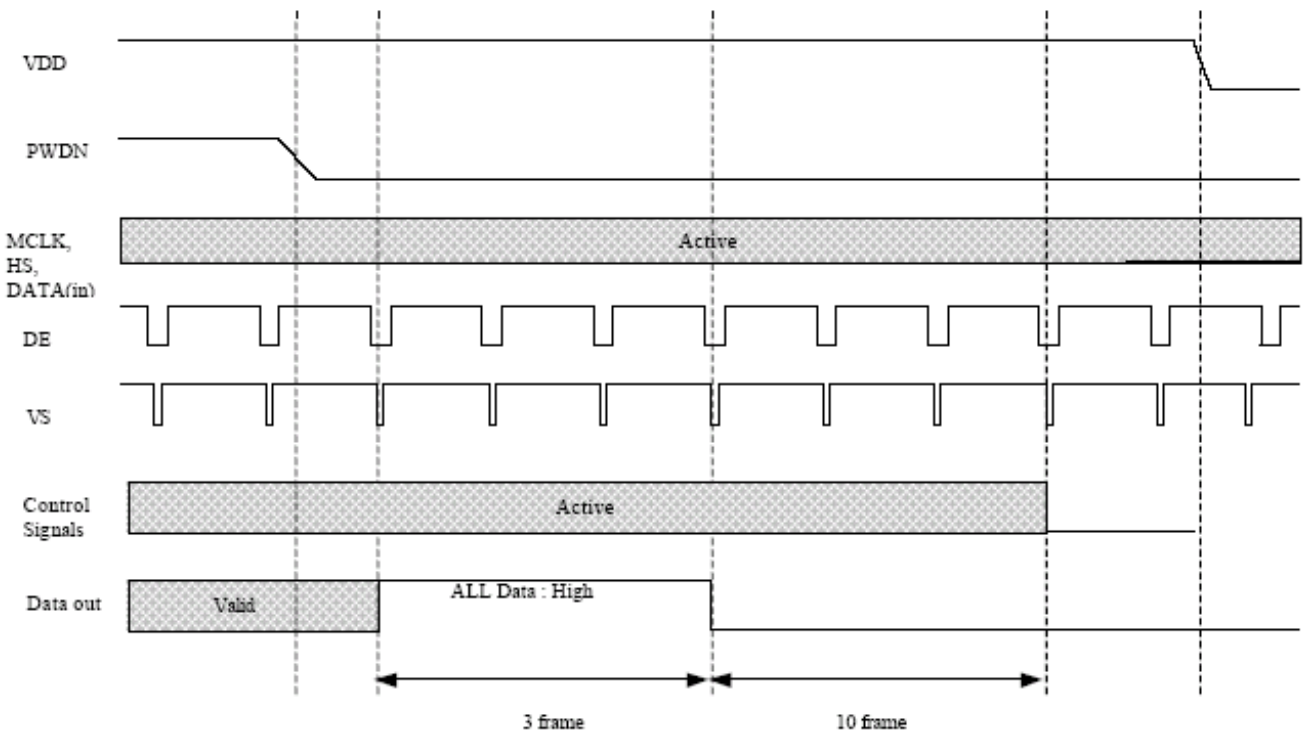
Item	Symbol	Min	Typ	Max	unit
E_RD cycle time	t _{cyw}	200	—	—	ns
	t _{cycr}	300	—	—	ns
E_RD pulse width low	P _{WLW}	40	—	—	ns
	P _{WLR}	150	—	—	ns
E_RD pulse width high	P _{WHW}	100	—	—	ns
	P _{WHR}	100	—	—	ns
Pulse rise/fall time	t _{wrf} , t _{wrf}	—	—	25	ns
Chip select setup time	t _{AS}	10	—	—	ns
Chip select hold time	t _{AH}	2	—	—	ns
Data setup time	t _{ds}	60	—	—	ns
Data hold time	t _{hwr}	2	—	—	ns
Data output setup time	t _{ddr}	—	—	100	ns
Data output hold time	t _{dhr}	5	—	—	ns

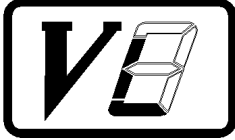


5.3.2 Power On Sequence



5.3.3 Power Off Sequence





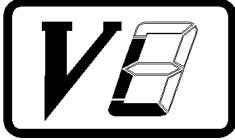
6. Optical Characteristics

6.1 Panel Optical Specification

6.1.1 Transmissive Mode

Ta=25°C

Item	Symbol	Condition	MIN	TYP	MAX	Unit	Remarks	
Viewing angles	$\theta 11$	CR = 2	40	45	--	Degree	Note 6-1	
	$\theta 12$		40	45	--			
	$\theta 21$		40	45	--			
	$\theta 22$		50	60	--			
Contrast ratio	CR	$\theta = 0^\circ$	40	50	--		Note 6-2	
Luminance	L		30	37	--	cd/m ²	Note 6-3	
Transmittance ratio	T		TBD	TBD	--	%		
Chromaticity	White	X	$\theta = 0^\circ$	0.22	0.32	0.42		Note 6-4
		y		0.23	0.33	0.43		
	Red	X		0.4	0.5	0.6		
		y		0.22	0.32	0.42		
	Green	X		0.25	0.35	0.45		
		y		0.39	0.49	0.59		
	Blue	X		0.07	0.17	0.27		
		y		0.07	0.17	0.27		
Response Time	Rising Tr	Tr+Tf	25°C	--	20	40	msec	
	Falling Tf							



6.1.2 Reflective Mode

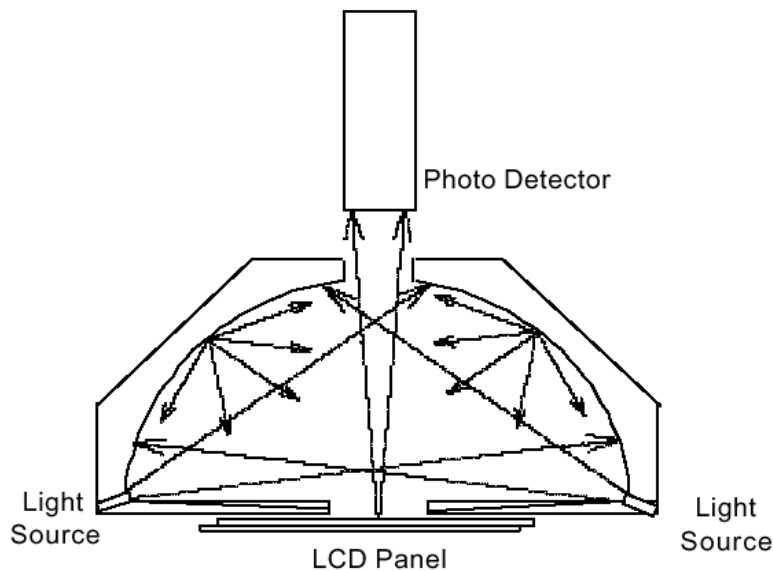
Ta=25°C

Item	Symbol	Condition	MIN	TYP	MAX	Unit	Remarks	
Viewing angles	$\theta 11$	CR = 2	40	45	--	Degree	Note 6-1	
	$\theta 12$		40	45	--			
	$\theta 21$		40	45	--			
	$\theta 22$		50	60	--			
Contrast ratio	CR	$\theta = 10^\circ$	10	15	--		Note 6-5	
Chromaticity	White	$\theta = 0^\circ$	x_{WON}	0.28	0.33	0.38		Note 6-6
			y_{WON}	0.31	0.36	0.41		
Reflection ratio	R	$\theta = 10^\circ$	15	20	--	%	Note 6-7	

6.2 Basic Measure Condition

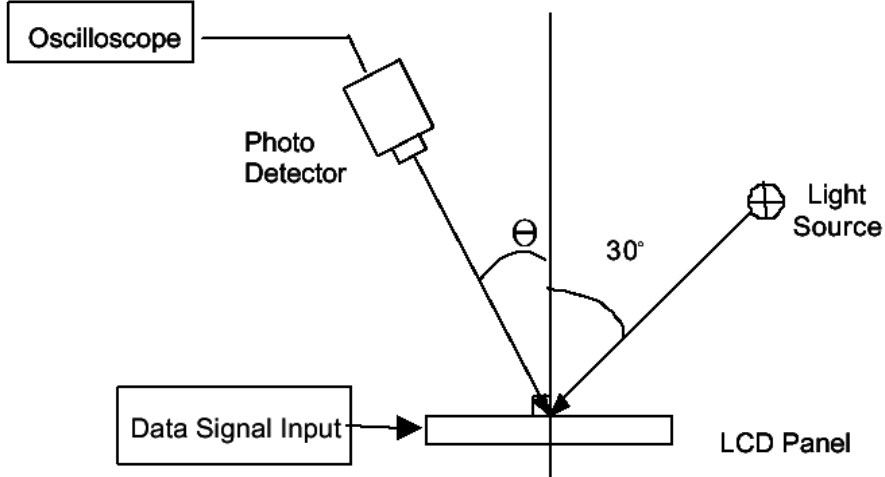
- (1) Ambient Temperature: Ta=25°C
- (2) Testing Point: Measure in the display center point and the test angle $\theta = 0^\circ$
- (3) Measuring System

a. Measure System A

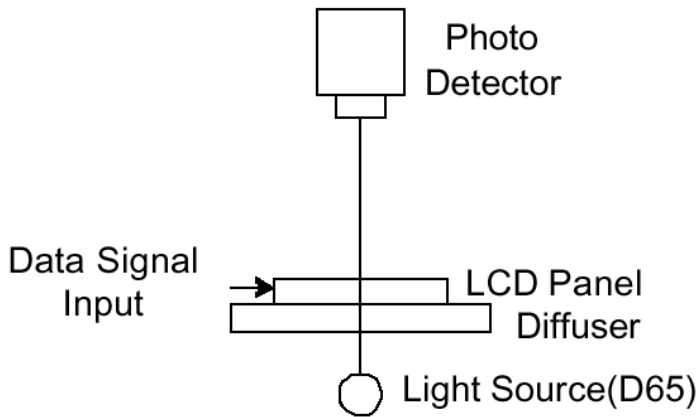




b. Measure System B

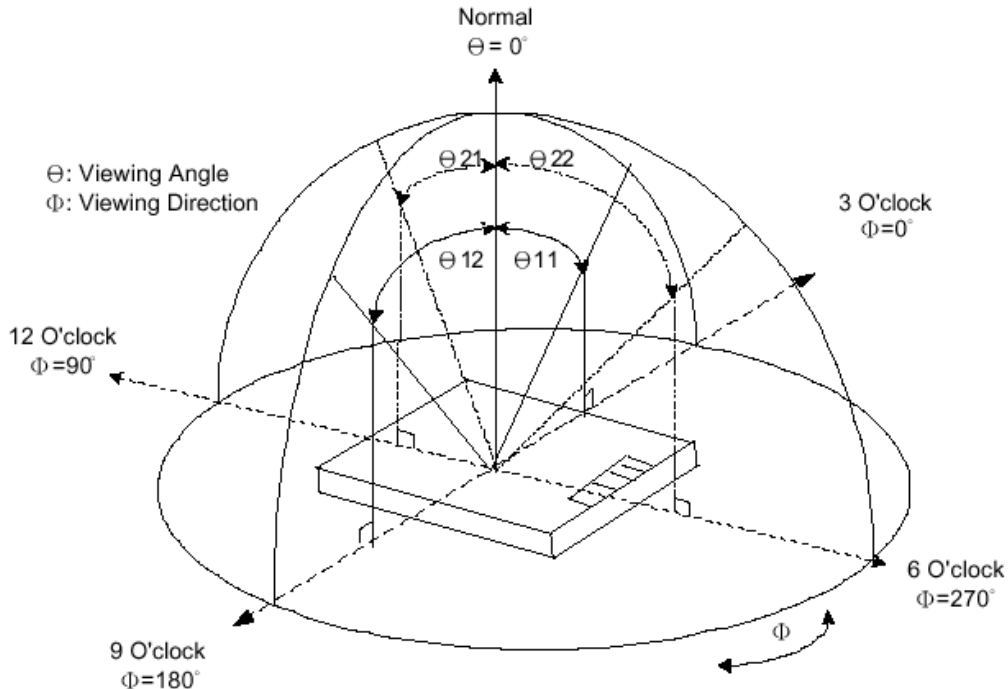


c. Measure System C





Note 6-1: Viewing angle diagram:



Note 6-2: Contrast Ratio as Backlight On: (Measure System C)

Contrast ratio is measured in optimum common electrode voltage. The signal amplitude

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

Note 6-3: Luminance: (Measure System C)

Test Point: Display Center

Note 6-4: Chromaticity: The same test condition as Note 7-3.

Note: 6-5: Contrast Ratio: (Measure System B)

Contrast ratio is measured in optimum common electrode voltage. The signal amplitude

$$CR = \frac{\text{Luminance with white image}}{\text{Luminance with black image}}$$

Note 6-6: Reflectance: (Measure System B)

$$\text{Reflection ratio}(R) = \frac{\text{Light detected level of refrection by the LCD module}}{\text{Light detected level of refrection by the standard white}}$$

Note 6-7: Chromaticity: (Measure System A)






7. Specification And Inspection Items

7. Specification And Inspection Items

7.1. Shipping Cosmetic Specification

7.1.1 Display Inspection (Operating)

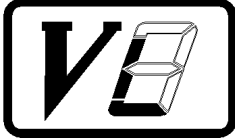
Item	Criteria for defect	Inspection pattern
Display function	No display malfunction	All pattern
Line defect	No obvious vertical and horizontal line defect in white or black (Note 1)	 
Mura	Visible through 5% ND filter (Note 2)	

7.1.2 Dot Defects







7.1.2.1 Inspection Conditions

- Viewing distance: 35 cm
- Ambient illumination: standard 500 Lux
- Light source condition: based on the specification
- View angle (CR > 2): U/D: 100°, L/R: 90°

Sit in front of screen and look up, down, left and right then adjust the screen till it is not visible from 4 directions. The angle range is flexible to locate the monitor.



7.1.2.2 Dot Defect Specification

Inspection standards		Inspection pattern		
Item	Number	Bright dot defect (Note 3) Dark dot defect (Note 4) Joined dots defect (Note 5) Small Bright dot defect (Note 6)		
Bright	TBD			
Dark	TBD			
Total	TBD			

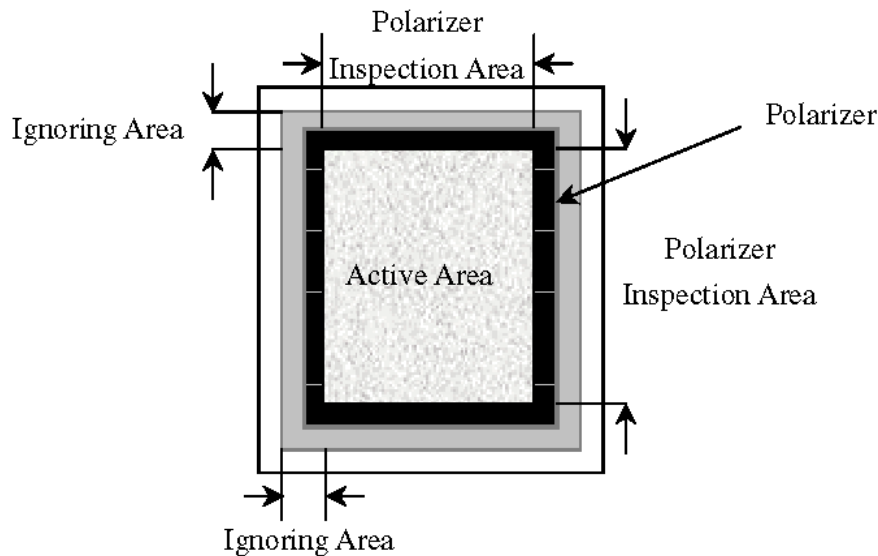
- (a) The distance between black dot defects or bright dot defects should be larger than 4 mm apart.
- (b) Definitions of joined bright dot or dark dot defects are as follows:
 - (i) Three joined dark dot defect must be nil.
 - (ii) Two pairs of joined dark dot defects are maximum.
(Two dark dots in junction is regarded as one dark dot).
- (c) Point defect definitions:
 - (i) Area \geq 1/2 Dot (0.0495x0.1485mm)
 - (ii) Bright dot defect is visible through 5% ND filter.
 - (iii) Dark dot defect is invisible through 5% ND filter.

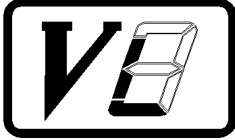


7.1.3 External Inspection

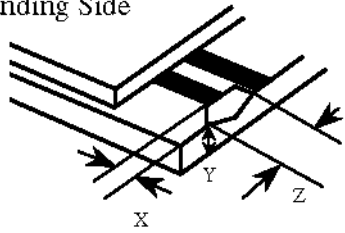
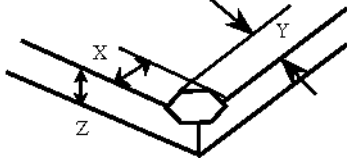
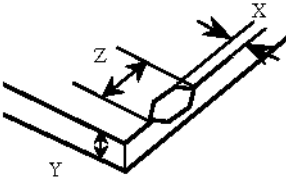
Inspection Item	Inspection standards			Note
	Width (mm)	Length (mm)	Acceptable Qty	
Scratches (Note 7)	$0.1 < W$	---	0	
	$0.05 < W \leq 0.1$	$L \leq 2.0$	2	
	$0.03 < W \leq 0.05$	$L \leq 4.0$	4	
	$W \leq 0.03$	---	Ignore	
Bubble on the polarizer (Circular) (Note 7)	<u>Average Diameter (mm)</u>		<u>Acceptable Qty</u>	
	$0.5 < D$		0	
	$0.25 < D \leq 0.5$		1	
	$D \leq 0.25$		Ignored	
Note: $D = (a + b) / 2$				
Bubble on the polarizer (Linear) (Note 7)	Invisible at Active area		<u>Acceptable Qty</u>	
			0	
Spots (Note 7) (Black and white) & Stain	<u>Average Diameter(mm)</u>		<u>Acceptable Qty</u>	
	$0.25 < D$		0	
	$0.15 < D \leq 0.25$		3	
	$D \leq 0.15$		Ignored	
Note: $D = (a + b) / 2$				
Maximum allowable number of defect	$N \leq 3$			

Note 7:





7.1.4

Up Strata Glass			
FPC Bounding Side	 <p>$X \leq 1.5\text{mm}$ Y: Ignore Z: Ignore</p>	Conner	 <p>$X \leq 2.0\text{mm}$ $Y \leq 2.0\text{mm}$ Z: Ignore</p>
Other Side	 <p>$x \leq 1.5\text{mm}$ Y: Ignore Z: Ignore</p>	Crack	None

7.2 Acceptable Quality Level (AQL)

7.2.1 Classification of Defects

Defects are classified as major defect and minor defect, according to the degree of defect defined herein.

7.2.2 Major Defect

A major defect is the defect that is likely to result in failure, or to reduce materially the usability of the product for its intended purpose.

7.2.3 Minor Defect

A minor defect either is the defect that is not likely to reduce materially the usability of the product for its intended purpose, or is a departure from an established having little bearing on the effective use or operation of the product.

Specific criteria of judgment on major or minor defects or otherwise shall be in accordance with the attached "Classification of defect".



7.3 Sampling Condition

Unless otherwise agreed in written, the sampling inspection shall be applied to the incoming inspection of customer.

7.3.1.1 Lot size: Quantity of shipment lot per model

7.3.1.2 Sampling type: Normal inspection, single sampling

7.3.1.3 Inspection level: Level II

7.3.1.4 Sampling table: ISO2859 (Also known as MIL-STD-105E)

7.4 The AQL for major and minor defects is defined as follows:

- Major defect: 0.4
- Minor defect: 1.0

7.5 Environmental Conditions

- Room temperature: 20 ~ 25°C
- Humidity: 65 ± 5% RH

7.6 Sampling Plan

Item	Inspection Item	Classification
1	No display function	Major
2	Line defect	Major
3	Dot defect	Minor
4	Scratches	Minor
5	Bubble on the polarizer(Circular)	Minor
6	Bubble on the polarizer (Linear)	Minor
7	Spots(Black and white) & Stain	Minor
8	Bezel appearance	Minor
Sampling table		MIL-STD-105E
Inspection level		Level II
Major defect		0.4
Minor defect		1.0



7.7 Defect comment

Note 1 : Line defect



Note 4 : Dark dot defect



Note 2 : Mura & Non-uniformity



Note 5 : Joined dot defect



Note 6: Small bright dot defect



Note 3 : Bright dot defect





8. Handling Cautions

8.1 ESD (Electrical Static Discharge) Strategy

ESD will cause serious damage of the panel, ESD strategy is very important in handling. Following items are the recommended ESD strategy

- (1) In handling LCD panel, please wear non-charged material gloves. Connect the wrist conduction ring to the earth and the conducting shoes to the earth are necessary.
- (2) The machine and working table for the panel should have ESD protection strategy.
- (3) In handling the panel, using ionized air to decrease the charge in the environment is necessary.
- (4) In the process of assembly the module, shield case should connect to the ground.

8.2 Environment

- (1) Working environment of the panel should be in the clean room.
- (2) The front polarizer is easy damaged. Handle it carefully and do not scratch it by sharp material.
- (3) Panel has polarizer protective film in the surface. Please remove the protection film of polarizer slowly with ionized air to prevent the electrostatic discharge.

8.3 Others

- (1) Turn off the power supply before connecting and disconnecting signal input cable.
- (2) Water drop on the surface or condensation as panel power on will corrode panel electrode.
- (3) As the packing bag open, watch out the environment of the panel storage. High temperature and high humidity environment is prohibited.
- (4) When the TFT LCD module is broken, please watch out whether liquid crystal leaks out or not. If your hand touches liquid crystal, wash your hand cleanly by water and soap as soon as possible.



9. Reliability Test Report

No	Test Item	Condition
1	High Temperature Operation	Ta = +70°C, 240hrs
2	High Temperature & High Humidity Operation	Ta = +40°C, 95% RH, 240hrs
3	Low Temperature Operation	Ta = -20°C, 240hrs
4	High Temperature Storage (non-operation)	Ta = +80°C, 240hrs
5	Low Temperature Storage (non-operation)	Ta = -30°C, 240hrs
6	Thermal Shock (non-operation)	-30°C \leftrightarrow 80°C, 50 cycles 30 min 30 min
7	Resistance to Static Electricity Discharge (non-operation)	C=200pF, R=0 Ω ; Discharge: \pm 150V 3 times / Terminal
8	Surface Discharge (non-operation)	C=150pF, R=330 Ω ; Discharge: Air: \pm 15kV; Contact: \pm 8kV 5 times / Point; 5 Points / Panel

Ta: Ambient Temperature

“Varitronix Limited reserves the right to change this specification.”

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