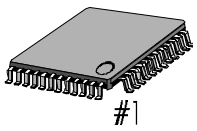
INTRODUCTION

44-QFP-1010B



- AM: AM RF MIXER, AM OSC,
  AM_IF AMP, AM Detector,
  AGC, Tuning LED Driver,
  OSC Buffer, IF Buffer
- FM: RF AMP, FM RF MIXER,
  FM OSC, FM_IF AMP,
  Quadrature Detector,
  Tuning LED Driver,
  OSC Buffer, IF Buffer
- MPX: PLL, Stereo Decoder, Stereo LED, MPX VCO Self-adjustment
- DTS : Prescaler, AM/FM Programmable Divider, AM/FM IF Counter, Lock Detector, LED Controller
- Microprocessor Interface

FEATURE

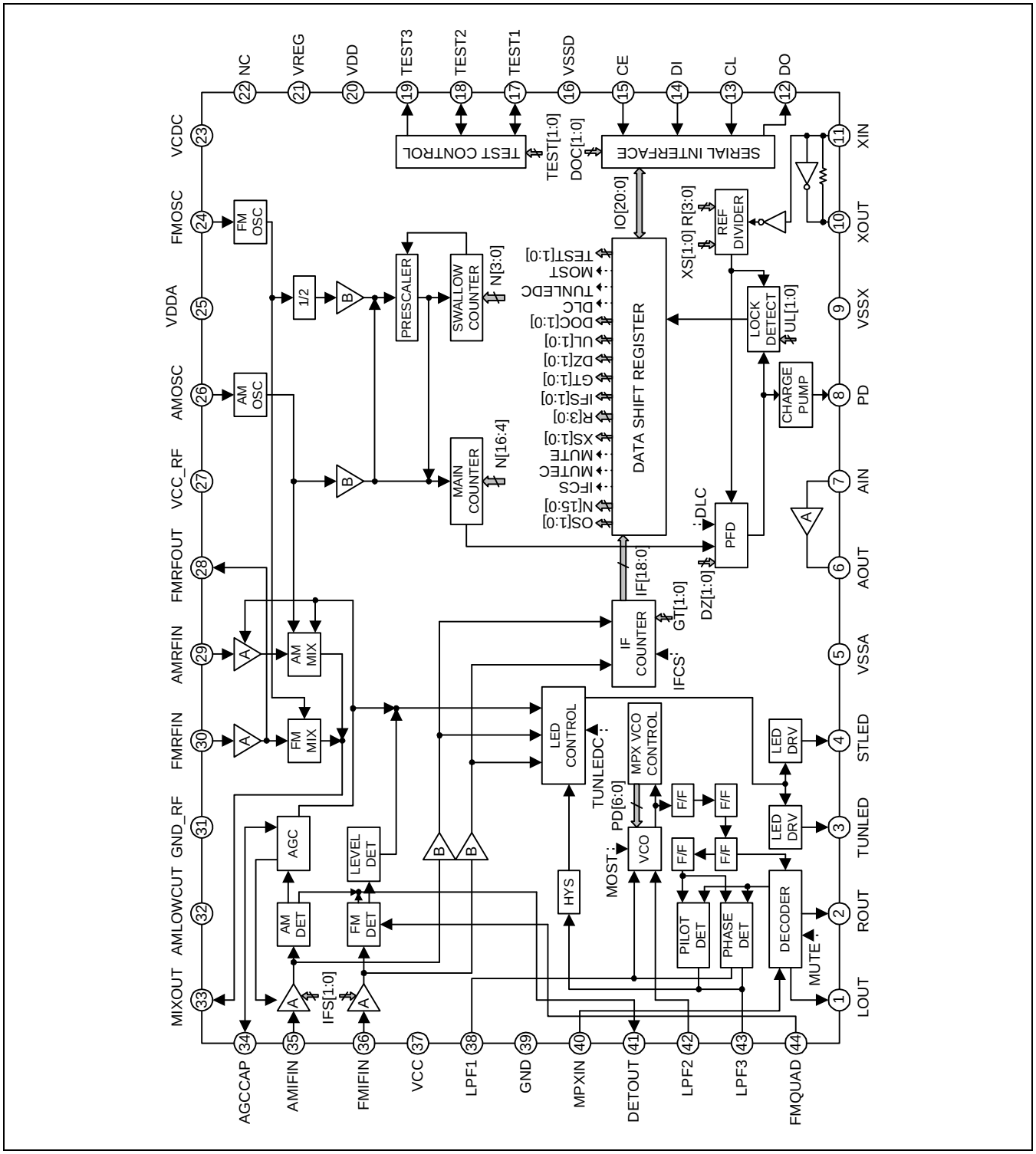
- Adopt New FCC
- AM/FM 1 Chip DTS with PLL
- MPX-VCO Self-adjustment
- Programmable Divider
  FM: 10 to 160MHz <pulse swallow technique>
  AM: 0.5 to 10MHz <direct division technique>
- IF COUNTER : 0.4 to 12MHz <AM/FM IF COUNTING>
- Reference Frequency
  Twelve Selectable Frequency
  1, 3, 5, 9, 10, 3.125, 6.25, 12.5, 15, 25, 50, and 100kHz
  (Selectable Crystal 75kHz, 3.6MHz, 7.2MHz, 10.8MHz choice)
- Built-in Transistor for forming an active low-pass filter
- Package : 44 QFP/48 LQFP

ORDERING INFORMATION

Device	Package	Supply voltage	Operating Temperature
S1A0903X01-Q0R0	44-QFP-1010B	2 to 7V	-20 to +75°C
S1A0903X01-E0R0	48-LQFP-0707AN		

BLOCK DIAGRAM

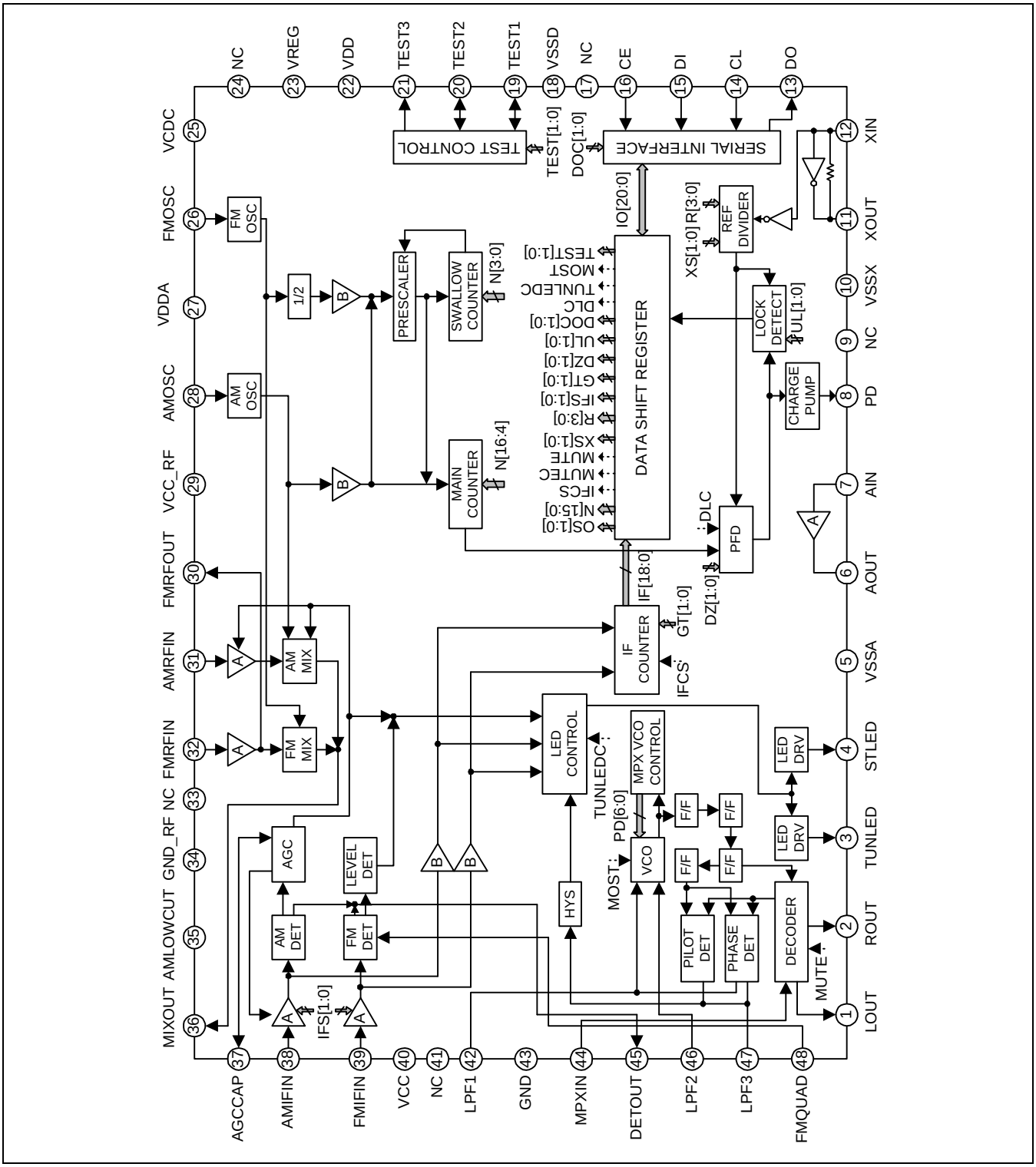
44-QFP



SAMSUNG ELECTRONICS

BLOCK DIAGRAM

48-LQFP



PIN CONFIGURATION

Pin No.		Symbol	In/Out	Function
44-QFP	48-LQFP			
1	1	LOUT	O	Stereo left channel output
2	2	ROUT	O	Stereo right channel output
3	3	TUNLED	O	Tuning LED
4	4	STLED	O	Stereo LED
5	5	VSSA	-	Ground
6	6	AOUT	O	Connections for the Tr. used for the PLL active LPF.
7	7	AIN	I	
8	8	PD	O	PLL charge pump output
9	10	VSSX	-	Crystal GND
10	11	XOUT	I	Crystal oscillator element connection
11	12	XIN	O	(75kHz, 3.6MHz, 7.2MHz, 10.8MHz)
12	13	DO	O	Serial data output to the microprocessor
13	14	CL	I	Clock used for data synchronization for serial data input(DI) and serial data output(DO)
14	15	DI	I	Serial data input from the microprocessor
15	16	CE	I	Chip enable for serial I/O
16	18	VSSD	-	Ground
17	19	TEST1	I/O	Only for test
18	20	TEST2	I/O	
19	21	TEST3	O	
20	22	VDD	-	Regulator voltage input
21	23	VREG	-	Regulator voltage output
22	24	NC	-	No connection

* 48-LQFP: 9, 17 pin NC

PIN CONFIGURATION (Continued)

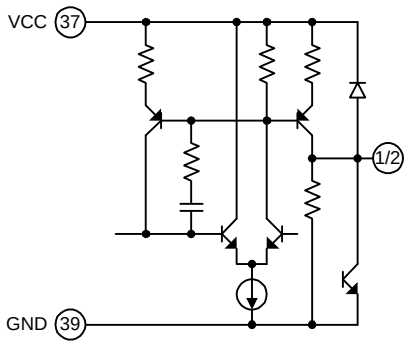
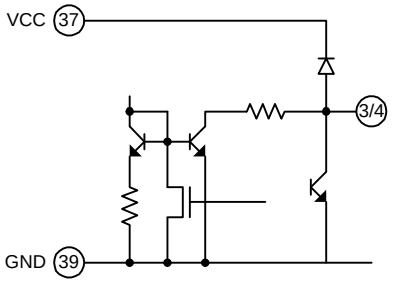
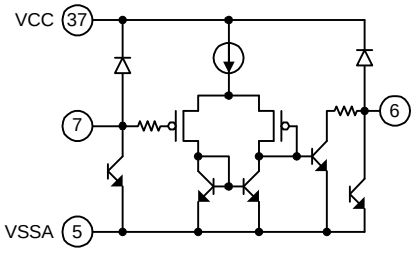
Pin No.		Symbol	In/Out	Function
44-QFP	48-LQFP			
23	25	VCDC	-	VCC ripple rejection cap.
24	26	FMOSC	I	FM oscillator input
25	27	VDDA	-	Power
26	28	AMOSC	I	AM oscillator input
27	29	VCC_RF	-	RF-Power
28	30	FMRFOUT	O	FM RF output
29	31	AMRFIN	I	AM RF input
30	32	FMRFIN	I	FM RF input
31	34	GND_RF	-	RF-Ground
32	35	AMLOWCUT	-	AM lowcut cap.
33	36	MIXOUT	O	AM/FM MIX output
34	37	AGCCAP	-	AGC cap.
35	38	AMIFIN	I	AM IF input
36	39	FMIFIN	I	FM IF input
37	40	VCC	-	Power
38	42	LPF1	-	connection for the phase detector and the VCO LPF
39	43	GND	-	Ground
40	44	MPXIN	I	MPX input
41	45	DETOUT	O	AM/FM Detect Output
42	46	LPF2	-	connection for the VCO LPF
43	47	LPF3	-	connection for the pilot detector and the phase detector LPF
44	48	FMQUAD	-	connection for the FM QUAD detector resonator

* 48-LQFP: 33, 41 pin NC

PIN DESCRIPTION

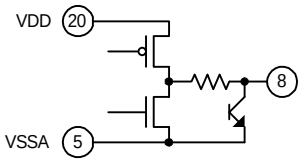
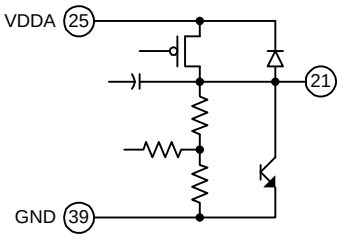
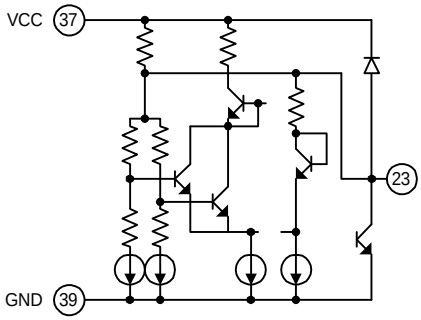
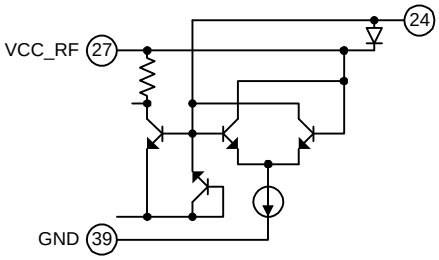
ANALOG BLOCK I/O PIN

(Terminal voltage: Typical terminal voltage at no signal with test circuit, V_{CC} = 3V, Ta = 25°C)

Pin No.		Pin Name	Internal Circuit (Standard 44-QFP Device)	Terminal(Typ.) Voltage (V)	
44-QFP	48-LQFP			AM	FM
1 2	1 2	LOUT ROUT		1.1	1.1
3 4	3 4	TUNLED STLED		-	-
5	5	VSSA			
6 7	6 7	AOUT AIN		- -	- -

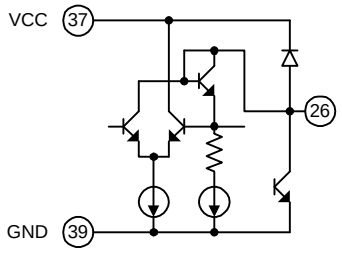
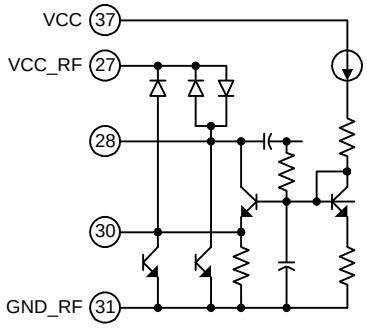
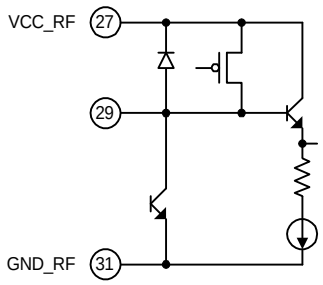
ANALOG BLOCK I/O PIN (Continued)

(Terminal voltage: Typical terminal voltage at no signal with test circuit, V_{CC} = 3V, Ta = 25°C)

Pin No.		Pin Name	Internal Circuit (Standard 44-QFP Device)	Terminal(Typ.) Voltage (V)	
44-QFP	48-LQFP			AM	FM
8	8	PD		-	-
9 — 20	10 — 22		cf. Digital block I/O PIN		
21	23	VREG		1.8	1.8
22	24	NC		-	-
23	25	VCCCAP		2.85	3.0
24	26	FMOSC		3.0	3.0

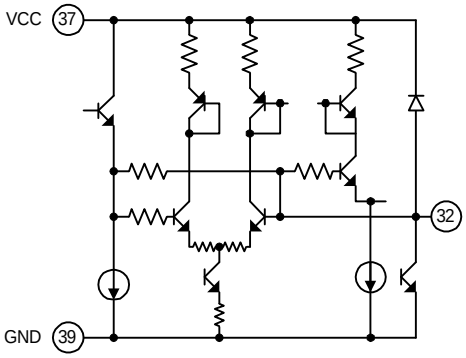
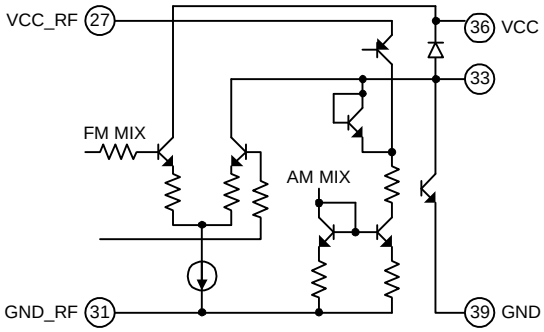
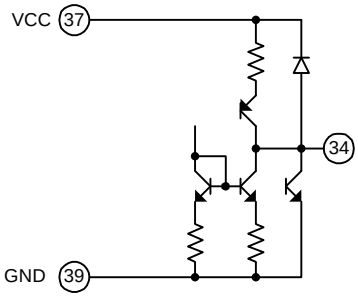
ANALOG BLOCK I/O PIN (Continued)

(Terminal voltage: Typical terminal voltage at no signal with test circuit, V_{CC} = 3V, Ta = 25°C)

Pin No.		Pin Name	Internal Circuit (Standard 44-QFP Device)	Terminal(Typ.) Voltage (V)	
44-QFP	48-LQFP			AM	FM
25	27	VDDA	-	3.0	3.0
26	28	AMOSC		3.0	3.0
27	29	VCC_RF	-	3.0	3.0
28 30	30 32	FMRFOUT FMRFIN		3.0 0	3.0 0.8
29	31	AMRFIN		3.0	3.0
30	32	FMRFIN	cf. PIN28		
31	34	GND_RF	-	0	0

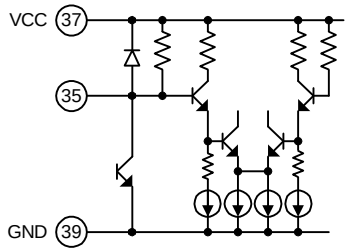
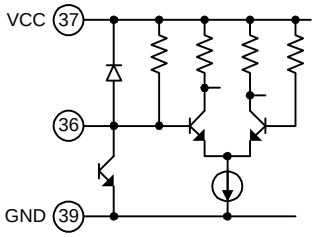
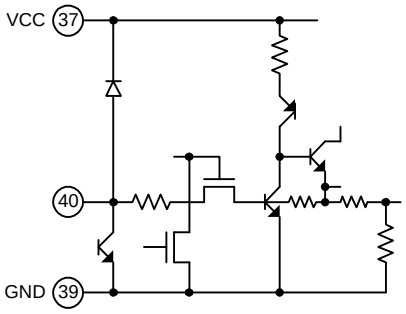
ANALOG BLOCK I/O PIN (Continued)

(Terminal voltage: Typical terminal voltage at no signal with test circuit, V_{CC} = 3V, Ta = 25°C)

Pin No.		Pin Name	Internal Circuit (Standard 44-QFP Device)	Terminal(Typ.) Voltage (V)	
44-QFP	48-LQFP			AM	FM
32	35	AMLOWCUT		1.7	-
33	36	MIXOUT		3.0	2.9
34	37	AGCCAP		-	-

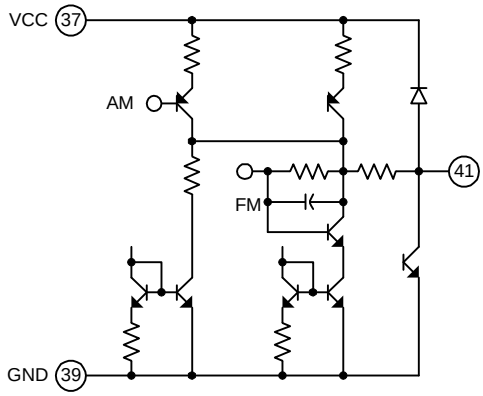
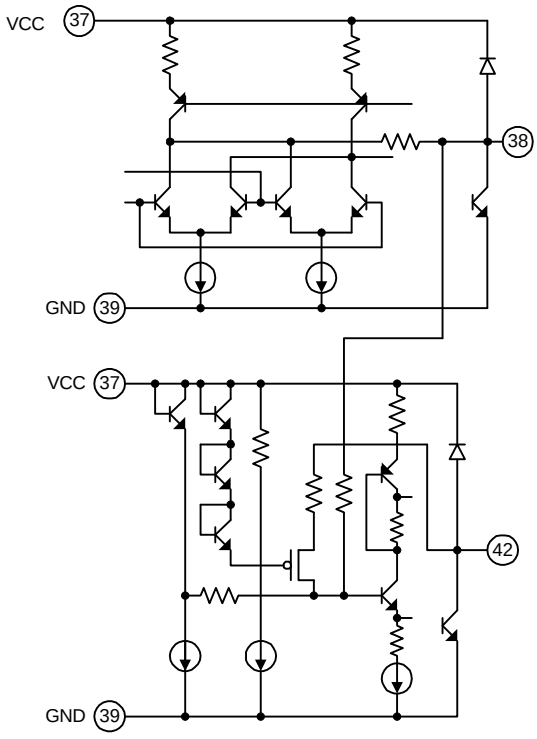
ANALOG BLOCK I/O PIN (Continued)

(Terminal voltage: Typical terminal voltage at no signal with test circuit, V_{CC} = 3V, Ta = 25°C)

Pin No.		Pin Name	Internal Circuit (Standard 44-QFP Device)	Terminal(Typ.) Voltage (V)	
44-QFP	48-LQFP			AM	FM
35	38	AMIFIN		3.0	3.0
36	39	FMIFIN		3.0	3.0
37	40	VCC	-	3.0	3.0
38	42	LPF1	cf. PIN42	2.2	2.2
39	43	GND	-	0	0
40	44	MPXIN		0.8	0.8

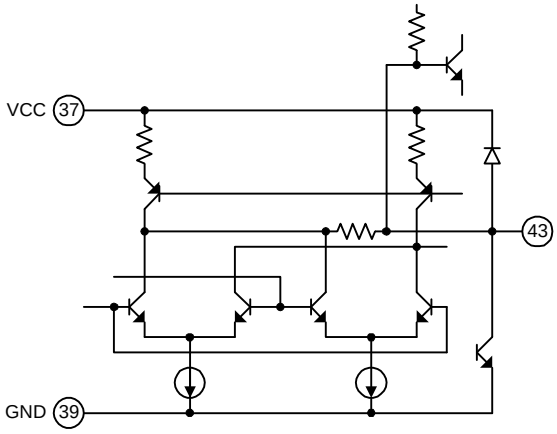
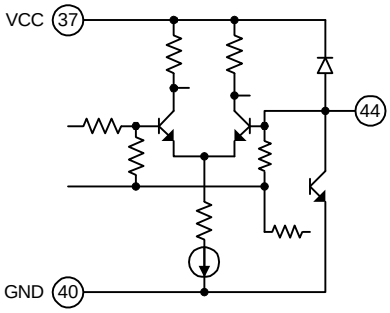
ANALOG BLOCK I/O PIN (Continued)

(Terminal voltage: Typical terminal voltage at no signal with test circuit, V_{CC} = 3V, Ta = 25°C)

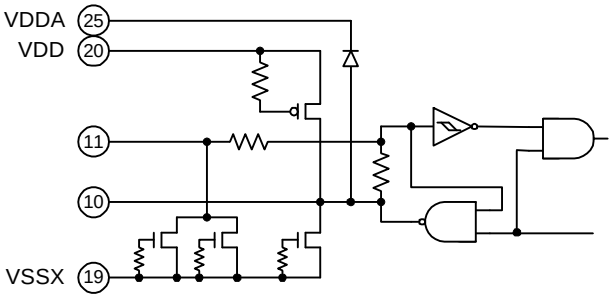
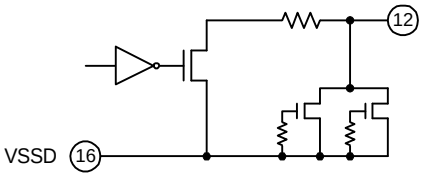
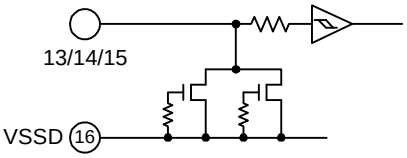
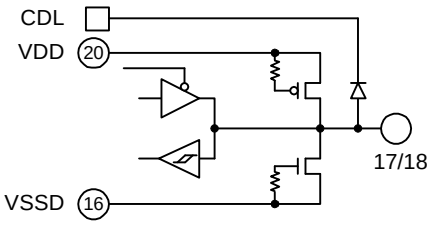
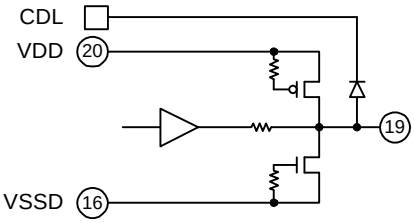
Pin No.		Pin Name	Internal Circuit (Standard 44-QFP Device)	Terminal(Typ.) Voltage (V)	
44-QFP	48-LQFP			AM	FM
41	45	DETOUT		1.0	1.0
38 42	42 46	LPF1 LPF2		2.2	2.2

ANALOG BLOCK I/O PIN (Continued)

(Terminal voltage: Typical terminal voltage at no signal with test circuit, V_{CC} = 3V, Ta = 25°C)

Pin No.		Pin Name	Internal Circuit (Standard 44-QFP Device)	Terminal(Typ.) Voltage (V)	
44-QFP	48-LQFP			AM	FM
43	47	LPF3		2.2	2.2
44	48	FMQUAD		2.2	2.2

DIGITAL BLOCK I/O PIN

Pin No.		Pin Name	Internal Circuit (Standard 44-QFP device)	Remark
44-QFP	48-LQFP			
9	10	VSSX		
10 11	11 12	XOUT XIN		
12	13	DO		
13 14 15	14 15 16	CL DI CE		
16	18	VSSD		
17 18	19 20	TEST1 TEST2		
19	21	TEST3		
20	22	VDD		

INPUT AND OUTPUT OF SERIAL DATA

SERIAL DATA FORMAT AND TIMING

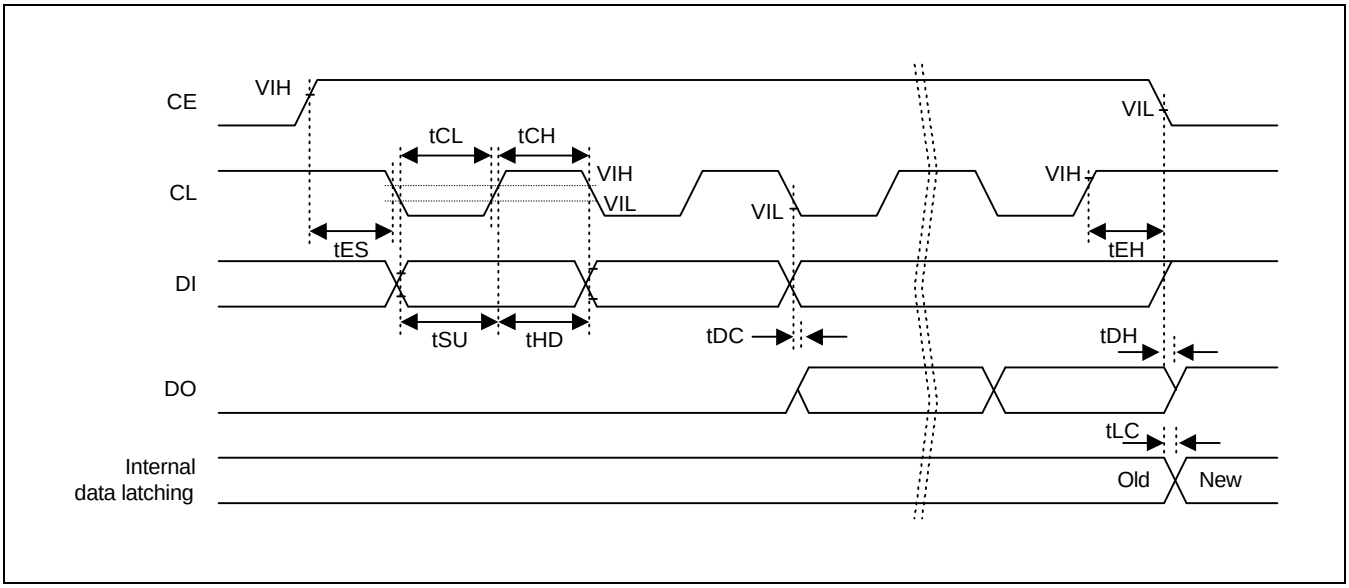
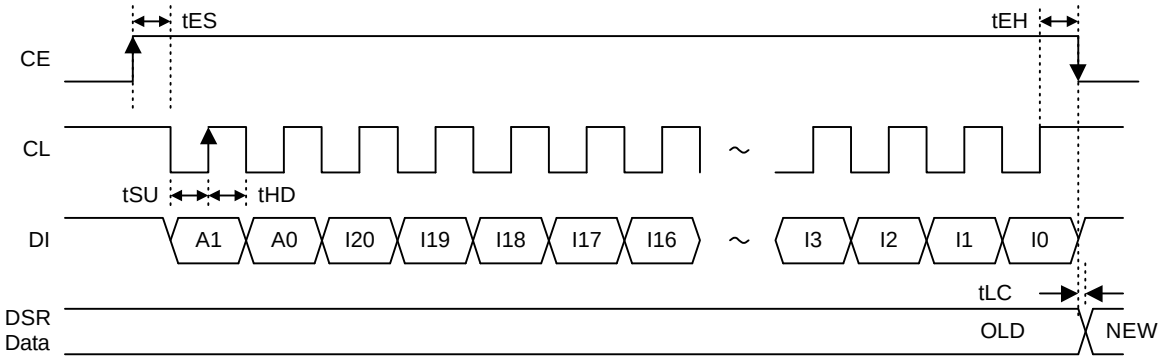


Figure 1. Serial Data I/O Format and Timing

Parameter	Symbol	Conditions	Ratings			Unit
			Min.	Typ.	Max.	
Data setup time	t_{SU}	DI, CL	0.75	-	-	µs
Data hold time	t_{HD}	DI, CL	0.75	-	-	µs
Cock low level time	t_{CL}	CL	0.75	-	-	µs
Clock high level time	t_{CH}	CL	0.75	-	-	µs
CE setup time	t_{ES}	CE, CL	0.75	-	-	µs
CE hold time	t_{EH}	CE, CL	0.75	-	-	µs
Data latch change time	t_{LC}		-	-	0.75	µs
Data output time	t_{DC}	DO, CL	-	-	0.35	µs
	t_{DH}	DO, CE	-	-	0.35	µs

STRUCTURE OF DI CONTROL DATA(SERIAL DATA INPUT)



[IN1 MODE]

DI	A1	A0	I20	I19	I18	I17	I16	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
	0	1	OS1	OS0	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	IFCS	MUTEC	MUTE
	ADDRESS		OSC SELECT		PROGRAMMABLE DIVISOR DATA (N1[3:0] : 4 BIT , N2[15:4] : 12 BIT)																IF CNT. START	MUTE OFF CONTROL	MUTE ON/OFF

[IN2 MODE]

DI	A1	A0	I20	I19	I18	I17	I16	I15	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
	1	0	XS1	XS0	R3	R2	R1	R0	IFS1	IFS0	GT1	GT0	DZ1	DZ0	UL1	UL0	DOC1	DOC0	DLC	TUNLEDC	MOST	TEST1	TEST0
	ADDRESS		X'TAL SELECT		REFERENCE DIVIDER DATA				IF SENSITIVITY CONTROL		IF MEASURE TIME		DEADZONE CONTROL		UNLOCK CONTROL		DO PIN CONTROL		DEADLOCK CLEAR	TUNLED CONTROL	MO/ST CONTROL	TEST DATA	

Figure 2. Serial Data Input Timing and Format

DI CONTROL DATA

<table>
<tr><th>No.</th><th>Control Block/Data</th><th>Function</th></tr>
<tr><td>1</td><td>Programmable Divider Data

OS<1:0>
N<15:0></td><td>
• Select the input source
<table>
<tr><th>OS1</th><th>OS0</th><th>LSB</th><th>AM/FM</th><th>Frequency Range</th><th>Divisor(N)</th></tr>
<tr><td>1</td><td>0</td><td>N0</td><td>FM</td><td>10 — 160MHz</td><td>256 — 65535</td></tr>
<tr><td>0</td><td>0</td><td>N4</td><td>AMLF</td><td>0.5 — 10MHz</td><td>4 — 4096</td></tr>
</table>
♦ FM : Real divisor = 2 × N
AM : Real divisor = N
♦ N[3:0] are "don't care" in the case of AMLF
</td></tr>
<tr><td>2</td><td>If Counter Start Data
IFCS</td><td>
• IF counter start control data
♦ IFCS = 1 : Start the IF counter
IFCS = 0 : Reset the IF counter
♦ After OUTMODE SIO, IFCS is automatically reset to 0
</td></tr>
<tr><td>3</td><td>Mute Control Data

MUTEC, MUTE</td><td>
• MUTE select/control data
<table>
<tr><th>MUTEC</th><th>MUTE</th><th colspan="2">Function</th></tr>
<tr><td>0</td><td>0</td><td>MUTE off</td><td rowspan="2">Self controlled</td></tr>
<tr><td>0</td><td>1</td><td>MUTE on</td></tr>
<tr><td>1</td><td>0</td><td>MUTE off</td><td rowspan="2">Microprocessor
controlled</td></tr>
<tr><td>1</td><td>1</td><td>MUTE on</td></tr>
</table>
♦ MUTEC = 0 : Microprocessor set MUTE
MUTE is automatically reset when tuning LED is on
♦ Whenever BAND is switched from AM to FM, MUTE is automatically on until MPX VCO free-running frequency self_adjustment is end
</td></tr>
<tr><td>4</td><td>Reference Crystal Data

XS<1:0></td><td>
• Crystal selection data
<table>
<tr><th>XS1</th><th>XS0</th><th>CRYSTAL OSC.</th></tr>
<tr><td>0</td><td>0</td><td>3.6MHz</td></tr>
<tr><td>0</td><td>1</td><td>75kHz</td></tr>
<tr><td>1</td><td>0</td><td>7.2MHz</td></tr>
<tr><td>1</td><td>1</td><td>10.8MHz</td></tr>
</table>
</td></tr>
</table>

DI CONTROL DATA (Continued)

<table>
<tr><th>No.</th><th>Control Block/Data</th><th>Function</th></tr>
<tr><td>5</td><td>Reference
Frequency
Select Data

R<3:0></td><td>
• Reference frequency selection
<table>
<tr><th rowspan="2">R3</th><th rowspan="2">R2</th><th rowspan="2">R1</th><th rowspan="2">R0</th><th colspan="2">Reference frequency</th></tr>
<tr><th>3.6,7.2,10.8MHz</th><th>75kHz</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>100 kHz</td><td rowspan="3">25 kHz</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>50 kHz</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>25 kHz</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>15 kHz</td><td>15 kHz</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0</td><td>12.5 kHz</td><td rowspan="2">12.5 kHz</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>10 kHz</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>9 kHz</td><td rowspan="2">6.25 kHz</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>1</td><td>6.25 kHz</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>5 kHz</td><td>5 kHz</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>3.125 kHz</td><td>3.125 kHz</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>3 kHz</td><td>3 kHz</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>1 kHz</td><td>1 kHz</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0</td><td colspan="2">♣</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td colspan="2">All stop</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td colspan="2">PLL stop + X'tal OSC. stop</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>1</td><td colspan="2">PLL stop</td></tr>
</table>
♦ PLL stop mode
Programmable divider and IF counter are stopped.
Charge Pump's output is a high- impedance state.
♦ All stop mode
All the frequency of DTS control block is stopped Control data are holded the previous state
♣ : No use
</td></tr>
<tr><td>6</td><td>If
Sensitivity
Control Data

IFS<1:0></td><td>
• IF sensitivity control
<table>
<tr><th>IFS1</th><th>IFS0</th><th>Sensitivity (AM / FM)</th></tr>
<tr><td>0</td><td>0</td><td>0dB / 0dB</td></tr>
<tr><td>0</td><td>1</td><td>-4B / -5dB</td></tr>
<tr><td>1</td><td>0</td><td>-8B / -10dB</td></tr>
<tr><td>1</td><td>1</td><td>-12/ -16dB</td></tr>
</table>
</td></tr>
</table>

DI CONTROL DATA (Continued)

<table>
<tr><th>No.</th><th>Control Block/Data</th><th>Function</th></tr>
<tr><td>7</td><td>If Counter
Control Data

GT<1:0></td><td>• Select IF counter measurement time
<table>
<tr><th>GT1</th><th>GT0</th><th>Measurement time (ms)</th></tr>
<tr><td>0</td><td>0</td><td>4</td></tr>
<tr><td>0</td><td>1</td><td>8</td></tr>
<tr><td>1</td><td>0</td><td>16</td></tr>
<tr><td>1</td><td>1</td><td>32</td></tr>
</table></td></tr>
<tr><td>8</td><td>Dead Zone
Control Data

DZ<1:0></td><td>• Dead zone data
<table>
<tr><th>DZ1</th><th>DZ0</th><th>Charge Pump</th><th>DeadZone</th></tr>
<tr><td>0</td><td>0</td><td>ON</td><td>--0</td></tr>
<tr><td>0</td><td>1</td><td>ON</td><td>-0</td></tr>
<tr><td>1</td><td>0</td><td>OFF</td><td>+0</td></tr>
<tr><td>1</td><td>1</td><td>OFF</td><td>++0</td></tr>
</table>
♦ ON: Both of NMOS and PMOS in Charge pump turn on in the same time and Dead zone is reduced
♦ OFF: Each of NMOS and PMOS in Charge pump turn mutual exclusively on</td></tr>
<tr><td>9</td><td>Unlock State
Control Data

UL<1:0></td><td>• decide the LOCK state with the width of Phase error(ψ E)
<table>
<tr><th>UL1</th><th>UL0</th><th>ψ E Detection Width</th><th>DO Pin State</th></tr>
<tr><td>0</td><td>0</td><td>stopped</td><td>hold the previous state</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ψ E is directly out</td></tr>
<tr><td>1</td><td>0</td><td>± 0.55us</td><td rowspan="2">ψ E is extended by 2ms</td></tr>
<tr><td>1</td><td>1</td><td>± 1.11us</td></tr>
</table>
♦ DOC[1:0] = 2: DO pin is controlled with LOCK state
♦ UL[1:0] = 1: Width of ψ E set DO pin low, else high</td></tr>
</table>

DI CONTROL DATA (Continued)

<table>
<tr><th>No.</th><th>Control Block/Data</th><th>Function</th></tr>
<tr><td>10</td><td>DO Pin
Control Data

DOC<1:0></td><td>• DO pin control data
<table>
<tr><th>DOC1</th><th>DOC0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td rowspan="2">DO pin open</td></tr>
<tr><td>0</td><td>1</td></tr>
<tr><td>1</td><td>0</td><td>DTS PLL = lock, DO pin = open</td></tr>
<tr><td>1</td><td>1</td><td>IF counting = end, DO pin = low</td></tr>
</table>
♦ When CE is low, DOC[1:0] controls DO pin</td></tr>
<tr><td>11</td><td>Deadlock Clear
Control Data

DLC</td><td>• Deadlock clear data
♦ DLC = 1 : The output of Charge pump is forcibly set to low, which makes control voltage VCC and gets out of DEADLOCK condition
♦ DLC = 0 : Normal operation</td></tr>
<tr><td>12</td><td>Tuning Led
Control Data

TUNLEDC</td><td>• LED control data
<table>
<tr><th>TUNLEDC</th><th>AM</th><th>FM</th></tr>
<tr><td>0</td><td>IF ≥ 32dBμ
=> LED On</td><td>IF ≥ 45dBμ
=> LED On</td></tr>
<tr><td>1</td><td>IF ≥ 32dBμ and within
450kHz ± 5kHz
=> LED On</td><td>IF ≥ 45dBμ and within
10.7MHz ± 12.5kHz
=> LED On</td></tr>
</table>
♦ Abobe condition is IFS[1:0] = 0
♦ The point of turning Tuning LED on depends on the value of IFS[1:0]</td></tr>
<tr><td>13</td><td>Mono, Stereo Control Data
MOST</td><td>• MONO/STEREO control
♦ MOST = 1 : Set STEREO mode
♦ MOST = 0 : Set forcibly MONO mode</td></tr>
<tr><td>14</td><td>Test
Control Data

TEST<1:0></td><td>• Test data
<table>
<tr><th>TEST1</th><th>TEST0</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>NORMAL OPERATION</td></tr>
<tr><td>0</td><td>1</td><td>TEST MODE1</td></tr>
<tr><td>1</td><td>0</td><td>TEST MODE2</td></tr>
<tr><td>1</td><td>1</td><td>TEST MODE3</td></tr>
</table></td></tr>
</table>

STRUCTURE OF DO OUTPUT DATA(SERIAL TEST DATA OUTPUT)

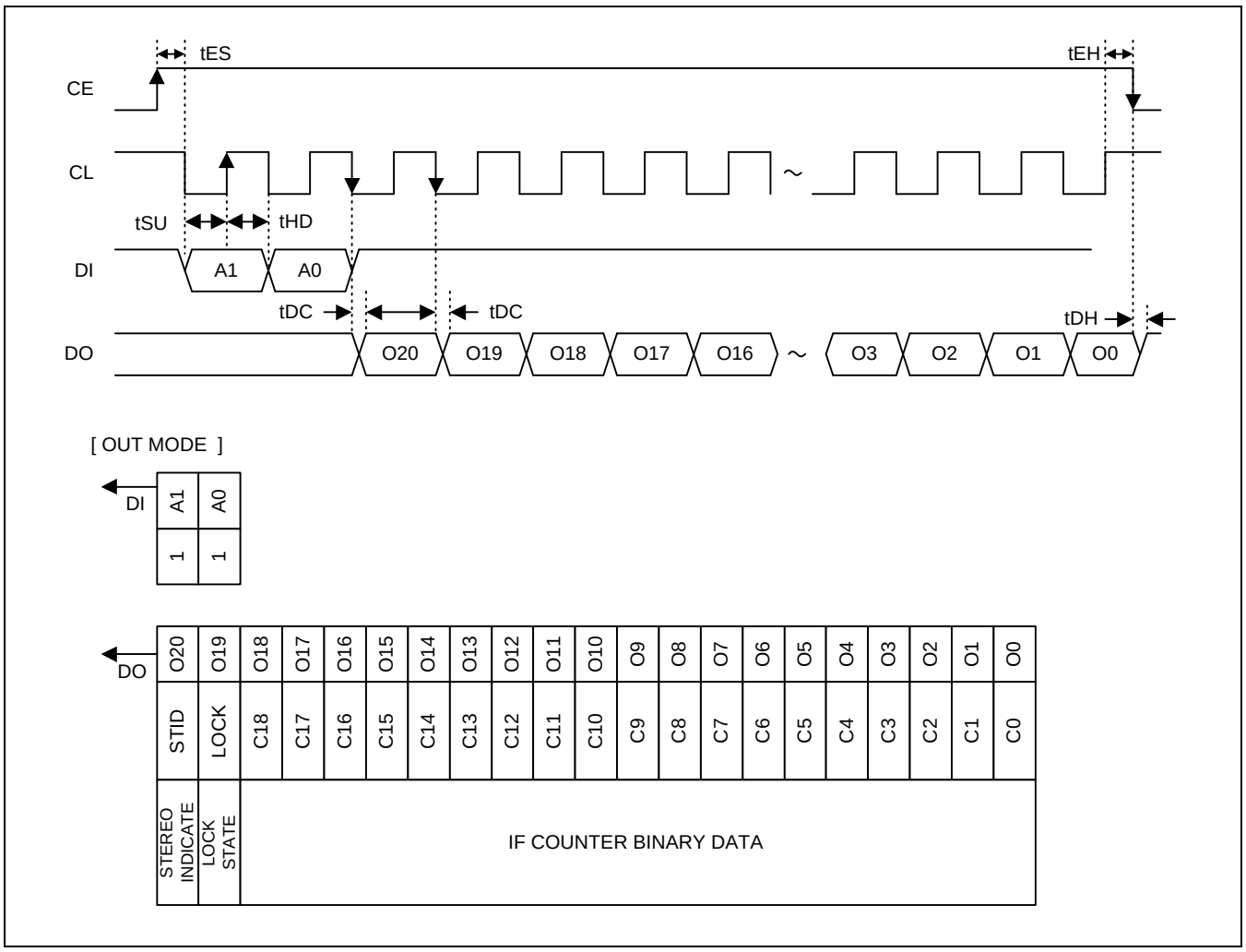


Figure 3. Serial Data Output Timing and Format

DI OUTPUT DATA

No.	Control Block/Data	Function
1	STEREO INDICATION DATA STID	STID = 1 : detect STEREO STID = 0 : detect MONO
2	PLL LOCKED STATE DATA LOCK	LOCK = 1 : PLL is lock LOCK = 0 : PLL isn't lock
3	IF COUNTER BINARY DATA C18 — C0	C18 : IF counter value (MSB) C0 : IF counter value (LSB)

STRUCTURE OF TEST MODE DO OUTPUT DATA(SERIAL DATA OUTPUT)

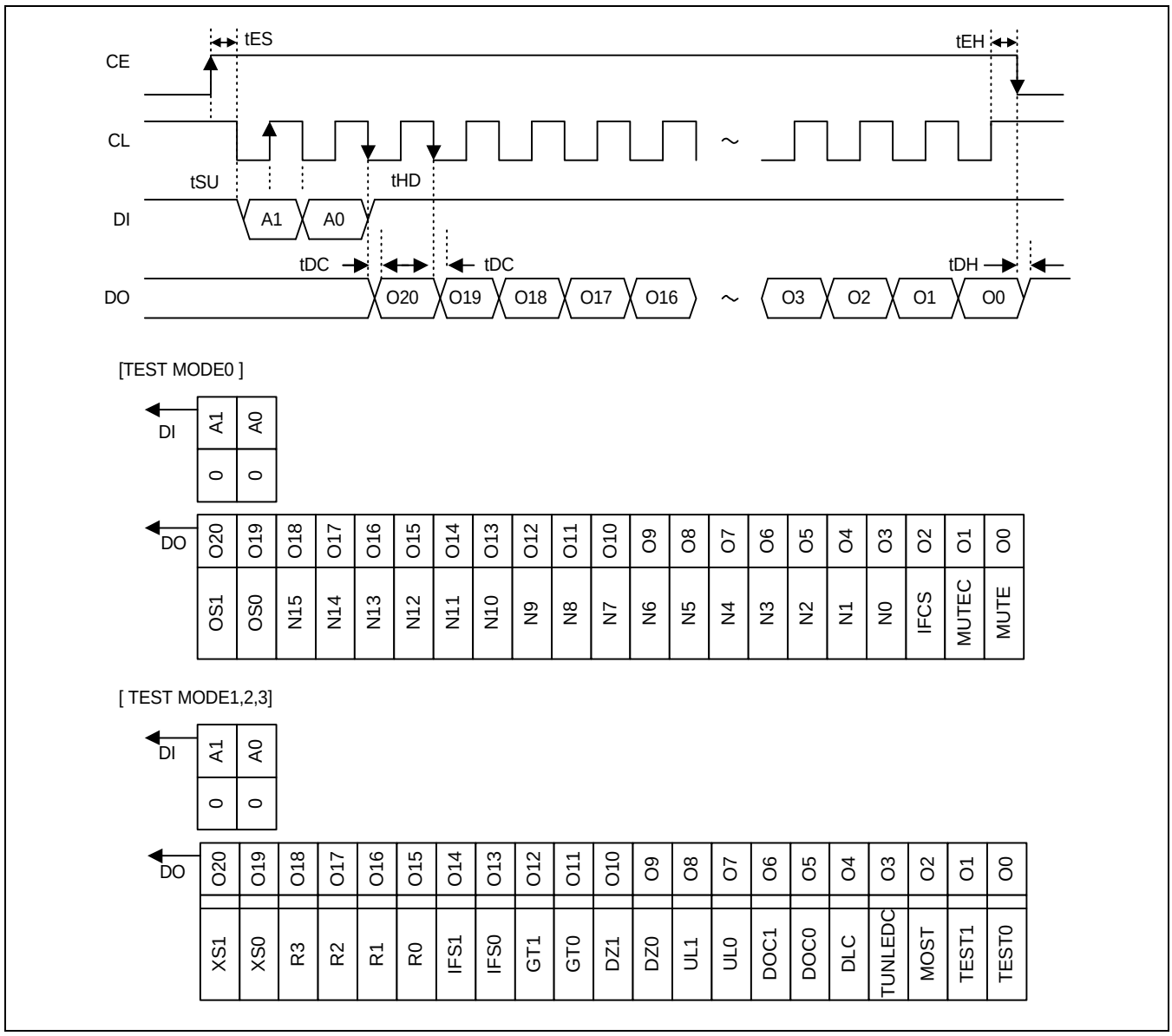


Figure 4. Serial Test Data Output Timing and Format

DO OUTPUT DATA

No.	Mode	Function
1	TEST MODE0	When TEST[1:0]=0 in MODE2 data, IN1 data in Data Shift Register is sent from DO pin to Microprocessor synchronously with the CL
2	TEST MODE1,2,3	When TEST[1:0]=1,2,3 in MODE2 data, IN1 data in Data Shift Register is sent from DO pin to Microprocessor synchronously with the CL

PROGRAMMABLE DIVIDER STRUCTURE

SERIAL INTERFACE

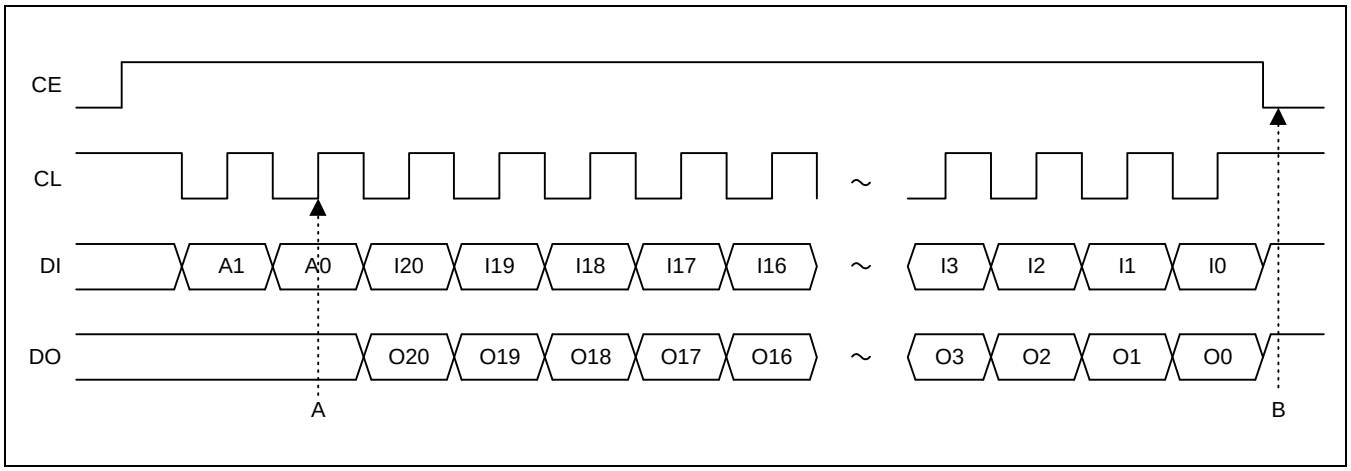


Figure 5. Serial I/O Timing

A[1:0]	Mode	DI / DO	Remarks
0	TEST	♦ Data of IN1(TEST[1:0]=0) or IN2(TEST[1:0]=1,2,3) latched in DSR are transferred to serial interface, which data are transferred to Micro-processor through DO pin synchronized with the CL	
1	IN1	♦ Data I[20:0] from DI pin are latched in IN1 or IN2 Data shift register on B point.	
2	IN2	♦ When OS[1:0] in IN1 MODE is changed, N[16:0] is changed and R[3:0] is changed from PLL STOP MODE, Fr and Fc counter are reset which make lock time of PLL fixed.	
3	OUT	♦ Data of OUT MODE latched in DSR are transferred on A point, which data transferred to Microprocessor through DO pin synchronized with the CL. ♦ IFCS bit is reset on B point, which makes Micro-processor restart IF counter	

CE	DOC1	DOC0	OUTMODE	DO Pin State
0	0	0	X	Open
0	0	1	X	Open
0	1	0	X	When LOCK bit in OUT MODE is high, DO pin holds the low state.
0	1	1	X	When IF counting is end, DO pin holds the low state.
1	X	X	0	Open
1	X	X	1	OUTMODE data are transferred through DO pin

X : don't care

1/N BLOCK

1/N block is used for frequency down-scaling from AM OSC. or FM OSC. to reference frequency Fr and Prescaler, Swallow Counter, Main Counter is used for a natural number dividing.

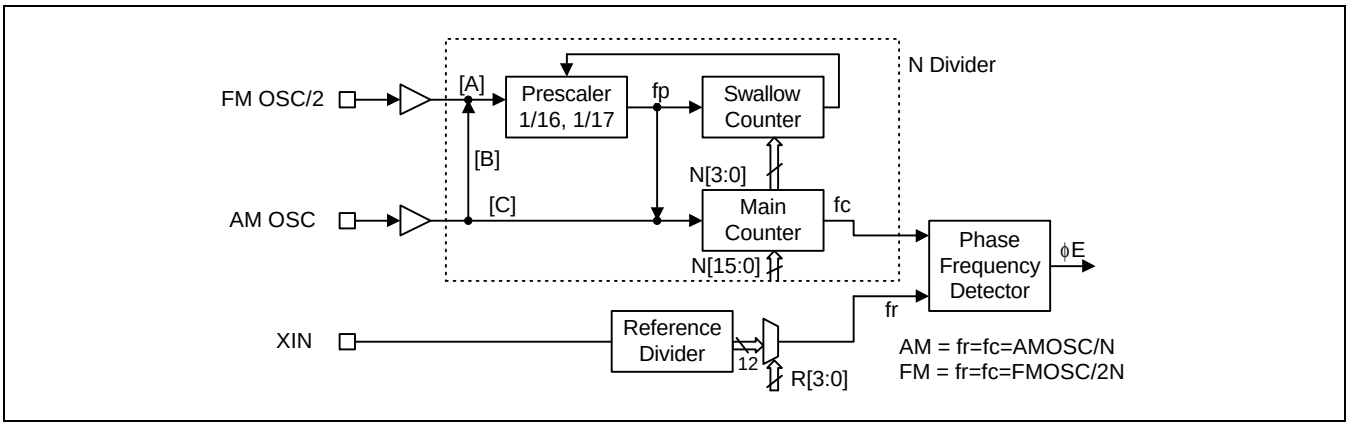


Figure 6. 1/N block diagram

	OS1	OS0	Input Frequency	Input Frequency Range
A	1	0	FM / 2	5 — 80 MHz
B	0	0	AMLF	0.5 — 10 MHz

- N = (16 × N2) + N1
  = 17 × N1 + 16 × (N2 - N1)
- Fc is derived from OSC. divided by N, N2 is derived from N[16:4] and N1 is derived from N[3:0]

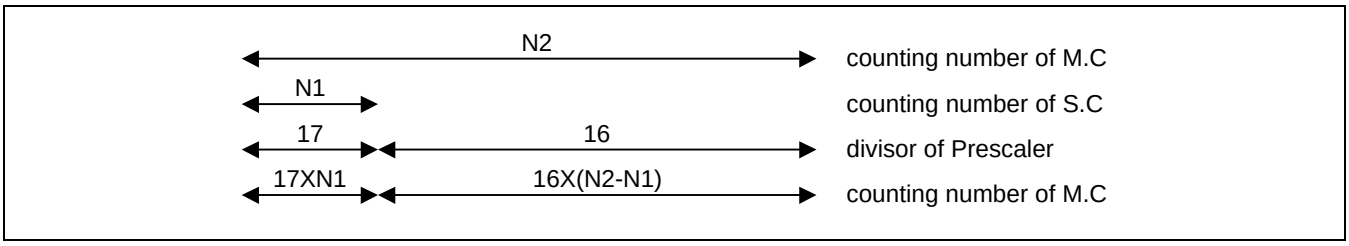


Figure 7. 1/N counting method

- Prescaler : operates on FM MODE.
- Swallow Counter : counts down with N1 divisor and divides Fp by 17 on operation of swallow counter and divide by 16 until S.C reloads N1 at the end of Fc 1 period.
- Main Counter : makes Fc divided by N2 divisor from Fp divided by 16 or 17
- Reference Divider : makes Fr divided by R[3:0] divisor from X'tal.

- For FM with a step size of 50kHz
  FM RF = 89.3MHz (IF = 10.7MHz)
  FM VCO = 100.0MHz
  Reference clock(Fr) = 50kHz
  100.0MHz(FM VCO) ÷ 50kHz(fr) ÷ 2 = 1000 → 03E8(hex)

OS1	OS0	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	IFCS	MUTEC	MUTE
1	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	X	X	X
		0				3				E				8						

X : don't care

- For AMLF with a step size of 9kHz
  AMLF RF = 1161kHz (IF = 450kHz)
  AM VCO = 1611kHz
  Reference clock(fr) = 9kHz
  1611kHz(AM VCO) ÷ 9kHz(fr) = 179 → OB3(hex)

OS1	OS0	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	IFCS	MUTEC	MUTE
0	0	0	0	0	0	1	0	1	1	0	0	1	1	X	X	X	X	X	X	X
		0				B				3				X						

X : don't care

- Fc generated by First example of setting 'N' divisor
  N[15:0] = 03E8(hex) = 1000(dec)
  N1 = N[3:0] = 8
  N2 = N[15:4] = 3E(hex) = 62(dec)
  Fc is divided by 17 with the amount of N1 and divided by 16 with the amount of N2 - N1 in Figure. 8.

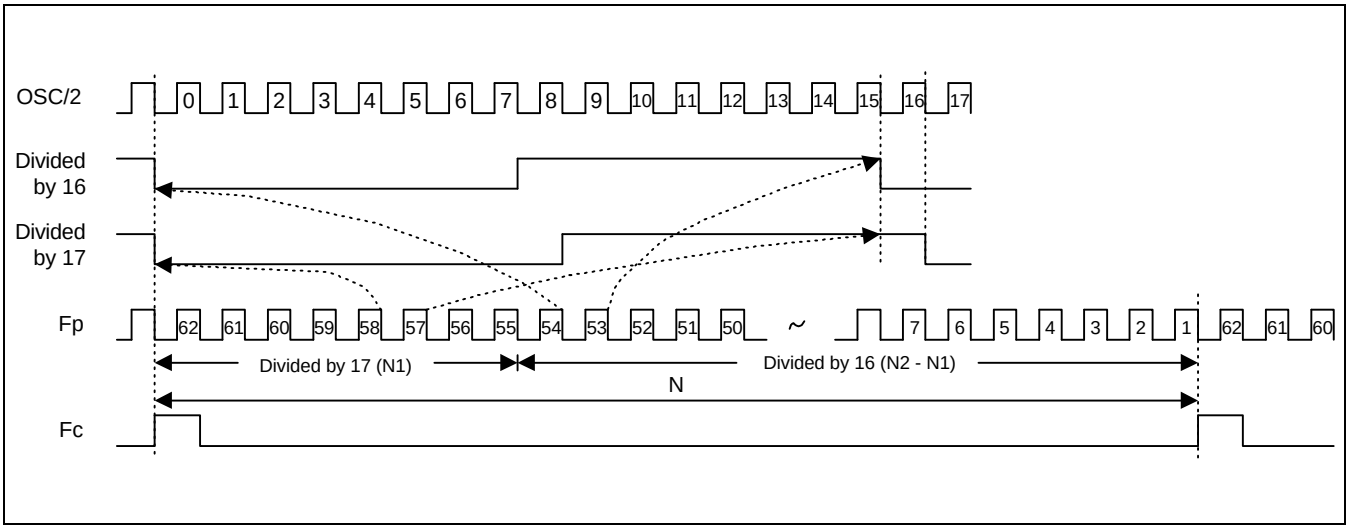


Figure 8. Generated FC by First Example

PHASE FREQUENCY DETECTOR

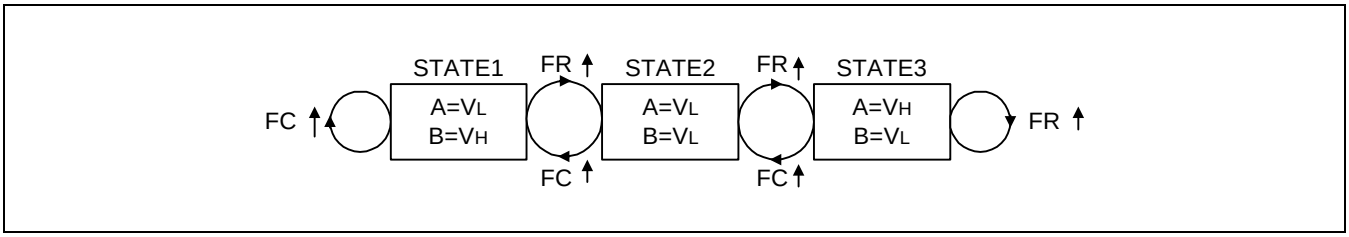


Figure 9. PFD state diagram

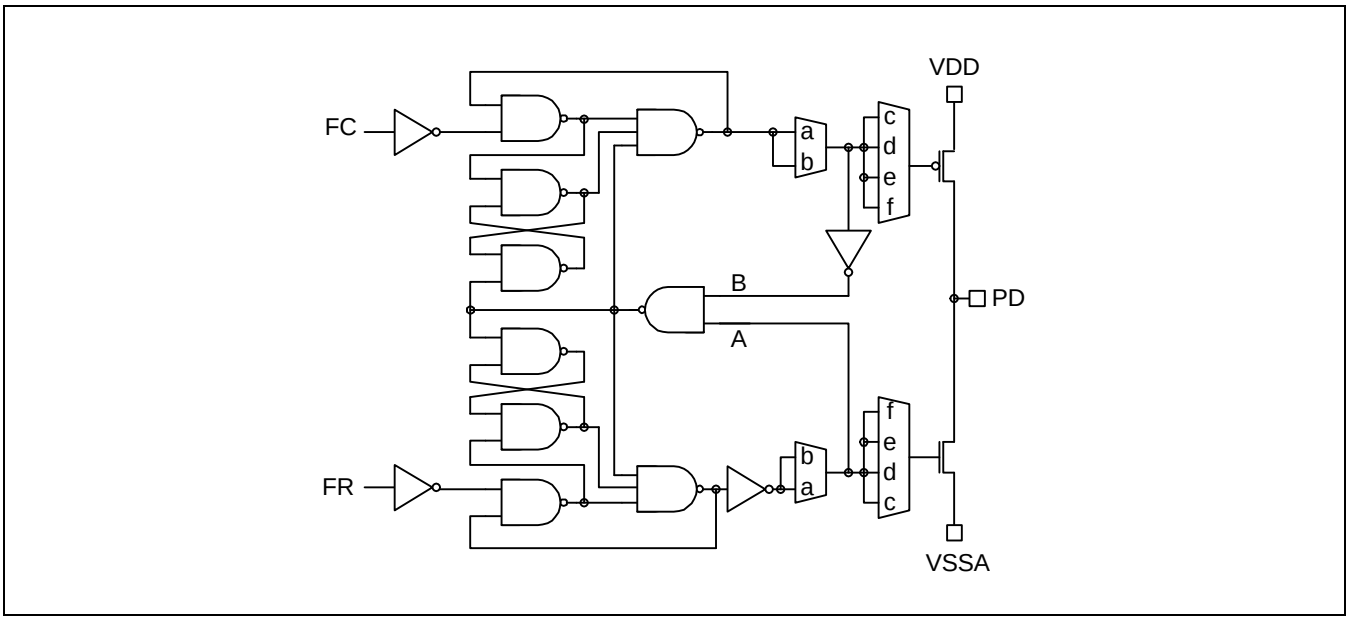


Figure 10. PFD scheme

States are changed on rising edges of Fr or Fc in Figure. 9(Fr moving to higher states and Fc moving to lower states) Suppose the circuit is initially in state 1, Then alternate rising edges on Fr and Fc will cycle between states 1 and 2. If Fc is constantly falling behind Fr in phase, as in the timing diagram(Figure. 11 A point), then eventually there will be two Fr rising edges without an intervening Fc rising edge. This will take the circuit to state 3, and thereafter it will cycle between state 2 and state3.

For phase difference of Fc and Fr is almost zero, the rising edges of Fr and Fc are coincident, and the PD remains in state 2 almost all the time

- Z-state Phase Frequency Detector is composed of 3-State PFD and two MOS gates
- State 1 : make the frequency of Fc slower.
- State 2 : hold the frequency of Fc.
- State 3 : make the frequency of Fc faster.
- State transition at rising edges of Fr and Fc
  - ♦ rising edge of Fr : cause current state to go high
  - ♦ rising edge of Fc : cause current state to go low

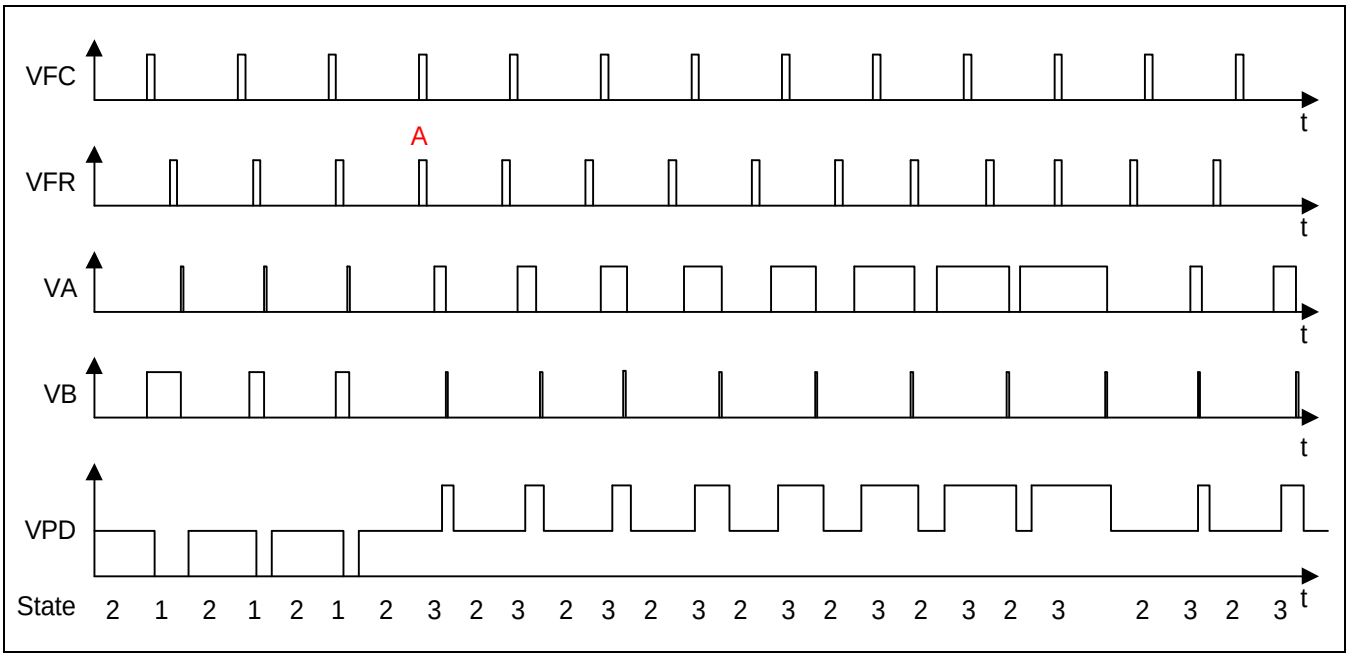


Figure 11. Timing Diagram (DZ[1:0]=0)

- differences of deadzone (in Figure. 10)

DZ[1]	DZ[0]	MX2 path	MX4 path	PMOS / NMOS	DeadZone	remarks
0	0	b	a	on/on	--0	(1)
0	1	a	b	on/on	-0	(2)
1	0	a	c	off/off	+0	(3)
1	1	a	d	off/off	++0	(4)

♦ DZ[1:0] = 0 mode : Even though PLL loop is locked, generate phase error pulse and phase error correction pulse which make Deadzone reduced.

♦ DZ[1:0] = 1 mode : Same as Dz[1:0] = 0 mode, but a width of phase error correction pulse is relatively narrower.

♦ DZ[1:0] = 2 mode : Generate only phase error pulse but phase error correction pulse.

♦ DZ[1:0] = 3 mode : Same as DZ[1:0] = 2 mode, but a width of phase error pulse is relatively narrower.

♦ DZ[1:0] = 0 or 1

— Excellent C/N characteristics

— Sidebands may be created by reference frequency leakage

— Sidebands may be created by low-frequency leakage due to the correction pulse envelope.

♦ DZ[1:0] = 2 or 3

— PLL loop stable

♣ **DEADZONE**

PFD has to detect subtle phase error and makes phase error signal. There is a region that PFD doesn't make any phase error pulse due to the propagation delay or other factors, which is called Deadzone.
(detailed in IX. Terminology)

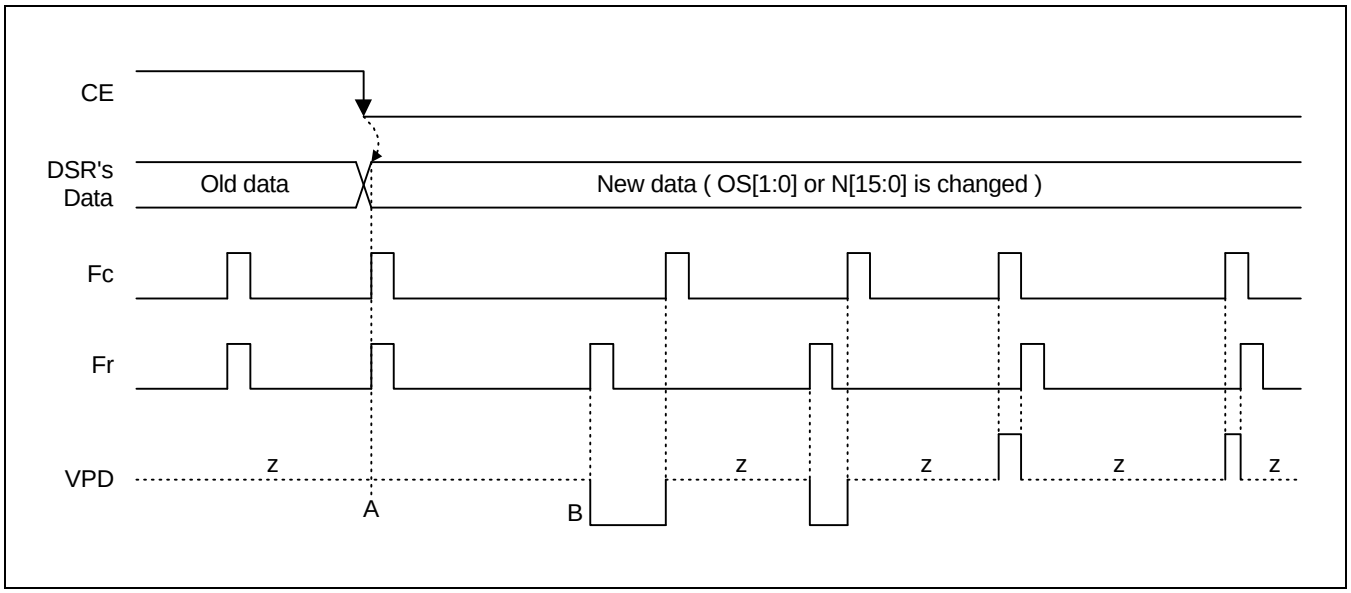


Figure 12. PFD and PD Output Relationship

- ψ Error pulse is made from rising edge of Fr and Fc.
- If rising edge of Fc is slower than that of Fr, set Vpd to low
  → make the frequency of Fc fast. (Figure. 9 state1)
- If rising edge of Fc is faster than that of Fr, set Vpd to high
  → make the frequency of Fc slow. (Figure. 9 state3)
- A region with no ψ Error makes Vpd high impedance and hold the frequency of Fc
- When data are changed in OS[1:0], N[15:0] or changed in R[3:0] from PLL stop mode.
  - ♦ reset Fc and Fr counter(Figure. 12 A) and change PFD in state 2
  - ♦ After new data is latched, accurate ψ Error can be reflected on the first phase error(Figure. 12 B)
  - ♦ Lock time can be estimated in advance depending on N[15:0] or OS[1:0] is changed

LOCKED STATE DETECTION TIMING

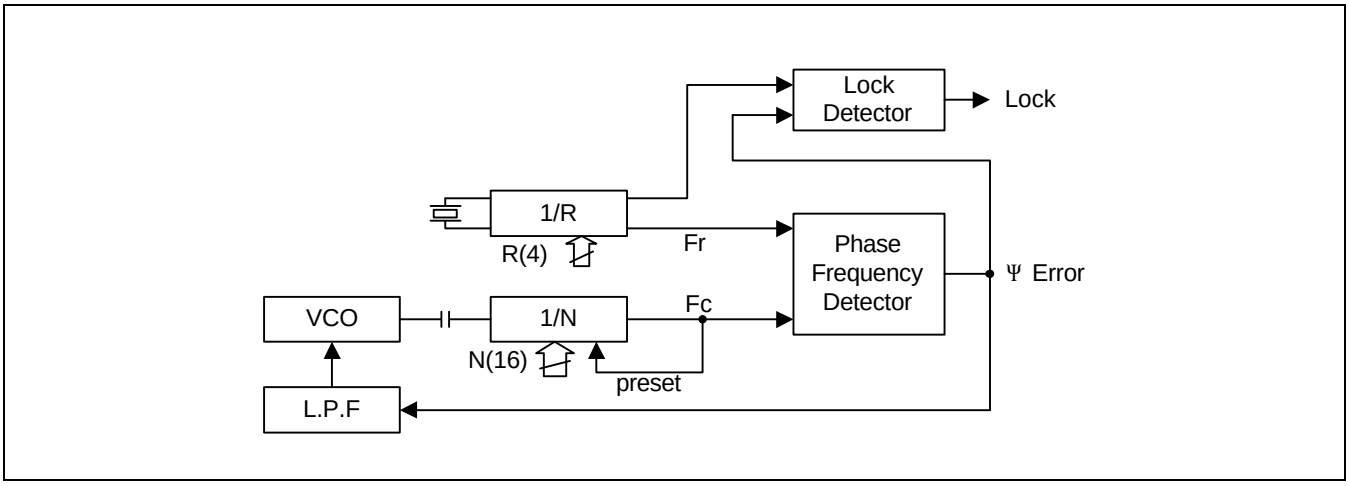


Figure 13. Lock Detection Scheme

- Getting LOCK State

UL[1:0]	LOCK state in serial data	LOCK state on DO pin	Remarks
0	hold the previous state		
1	ψ E is out directly depending on SIO timing	ψ E is out directly	
2	when ψ E is narrower than ψ E width more than 2ms, set LOCK		
3			

- LOCK bit in serial data reflects LOCK state regardless of DOC[1:0]
- DO pin reflects LOCK state only when DOC[1:0] is 2

  → LOCK : DO pin = open , UNLOCK : DO pin = low

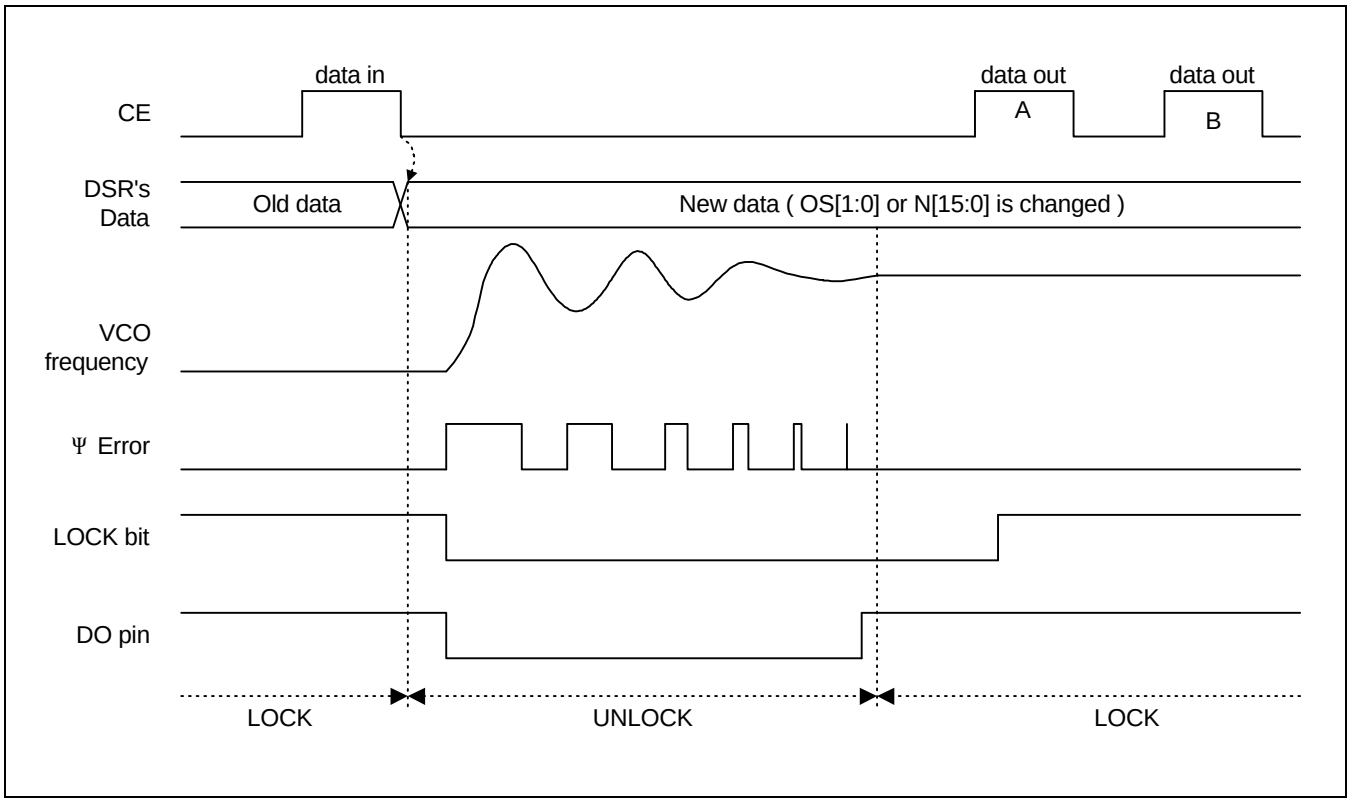


Figure 14. Lock detection timing diagram

- LOCK bit in serial data
  - ♦ LOCK bit in serial data shows UNLOCK because VCO frequency isn't stable (Figure. 14 A) → wait at least several cycle and check LOCK again(Figure. 14 B)
  - ♦ needs several LOCK check in order to get more reliable result.
- LOCK state on DO pin
  - ♦ Only when DOC[1:0]=1 and UL[1:0] ≠ 0, LOCK state can be checked on DO pin
  - ♦ needs several LOCK check in order to get more reliable result.

IF COUNTER

Count IF frequency during measurement time(GT[1:0]), start counting on IFCS setting high.

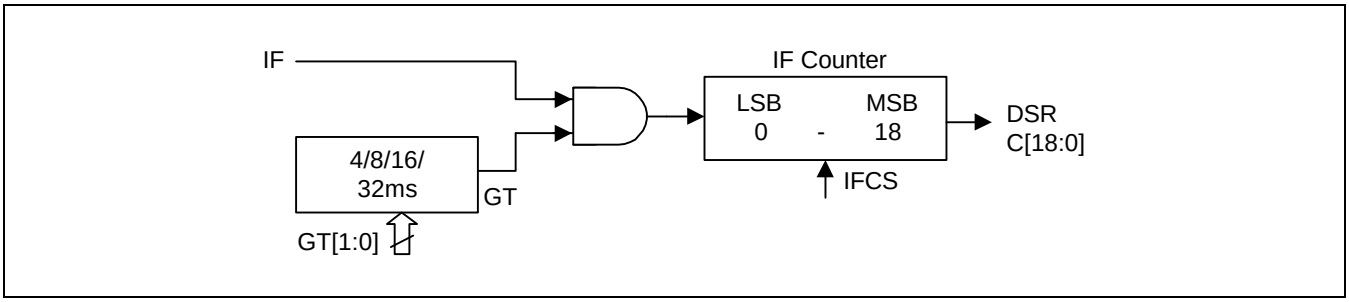


Figure 15. IF Counter Structure

- C[18:0] = $F_{IF} \times GT$: Counted value (the number of pulse)

GT1	GT0	Measurement time(GT)	GT1	GT0	Measurement time(GT)
0	0	4 ms	1	0	16 ms
0	1	8 ms	1	1	32 ms

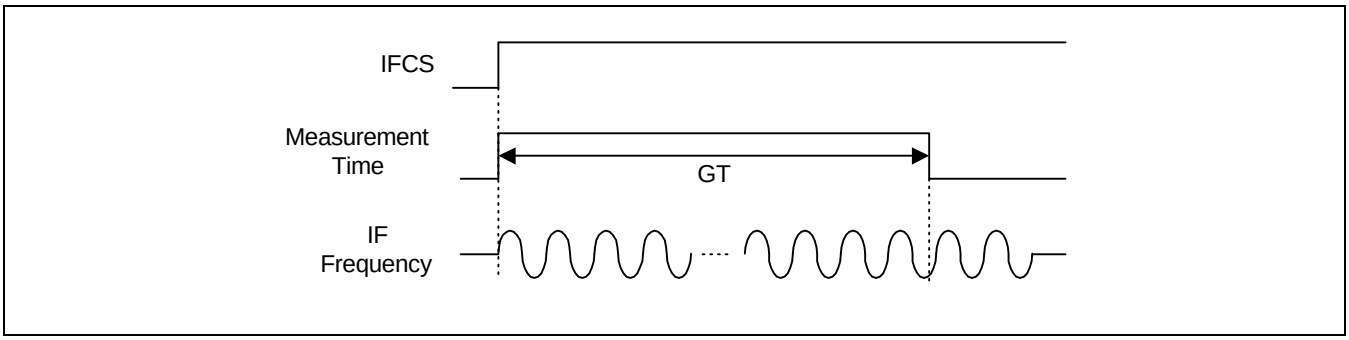


Figure 16. IF counter operation

- In Figure. 16
  - ♦ When IFCS bit is zero, IF counter is reset. On IFCS bit is turning to one, IF counter starts to count IF frequency during measurement time. Then IF counter holds the counted value. If DOC[1:0] is 3, inform the micro- processor of the end of counting by means of setting DO pin to be low.
  - ♦ IF counter is automatically reset after sending serial data to Micro- processor and ready to count.
  - ♦ If IF frequency less than 45kHz(FM : 1.07MHz) comes into IF counter during first 100us of measurement time(GT[1:0]), inform Micro-processor of the end of counting by means of setting DO pin to be low in the case that DOC[1:0] is 3, even though measurement time isn't passed .
  - ♦ After measurement time(GT[1:0]) is passed, IFCS bit has to be held 1. Unless IFCS bit is held to be one, counted IF value is all reset to be 0.
  - ♦ IFCS bit is automatically reset after Micro-processor reads the counted IF values.

MPX VCO FREE-RUNNING-FREQUENCY SELF-ADJUSTING CONTROLLER

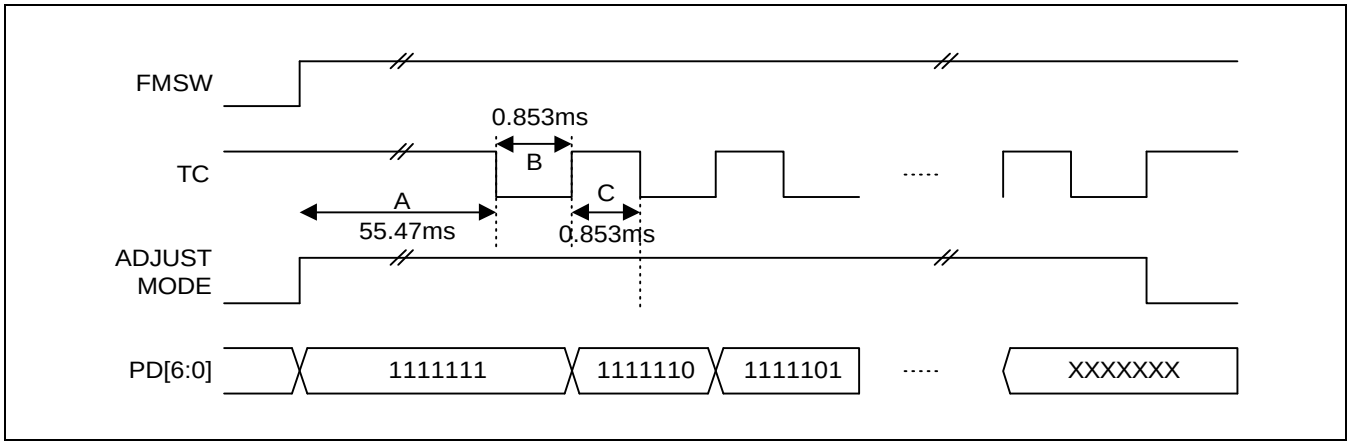


Figure 17. MPX VCO Free-Running Adjustment Timing Diagram

- Whenever band is switched to the FM mode, FM MPX VCO free-running frequency will be adjusted between 302.5kHz and 309.5kHz using control code PD[6:0]
- A region : wait time for MPX VCO to oscillate due to band switching.
- B region : measure MPX VCO free-running frequency and check whether free-running frequency is between 302.5kHz — 309.5kHz or not. If MPX VCO free-running frequency is between 302.5kHz — 309.5kHz, hold the control code and end the adjusting.
- C region : reduce control code PD[6:0] into 1 step, make free-running frequency fast. If PD[6:0] is 1111111(bin), VCO frequency will be minimum frequency and If PD[6:0] is 0000000(bin), VCO frequency will be maximum frequency.
- In adjusting MPX VCO free-running, MUTE will be set to one.
- The result of MPX VCO free-running adjust is out through TEST1 pin, when TEST[1:0] is zero.
  - ♦ TEST1 pin = 1 : operating VCO free-running adjustment
  - ♦ TEST1 pin = 0 : success adjusting VCO free-running between 302.5kHz — 309.5kHz
  - ♦ TEST1 pin = 1.172kHz/2 : 1.172kHz/2 frequency is out when first adjustment cycle (maximum adjustment time : 164.7ms / 1 cycle) is failed. Try to adjust VCO free-running on and on, TEST1 pin is set to be zero when VCO free-running frequency is between 302.5kHz — 309.5kHz

TEST FUNCTION

TEST[1:0]	TEST1 Pin		TEST2 Pin		TEST3 Pin	Remarks
	IN	OUT	IN	OUT	OUT	
0	-	ADJRESULT	-	-	-	(1)
1	-	TFCOUT	-	TFROUT	TMPXVCO	(2)
2	TIF	-	TLEDRSTB	-	TIFMINMAX	(2)
3	TFCIN	-	TFRIN	-	-	(2)

- ADJRESULT : out MPX VCO adjustment result
  - 1 : on adjusting
  - 0 : success in adjustment
  - 1.172kHz : 1st. adjustment cycle is failed, but adjusting 2nd, 3rd adjustment cycle.
- TFCOUT : Fc Frequency divided by N[16:0]
- TIF : IF frequency comes in through external source for test
- TFCIN : Fc frequency comes in through external source for test
- TLEDRSTB : counter reset signal of tuning LED control block comes in through external source for test
- TFRIN : Fr frequency comes in through external source for test
- TFROUT : Fr frequency divided by R[4:0]
- TMPXVCO : MPX VCO free-running frequency which is end of adjusting
- TIFMINMAX : Minimum and maximum of IF frequency which is used to check tuning LED operation
  - TEST[1:0]=0 :inform the state of MPX VCO free-running adjustment
  - TEST[1:0]=1 : Fc frequency for testing N divider block, Fr frequency for testing X'tal divider block, MPX VCO free-running frequency for testing MPX VCO self adjusting block
  - TEST[1:0]=2 : IF frequency, reset signal of LED control counter and IF Min. Max value for testing LED control block
  - TEST[1:0]=3 : Fc and Fr frequency for testing PFD and LOCK detector
  - (1) : If A[1:0] is zero, send the IN1 MODE data latched in DSR to Micro- processor through DO pin synchronized with falling edge of CL
  - (2) : If A[1:0] is zero, send the IN2 MODE data latched in DSR to Micro- processor through DO pin synchronized with falling edge of CL

CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit	Remarks
Supply Voltage	Vs	10	V	
Operating Temperature	Top	-20 — +75	°C	
Storage Temperature	Tstg	-55 — +150	°C	
Power Dissipation	Pdmax	1800	mW	

TEMPERATURE CHARACTERISTICS

Parameter	Symbol	Condition	Ratings	Unit	Remarks
Quiescent circuit current1(FM)	Δ Icc1	-20 — +75°C	20	uA/°C	
Quiescent circuit current2(AM)	Δ Icc2	-20 — +75°C	20	uA/°C	

ELECTRO_STATIC DISCHARGE CHARACTERISTICS

Parameter	Condition	Pin No.	Ratings	Unit	Remarks
Human Body Model	C = 100pF, R = 1.5kΩ	ALL PINS	± 2000	V	
Machine Model	C = 200pF, R = 0 kΩ	ALL PINS	± 200	V	
CDM	-	ALL PINS	± 500	V	

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, Vcc = 3V. unless otherwise specified)
FM F/E : f = 98MHZ, fm = 1kHz, Δf = 22.5kHz, AM : f = 1MHz, fm = 1kHz, 30% Mod
FM IF : f = 10.7MHZ, fm = 1kHz, Δf = 22.5kHz, MPX : f = 1kHz, L+R = 90%, P = 10%, Vi = 150mV)

Parameter		Symbol	Condition	Ratings			Unit
				Min.	Typ.	Max.	
Supply Voltage Range		Vcc		2.0	-	7.0	V
Supply Current		Iccq1	FM, Vi = 0	6	13	18	mA
		Iccq2	AM, Vi = 0	2.5	5	8	mA
F/E	Input Limiting Voltage	Vi lim1	Vo = -3dB	-	12	18	dBu
	Local Oscillation Voltage	Vosc	fosc = 108.7MHz	40	70	110	mV
FM IF	Input Limiting Voltage	Vi lim2	Vo = -3dB	30	36	42	dBu
	Detection Output Voltage	Vo det1	Vi = 80dBu	60	80	110	mV
	S/N Ratio	S/N1	Vi = 80dBu	55	65	-	dB
	AM Depression Ratio	AMR	Vi = 80dBu	40	50	-	dB
	THD	THD1	Vi = 80dBu	-	0.2	1.0	%
	LED Turning On sensitivity	VI11	IFS[1:0] = 0	40	45	50	dBμ
		VI12	IFS[1:0] = 1	46	51	56	dBμ
		VI13	IFS[1:0] = 2	52	57	62	dBμ
		VI14	IFS[1:0] = 3	58	63	68	dBμ
AM RF	Voltage Gain	Gv1	Vi = 26dBu	30	55	-	mV
	Detection Output Voltage	Vo det2	Vi = 60dBu	60	85	110	mV
	LED Turning On	VI21	IFS[1:0] = 0	22	27	32	dBμ
		VI22	IFS[1:0] = 1	28	33	38	dBμ
		VI23	IFS[1:0] = 2	32	37	42	dBμ
		VI24	IFS[1:0] = 3	36	41	46	dBμ
AM IF	S/N Ratio	S/N2	Vi = 60dBu	32	42	-	dB
	THD	THD2	Vi = 60dBu	-	1	2	%

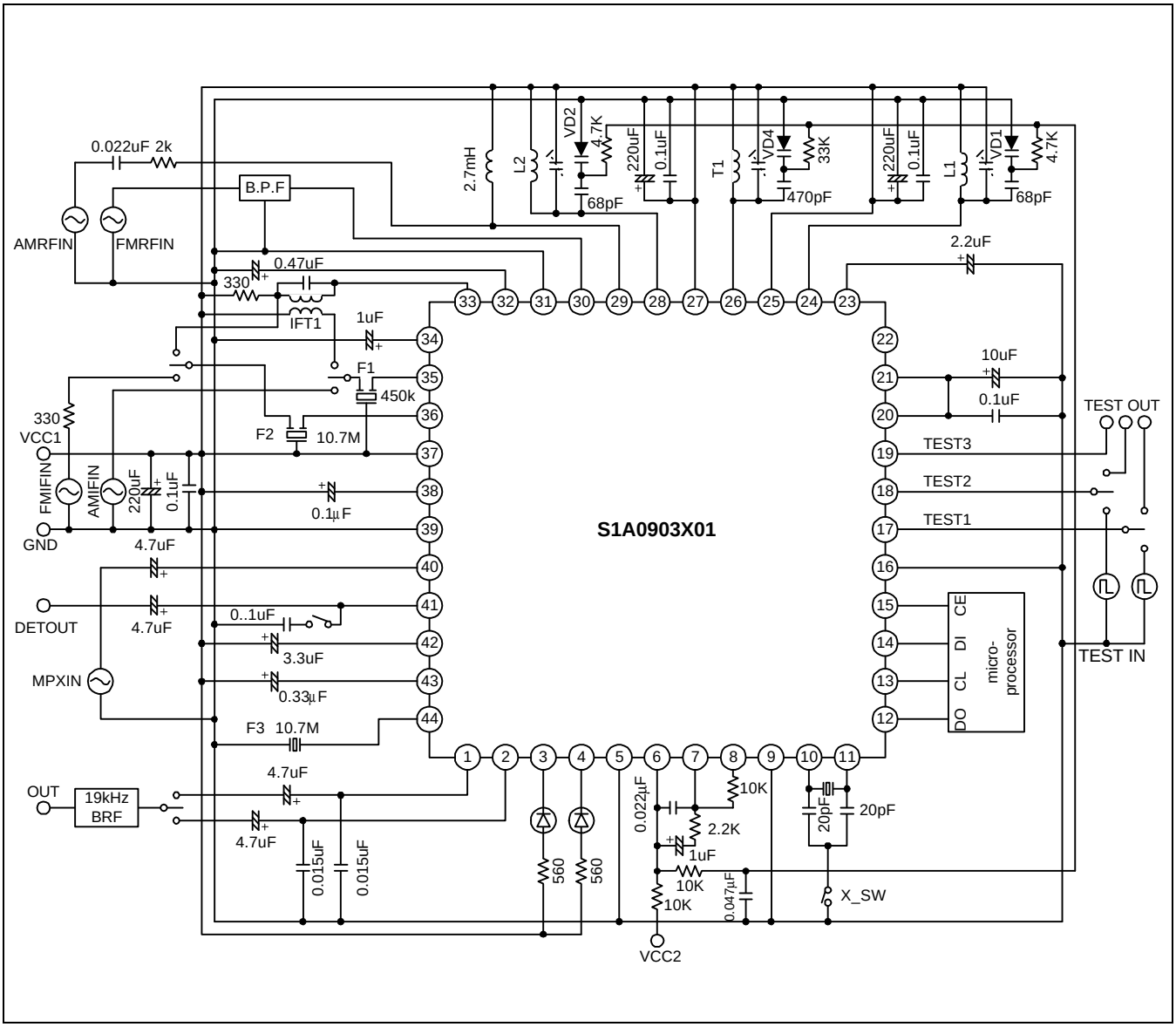
ELECTRICAL CHARACTERISTICS (Continued)

(Ta = 25°C, Vcc = 3V. unless otherwise specified)
FM F/E : f = 98MHZ, fm = 1kHz, Δf = 22.5kHz, AM : f = 1MHz, fm = 1kHz, 30% Mod
FM IF : f = 10.7MHZ, fm = 1kHz, Δf = 22.5kHz, MPX : f = 1kHz, L+R = 90%, P = 10%, Vi = 150mV)

Parameter			Symbol	Condition	Ratings			Unit
					Min.	Typ.	Max.	
MPX	Maximum Input Voltage		Vimax	Stereo, THD = 3%	300	450	-	mV
	Voltage Gain		Gv2		-5	-1	0.5	dB
	Channel Balance		CB	Mono	-1.5	0	1.5	dB
	THD1		THD3	Mono	-	0.2	1.0	%
	THD2		THD4	Stereo	-	0.2	1.0	%
	Separation 1		CS1	Stereo, f=100Hz	25	35	-	dB
	Separation 2		CS2	Stereo, f=1kHz	25	35	-	dB
	Separation 3		CS3	Stereo, f=10kHz	25	35	-	dB
	LED Turning On Sensitivity		Vlon	TUNLED=ON, Pilot only	-	8	16	mV
	LED Turning Off Sensitivity		Vloff	TUNLED = OFF, Pilot only	1	6	-	mV
	Lamp Hysteresis		HY		-	2	-	mV
	Capture Range		CR	Pilot only	-	4	-	%
	S/N Ratio		S/N3	Mono	60	70	-	dB
	Mute Attenuation		Amute		65	75	-	dB
DTS	Input Voltage	High Level	Vih	CE, DI, CL	0.7Vreg	-	-	V
		Low Level	Vil	CE, DI, CL	0	-	0.3Vreg	V
	Output Voltage	High Level	Voh1	PD : Io=-1mA	0.7Vreg	-	-	V
		Low Level	Vol1	PD : Io=1mA	-	-	0.3Vreg	V
			Vol2	DO : Io=5mA	0	-	0.3Vreg	V
	Output Voltage Range		Vo	Aout	0	-	9	V
	Internal Feedback Registance		Rf	XIN	-	0.4	-	MΩ
	Input Current		Iin1	CE, DI, CL=VDD or GND	-	-	5	μA
			Iin2	XIN=VDD or GND	1.3	-	8	μA
	Supply Current		Idd1	X'tal=10.8MHz, FM=130MHz	-	2.5	6	mA
			Idd2	PLL stop mode, X'tal=10.8MHz	-	0.3	-	mA
			Idd3	PLL stop mode, X'tal stop mode	-	-	10	μA

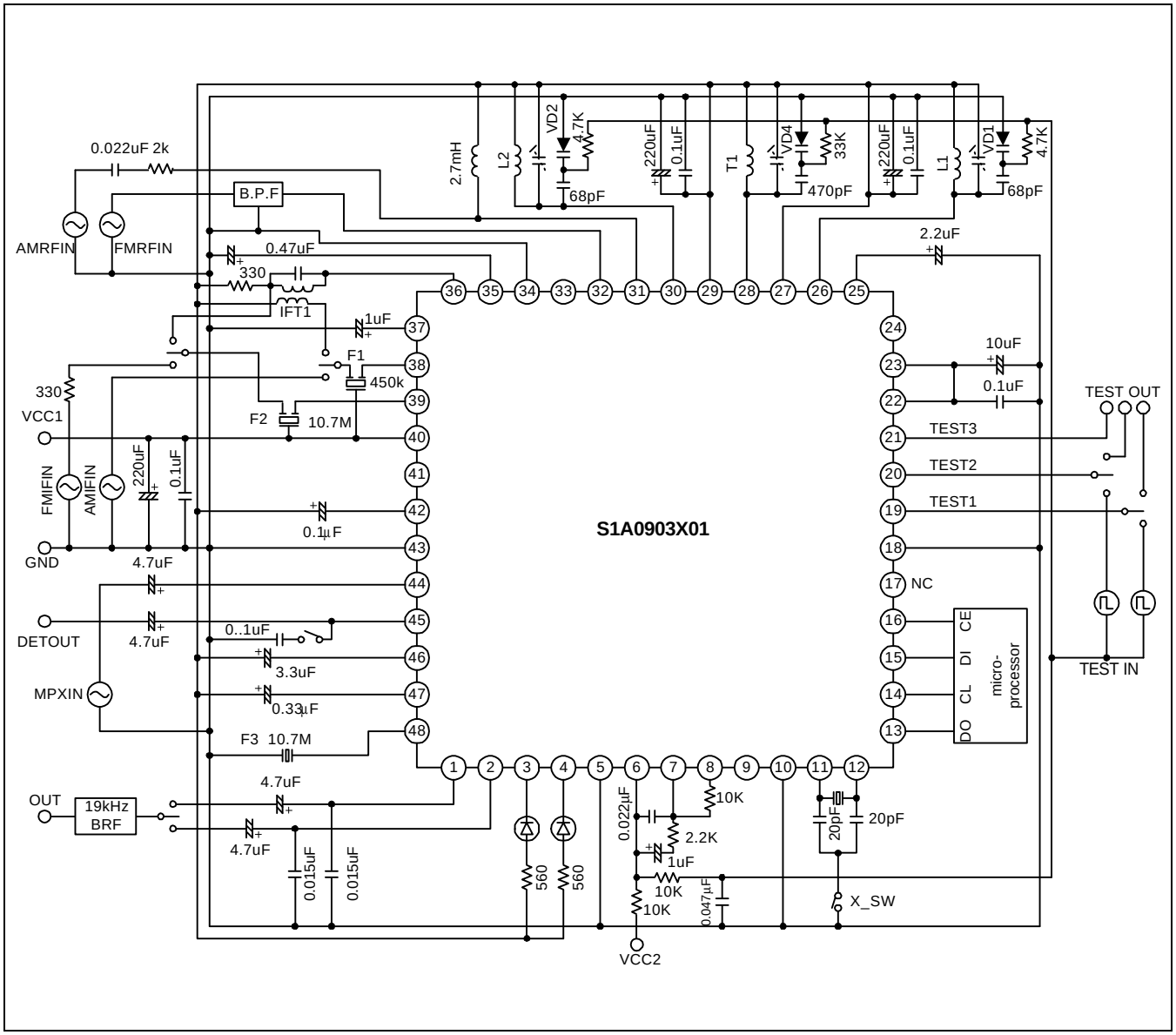
TEST CIRCUIT

44-QFP



TEST CIRCUIT

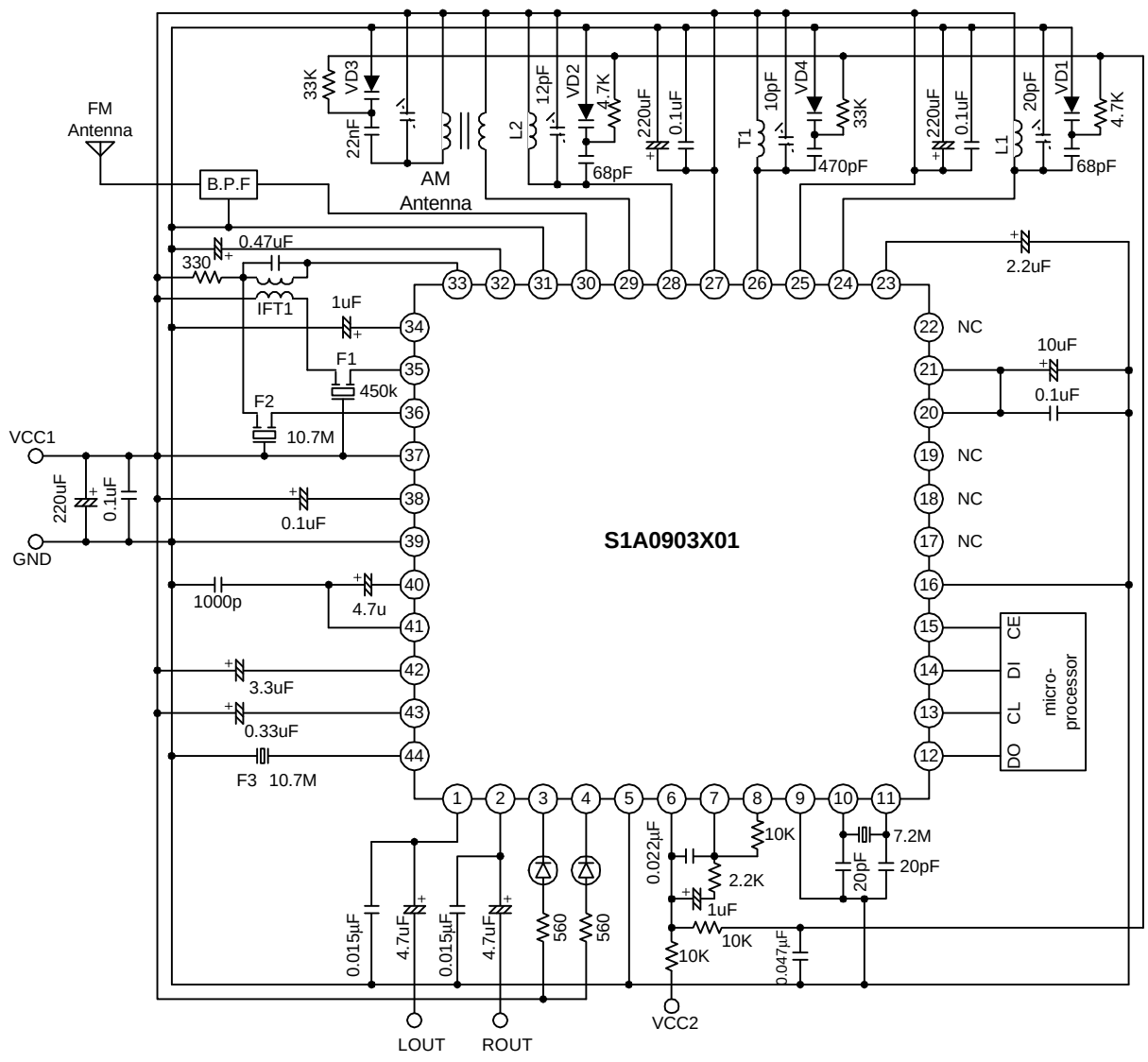
48-LQFP



SAMSUNG ELECTRONICS

APPLICATION CIRCUIT

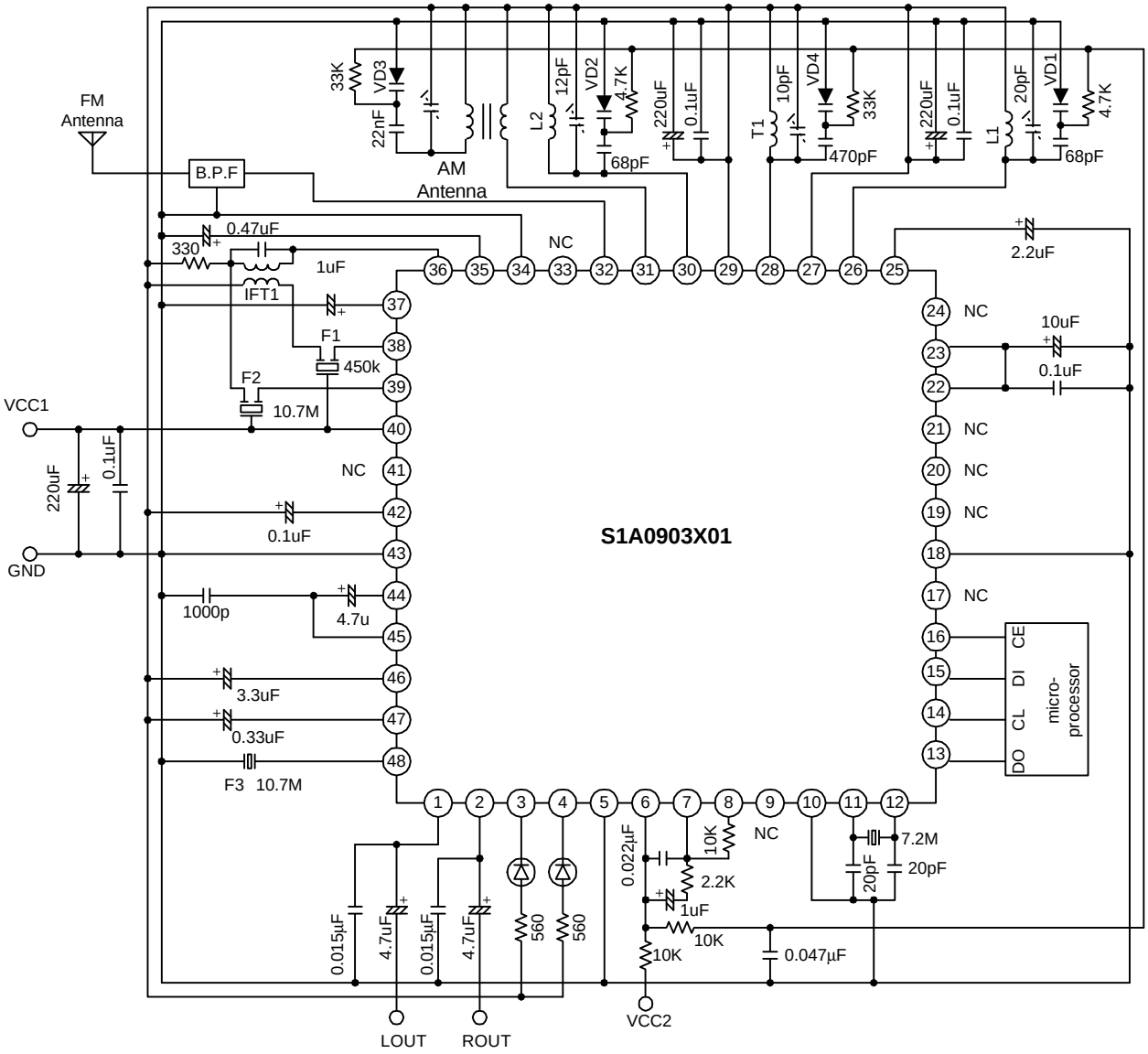
44-QFP



B.P.F : GFMG7 (KOREA SANGSHIN ELECTRIC Co.Ltd)
F1 (450kHz) : 450 BL(Toko co.Ltd)
F2 (10.7MHz) : SFE 10.7MA5 (MURATA Co.Ltd)
F3 (10.7MHz) : CDALA10M7GA115A-B0 (MURATA Co.Ltd)
VD1, VD2 : KV1471 (Toko co.Ltd)
VD3, VD4 : KV1236 (Toko co.Ltd)

APPLICATION CIRCUIT

48-LQFP



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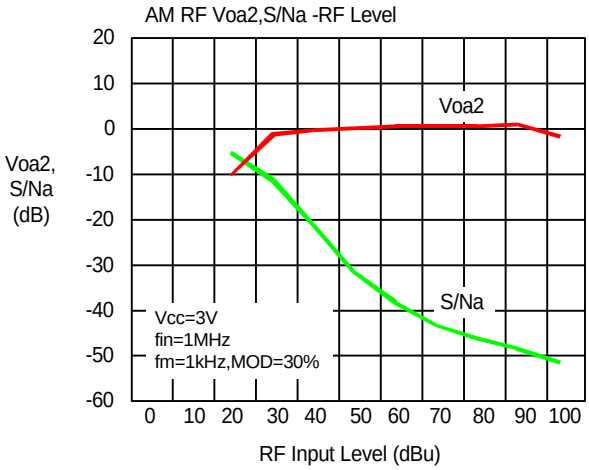
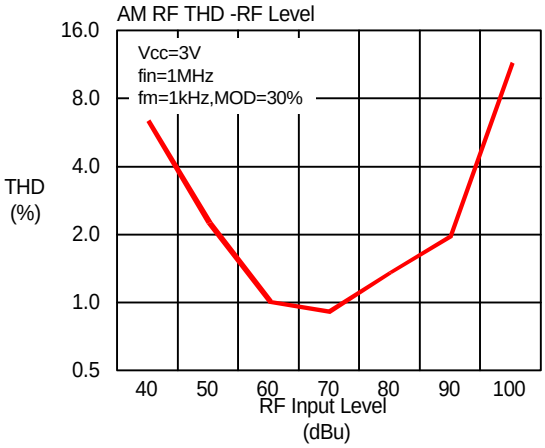
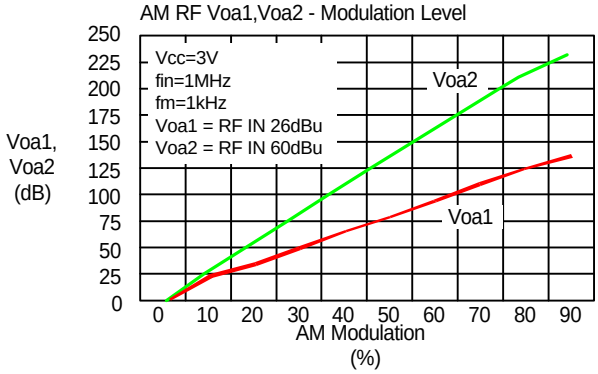
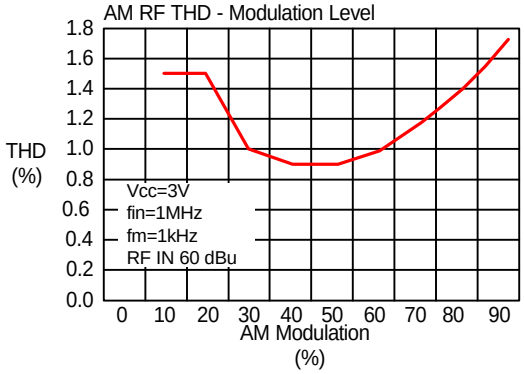
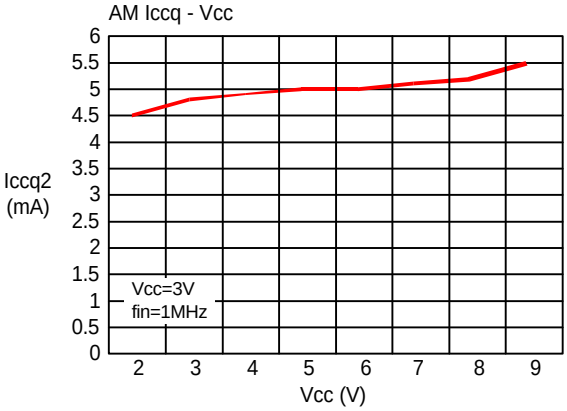
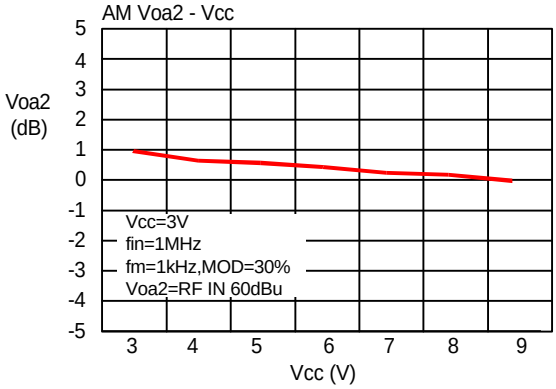

AM RF Voa2,S/Na -RF Level
Voa2, S/Na (dB)
20
10
0
-10
-20
-30
-40
-50
-60
Voa2
S/Na
Vcc=3V
fin=1MHz
fm=1kHz,MOD=30%
0 10 20 30 40 50 60 70 80 90 100
RF Input Level (dBu)

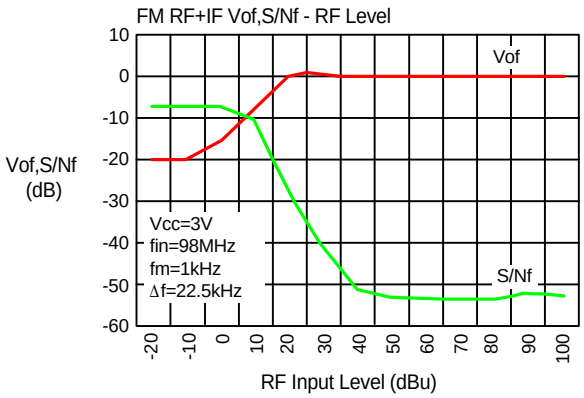

AM RF THD -RF Level
THD (%)
16.0
8.0
4.0
2.0
1.0
0.5
Vcc=3V
fin=1MHz
fm=1kHz,MOD=30%
40 50 60 70 80 90 100
RF Input Level (dBu)

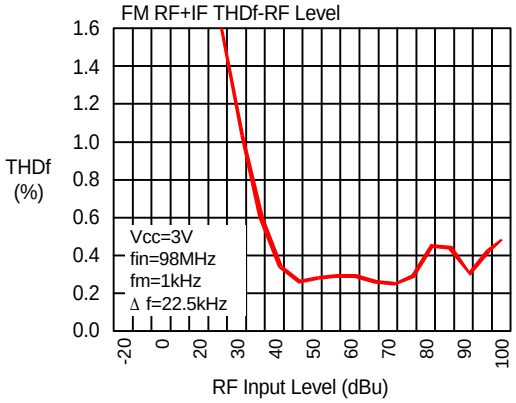

AM RF Voa1,Voa2 - Modulation Level
Voa1, Voa2 (dB)
250
225
200
175
150
125
100
75
50
25
0
Vcc=3V
fin=1MHz
fm=1kHz
Voa1 = RF IN 26dBu
Voa2 = RF IN 60dBu
Voa2
Voa1
0 10 20 30 40 50 60 70 80 90
AM Modulation (%)

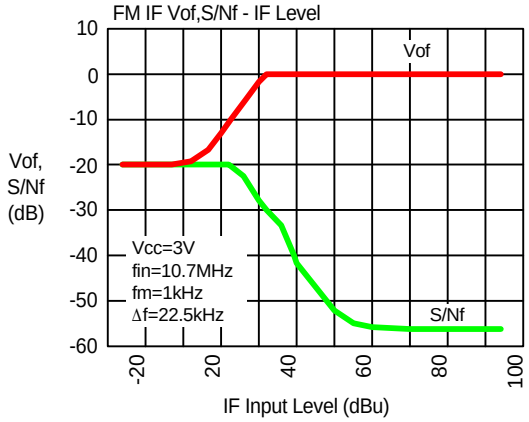

AM RF THD - Modulation Level
THD (%)
1.8
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
Vcc=3V
fin=1MHz
fm=1kHz
RF IN 60 dBu
0 10 20 30 40 50 60 70 80 90
AM Modulation (%)

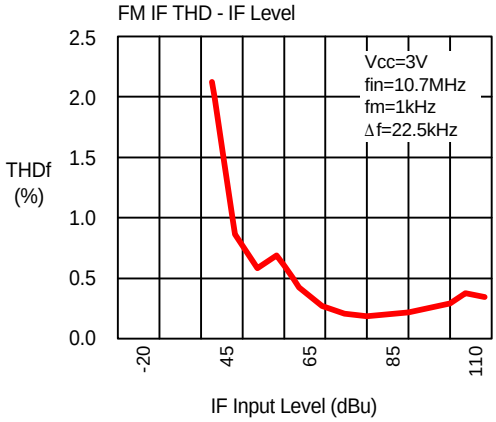

AM Iccq - Vcc
Iccq2 (mA)
6
5.5
5
4.5
4
3.5
3
2.5
2
1.5
1
0.5
0
Vcc=3V
fin=1MHz
2 3 4 5 6 7 8 9
Vcc (V)

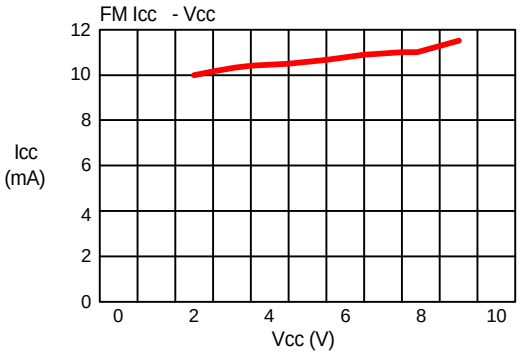

AM Voa2 - Vcc
Voa2 (dB)
5
4
3
2
1
0
-1
-2
-3
-4
-5
Vcc=3V
fin=1MHz
fm=1kHz,MOD=30%
Voa2=RF IN 60dBu
3 4 5 6 7 8 9
Vcc (V)





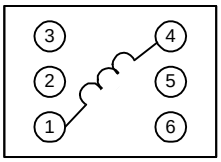






SAMSUNG ELECTRONICS

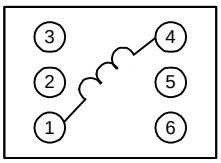
FM RF



SP-2065

f (MHz)	Qo	TURNS		KWANG SUNG PART NO
		1-4	WIRE	
100	80	7*(1/2)	0.45m/m	SP-2065

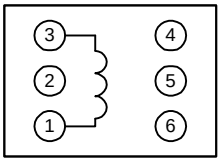
FM OSC



SP-2066

f (MHz)	Qo	TURNS		KWANG SUNG PART NO
		1-4	WIRE	
100	80	6*(1/2)	0.45m/m	SP-2066

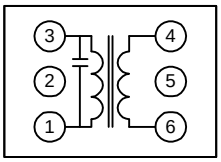
AM OSC



KS50N-354

f (MHz)	Qo	TURNS		L (uH)	KWANG SUNG PART NO
		1-3	WIRE		
796	50	84		110	KS50N-354

AM IFT (MIX OUT)

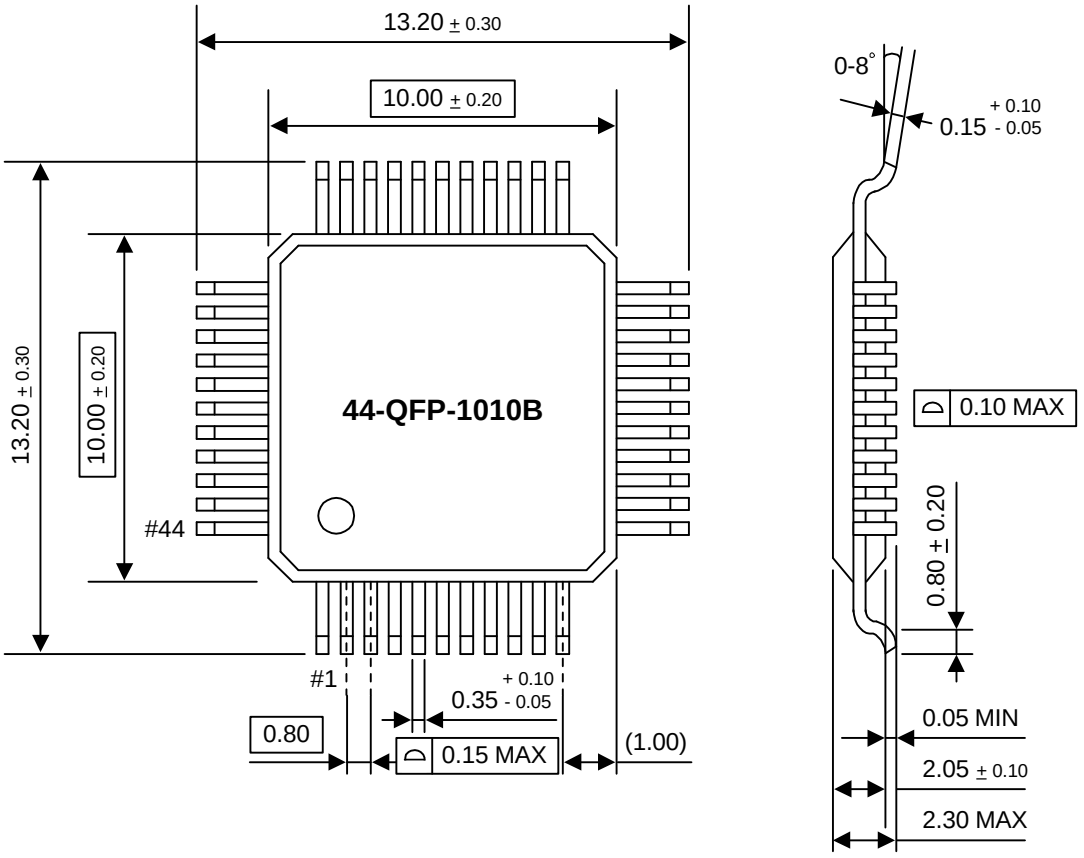


KS50-SAA

Co (pF)	f (MHz)	Qo	TURNS		KWANG SUNG PART NO
1-3			1-3	4-6	
470	455	40	115	5	KS50N-SAA

PACKAGE DIMENSIONS

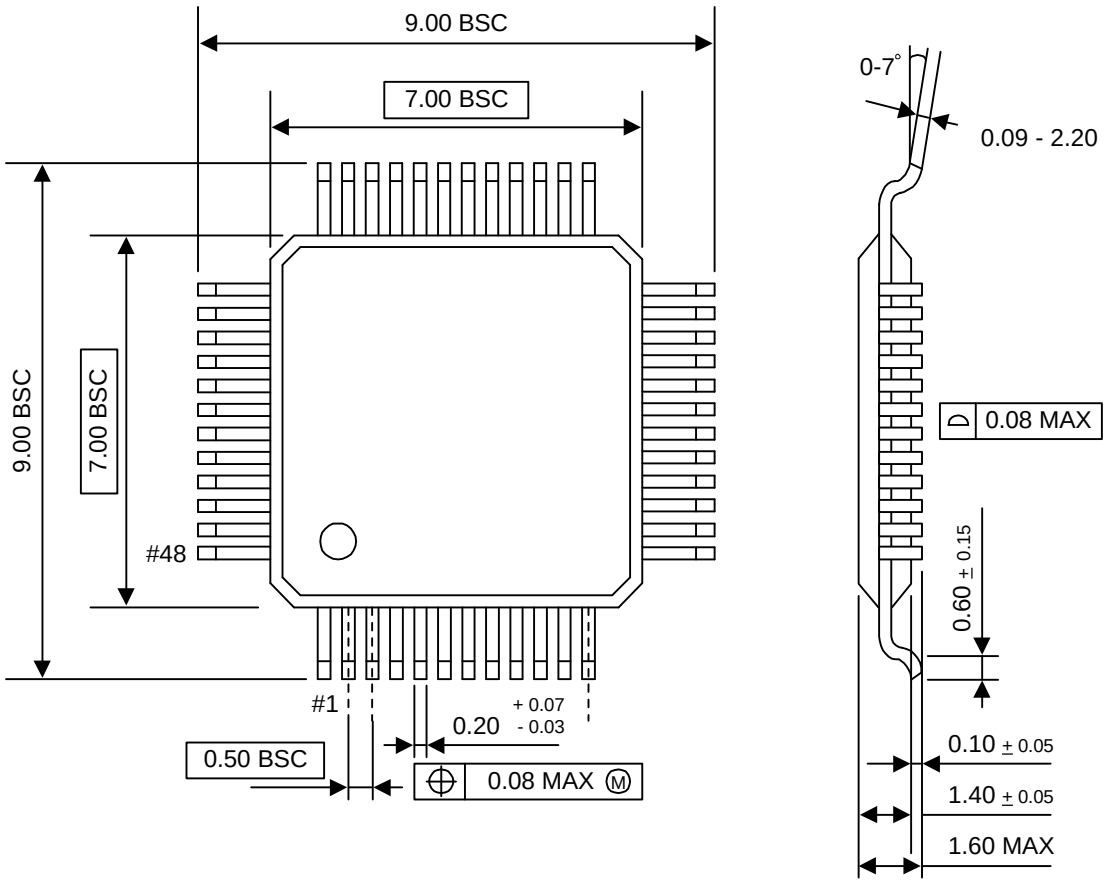
44-QFP



NOTE: Dimensions are in millimeters.

PACKAGE DIMENSIONS

48-LQFP



NOTE: Dimensions are in millimeters.

TERMONOLOGY

♣ DeadZone

PFD has to detect subtle phase error and makes phase error signal. There is a region that PFD doesn't make any phase error pulse due to the propagation delay or other factors, which is called Deadzone.
Performance of PLL frequency synthesizer depends on the width of DeadZone
The characteristic of PFD is not ideal A(Figure. 18) but curved B(Fig. 18) because PLL frequency synthesizer operates on reference signal just like a LPF(low pass filter)
The cause of Deadzone is that PFD doesn't generate phase error signal even though there is a phase error between reference frequency and VCO divided by N. In general deadzone has several nano seconds width.
To implement a high S/N ratio system, the width of Deadzone is as narrow as possible. But, RF leakage in MIXER block comes into VCO, which causes be a noise.

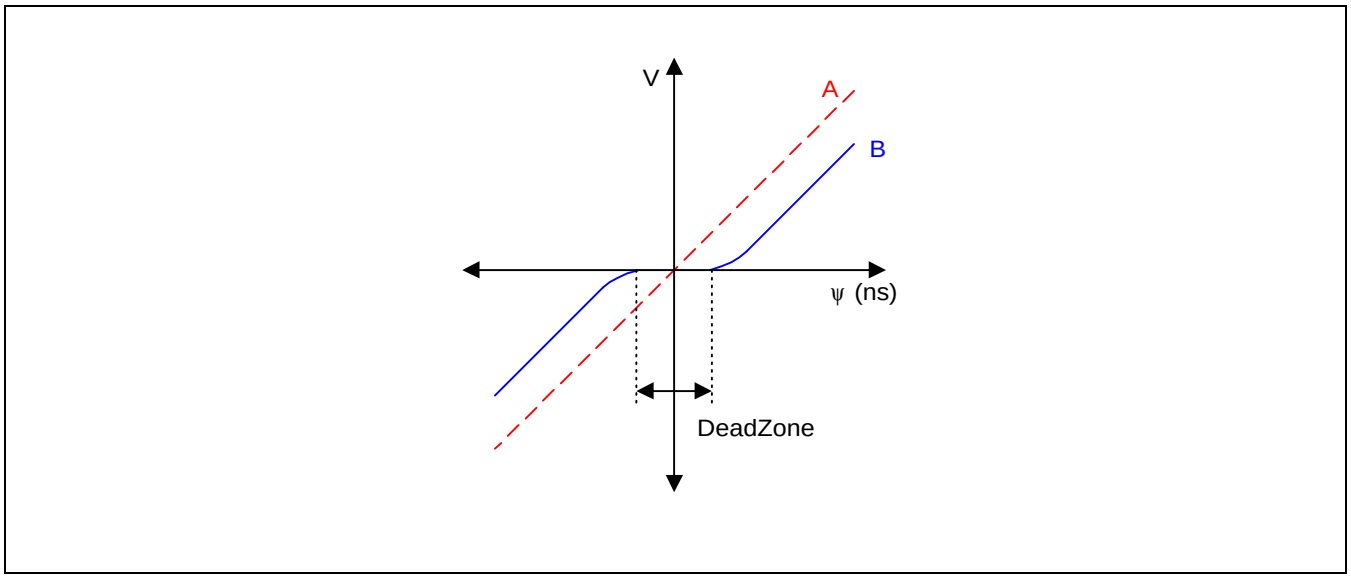


Figure 18. PFD Characteristic

♣ Application Note

1. Recommend using filter with 330Ω I/O impedance as 10.7MHz IF filter

2. Output gain of RF mixer is fixed by both of 330Ω register on PIN33 and parallel register of input impedance on 10.7MHz IF filter. Thereafter to control output gain of mixer depends on changing load register on PIN 34, which case both of input impedance of IF filter and load register are recommended to have same impedance.

3. Application of a input pin CE, DI, CL depends on the output of Micro-processor(Figure. 19). Input pin of CE, CL, DI must be set to be VDD using R1 and R2 In the case of Figure.19 <B>.

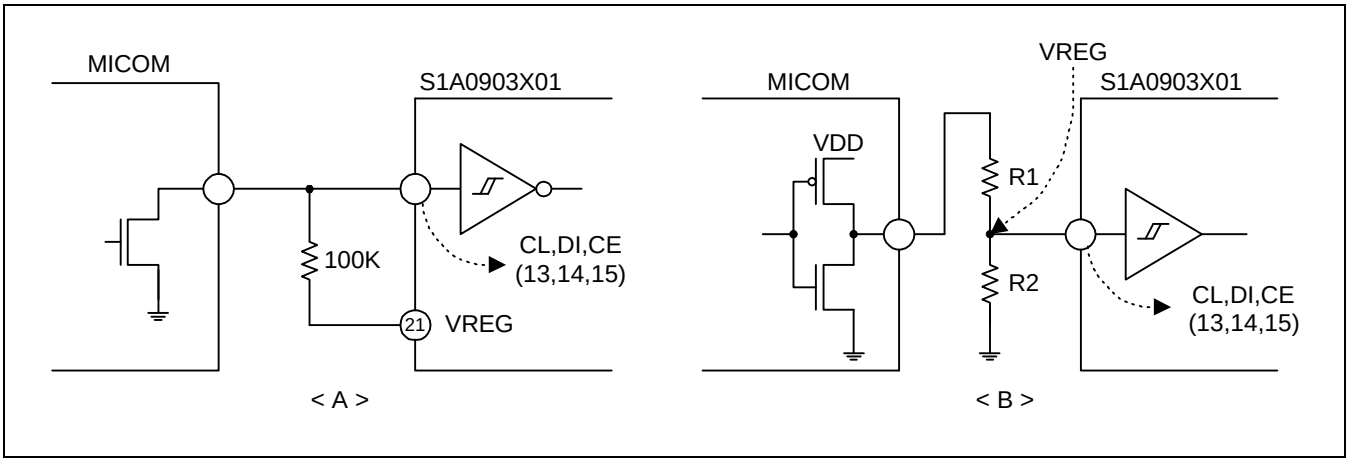


Figure 19. Connection between SIO and Microprocessor

4. Crystal can be selectable among 75kHz, 3.6MHz, 7.2MHz, 10.8MHz. The connection must be the same as Figure. 20 to share crystal for Micro-processor

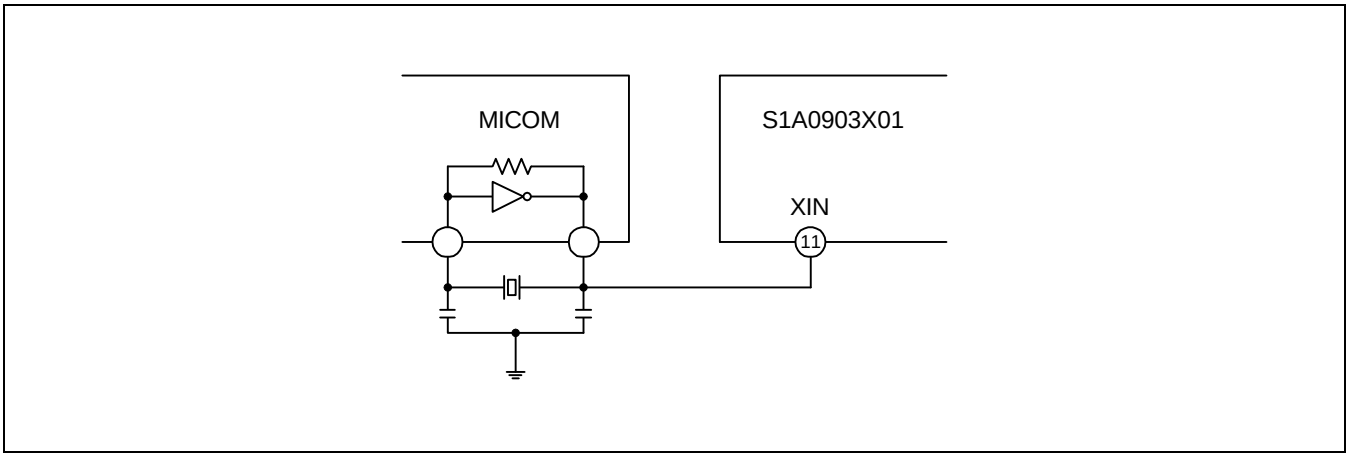


Figure 20. Connection X'tal for Micro-processor

NOTES