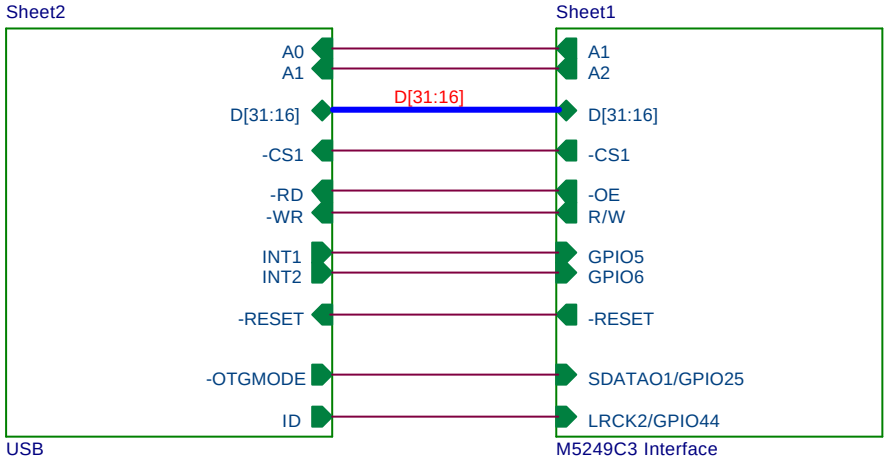
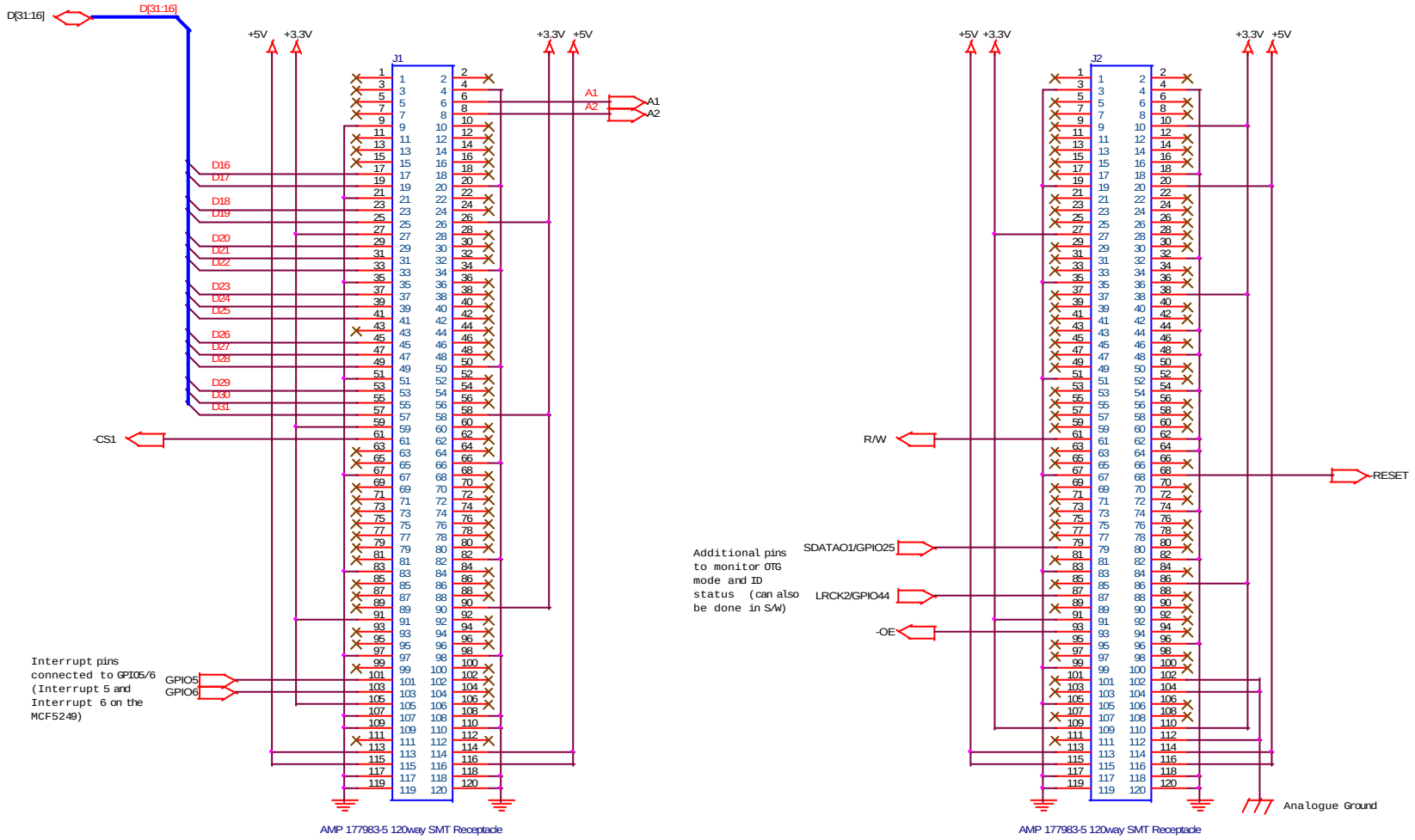
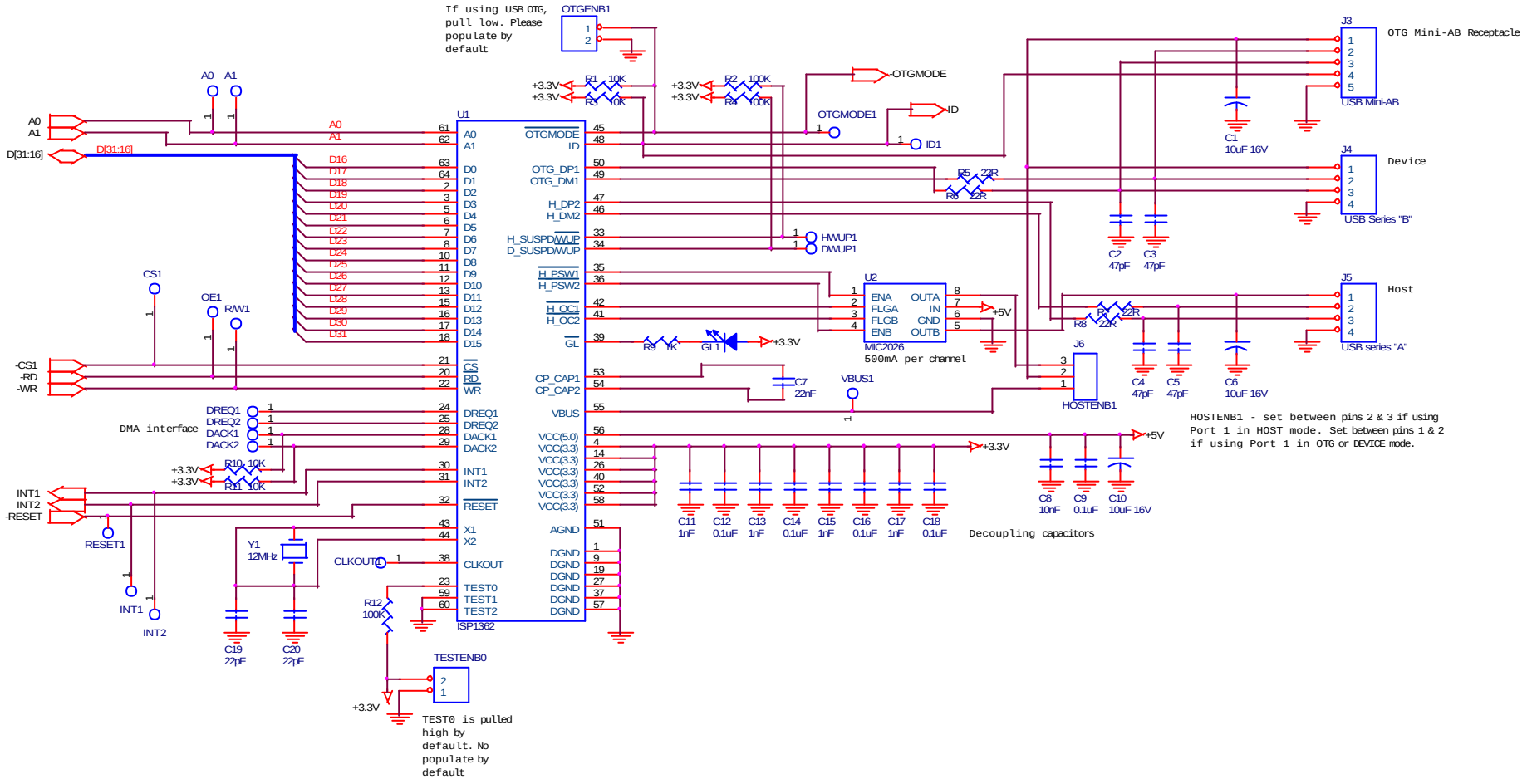


Title	MCF5249 EVB - USB daughter card	
Size A	Document Number Hierarchical Block Diagram	Rev 1.0
Date: Tuesday, October 07, 2003	Sheet 1 of 3	



Title	MCF5249 EVB - USB Daughter Card	
Size: B	Document Number: M5249C3 Expansion Connectors	Rev: 1.0
Date: Tuesday, October 14, 2003	Sheet 2 of 3	



Title	MCF5249 EVB - USB Daughter Card	
Size: B	Document Number: USB Controller	Rev: 1.0
Date: Monday, March 01, 2004	Sheet 3 of 3	

The schematics for the MCF5249 USB OTG reference design have been generated using Cadence Orcad Capture, release 9.2. This document outlines the schematic design hierarchy and explains, in some detail, the main design features.

1 Schematic Design Overview

The USB OTG reference design is divided into three schematic pages using a simple hierarchical structure. The pages are as follows:

Sheet 1	USB OTG Reference Design
Sheet 2	M5249C3 Expansion Connectors
Sheet 3	USB OTG Controller

2 Schematic Details

2.1 USB OTG Reference Design

This is the top level schematic detailing the connections between the two pages of the design.

2.2 M5249C3 Expansion Connectors

The 120-way AMP connectors are the mating connectors to the AMP expansion connectors on the M5249C3 evaluation board. Only the signals required for the USB interface are brought out onto the daughter card. In addition to that, the bus interface, the external interrupts, and power and ground are brought out as well.

2.3 USB OTG Controller

This schematic page includes the Philips™ ISP1362 USB OTG controller and a Micrel dual-channel power distribution switch for circuit protection.

2.3.1 Bus Operation

The ISP1362 is interfaced to the MCF5249 via the external bus interface. The external bus interface pins are utilized as follows:

- A0 determines whether the controller is to be in the command or data phase.
- A1 determines, on a per-access basis, whether the controller is to operate in host or device mode:
  - 0 Host control (HC) is selected
  - 1 Device control (DC) is selected
- $\overline{CS1}$ enables the HC/DC driver to access the buffer memory and registers of the HC/DC.
- $\overline{RD}$, when asserted low, indicates that the HC/DC driver is requesting a read to the buffer memory and registers of the HC/DC.
- $\overline{WR}$, when asserted low, indicates that the HC/DC driver is requesting a write to the buffer memory and registers of the HC/DC.
- D[31:16] connects the external 16-bit data bus to the internal registers and buffer memory of the ISP1362.

2.3.2 Interrupts

int1 and int2 are connected to gpio[5:6] on the MCF5249. Pins gpio[5:6] on the MCF5249 have the primary function of int[5:6] such that ISRs (Interrupt Service Routines) can be written to service the ISP1362.

2.3.3 Reset

The USB controller will be reset when the processor is reset using the $\overline{\text{RESET}}$ signal from the M5249C3 board. The reset time required for the ISP1362 is 10ms. The reset signal from U9 (MAX6355LSUT-T) on the M5249C3 is held active for 100ms, well within the 10ms requirement for the USB controller.

2.3.4 Clock

A 12-MHz crystal oscillator will be used to clock the ISP1362. This is connected to pins X1 and X2 of the ISP1362.

2.3.5 Mode of Operation

The ISP1362 has been interfaced to the MCF5249 in the PIO mode, therefore the DREQ and DACK pins are not required and have been set to the default values when not in use.

2.3.6 TEST Pins

These have been set to the default values in the data sheet for normal USB operation. TEST0 can be pulled high or low via jumper TESTENB0.

2.3.7 $\overline{\text{OTGMODE}}$ and ID Pins

Port 1 of the ISP1362 can be configured to operate in either OTG or device mode in this design. (host mode can also be implemented by the addition of a USB series “B” receptacle connected to Port 1; this isn’t included in this design as we are using port 2 configured for host operation therefore there is no requirement to configure Port 1 for host operation).

If port 1 is used in OTG mode then the $\overline{\text{OTGMODE}}$ pin needs to be pulled low. ID is pulled high by default, and is in use when an OTG device is connected to the Mini-AB receptacle so that a signal can be detected on the ID pin. The ID pin determines whether the OTG peripheral attached is operating in host or device mode.

If port 1 is to be used in device mode then $\overline{\text{OTGMODE}}$ is pulled high and the ID pin is not in use.

A logic table detailing the operation of Port 1 and the required signal levels of $\overline{\text{OTGMODE}}$ and ID can be found in the ISP1362 data sheet.

2.3.8 Standard USB Signals

OTG_DP1, OTG_DM1, H_DP2, H_DM2 are the standard differential transmission pairs for transmitting or receiving USB data.

OTG_DP1 and OTG_DM1 are connected to both the Mini-AB and USB series “B” receptacles for operation in both OTG and device modes.

NOTE

Only the Mini-AB (OTG) or the USB series "B" (device) receptacle will be in use at any one time. Only one USB connection (host, device, or OTG) can be used at a time. This device does not allow the user to connect an OTG and a device at the same time.

H_DP2 and H_DM2 are connected to a USB series "A" receptacle for operation in host mode.

Each USB device must specify its presence and speed on the USB bus. This is done by pulling high either the DP or the DM signal with a 1.5-KΩ resistor.

In order for the host to determine that there are device peripherals present on the USB bus, it must have 15-KΩ pull-down resistors attached to both the DM and DP pins.

All pull-up/pull-down resistors are internal to the ISP1362 therefore there is no need to include these externally in this design.

2.3.9 Suspend/Wake-up

There are two wake-up pins, one dedicated to the device controller and one for the host controller (D_SUSPD/$\overline{\text{WUP}}$ and H_SUSPD/$\overline{\text{WUP}}$). This means that the controller can be placed in the suspend mode when not in use, saving power and can be activated when required.

2.3.10 Circuit Protection

An external power distribution switch has been used for operation in host mode.

When $\overline{\text{H_OC}}$*n* detects an overcurrent status on the downstream port, $\overline{\text{H_PSW}}$*n* outputs a logic 1 to turn off the +5V power supply to the downstream port Vbus. When there is no such detection, $\overline{\text{H_PSW}}$*n* outputs a logic 0 to turn on the +5V power supply to the downstream port Vbus.

The external OC circuit cannot be used when port 1 is being operated in OTG or device mode. In order to access the internal pull-up resistors (SoftConnect) the input has to be Vbus sensing. Jumper 6 should be set by default between pins 1 and 2 when operating in OTG or device mode.

2.3.11 GoodLink LED

Indication of a good USB traffic connection is provided through GoodLink technology. $\overline{\text{GL}}$ is connected to an LED which blinks upon USB traffic.

2.3.12 Capacitors

There is a 22nF capacitor connected to pins CP_CAP1 & 2 which is used by the internal charge pump.

There are also decoupling capacitors connected to both the 3.3-V and 5-V supply rails to reduce EMC.

2.3.13 Vbus

Connected directly to port 1 when operating in OTG or device mode. In order to use SoftConnect the input has to be Vbus sensing.

2.3.14 Power

The M5249C3 board provides a 3.3-V and 5-V supply.

2.3.15 Test Points

A0, A1, CS1, OE1, R/W1, RESET1, INT1, INT2, CLKOUT, DREQ1, DREQ2, DACK1, DACK2, VBUS1, HWUP1, DWUP1, ID1 and OTGMODE1 have all been brought out to test points for use in hardware debug.