Data Sheet

S6D0139

Preliminary

240 RGB X 320 DOT 1-CHIP DRIVER IC WITH INTERNAL GRAM
FOR 262,144 Colors TFT-LCD

APR 19 , 2006

Ver. 0.5

System LSI Division
Semiconductor Business
SAMSUNG ELECTRONICS CO., LTD

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INTRODUCTION

The S6D0139 is a 1-chip solution for TFT-LCD panel: source driver with built-in memory, gate driver and power IC are integrated on one chip. This IC can display to a maximum of 240-RGB x 320 dot graphics on 260k-color TFT panel.

The S6D0139 supports Qualcomm's high-speed serial interface, MDDI (Mobile Display Digital Interface) type I, which is an implementation of client device Video Electronics Standards Association (VESA) standard.
The MDDI is a cost-effective low-power solution that enables high-speed short-range communication with a display device using a digital packet data link.

The S6D0139 offer interface for sub panel driver IC which doesn't support MDDI: it can generate conventional MPU-interface protocol from MDDI packet.

The S6D0139 also supports 18-/16-/9-/8-bits high-speed parallel interface, high-speed RAM-write functions that enable efficient data transfer, and high-speed rewriting of data to the internal GRAM.

There is an external interface. In case of display data, the S6D0139 offers a flexible 18-/16-/6-bits bus of RGB interface for transferring the 260k colors display data.

The motion picture area can be specified in internal GRAM by window function. The specified window area can be updated selectively, so that motion picture can be displayed simultaneously independent of still picture area.

The gamma curve is updated to support Black UI

The S6D0139 has various functions for reducing the power consumption of a LCD system: operating at low voltage (1.8V), register-controlled power-save mode, reduced the power consumption of backlight, partial display mode and so on. The IC has internal GRAM to store 240-RGB x 320 dot 260k-color image and an internal booster that generates the LCD driving voltage, breeder resistance and voltage follower circuit for LCD driver.

Therefore, The S6D0139 offer a special function MIE (Mobile Image Enhancement) which enhances the luminance / contrast adaptively by extracting the image's brightness information and reduces power consumption of the backlight. And The S6D0139 has a Non-Volatile Memory to control voltages.

This LSI is suitable for any medium-sized or small portable mobile solution requiring long-term driving capabilities, such as digital cellular phones supporting a web browser, bi-directional pagers, and small PDAs.

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FEATURES

- **240-RGB x 320 dot TFT-LCD display controller/driver IC for 262,144 colors (720 channel-source driver/ 320 channel-gate driver)**
- **18-/16-/9-/8-bit high-speed parallel bus interface (80- and 68- system) and serial peripheral interface (SPI)**
- **18-/16-/6-bit RGB interface and VSYNC interface**
- **MDDI (Mobile Display Digital Interface) support**
- **Sub Panel Driver IC control function support**
  - Conventional LCD driver IC (80-mode) can be selected as sub panel driver IC.
- **MIE(Mobile Image Enhancement) functions**
  - Adaptive luminance/contrast enhancement function.
  - Reduce the power consumption of backlight
- **MTP supports which is Non-Volatile Memory.**
- **Writing to a window-RAM address area by using a window-address function**
- **Various color-display control functions**
  - 262,144 colors can be displayed at the same time (including gamma adjust)
  - Vertical scroll display function in raster-row units
- **Internal RAM capacity: 240 x 18 x 320 = 1,382,000 bits**
- **Low-power operation supports:**
  - Power-save mode: stand-by mode, sleep mode
  - Partial display of two screens in any position
  - Maximum 6-times step-up circuit for generating driving voltage
  - Voltage followers to decrease direct current flow in the LCD drive breeder-resistors
  - Charge sharing function for the switching performance of step-up circuits and operational amplifiers
- **1-raster row inversion drive (Reverse the polarity of driving voltage in every selected raster row)**
- **Internal oscillation circuit and external hardware reset**
- **Structure for TFT-display retention volume (only for Cst)**
- **Alternating functions for TFT-LCD counter-electrode power**
  - Line alternating drive of Vcom.
- **Internal power supply circuit**
  - Step-up circuit: four to six times positive-polarity, three to five times negative-polarity
  - Adjustment of Vcom amplitude: internal 64-level digital potentiometer
- **Operating voltage**

• Apply voltage

– VDD3 to VSS = 1.65 to 3.3 V	Logic interface (I/O) level. Refer to Voltage Regulation Function.
– VCI to VSS = 2.5 to 3.3 V	Power supply voltage for booster / analog function block

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- Generate voltage

  – For the logic part : VDDM/VDD to VSS = 1.4 ~ 1.6 V (power supply for logic circuits)
  – For the source driver: AVDD to VSS = 3.5 to 6.0V (power supply for driving circuits)
  GVDD to VSS = 3.0 to 5.0V (reference power supply for grayscale voltages)
  – For the gate driver: VGH to VGL = 10.5 to 30 V, VGH to VSS = +7.0 to +18 V,
  VGL to VSS = -18 to -3.5 V.
  – For the step up circuit: VCI1 to VSS = 1.75 to 3.0 V (refer to Instruction Description)
  – For the TFT-LCD counter electrode: Vcom amplitude (max) = 6V,
  VcomH to VSS = 3.0 to 5.0V,
  VcomL to VSS = -2.0 to 0.0V

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BLOCK DIAGRAM

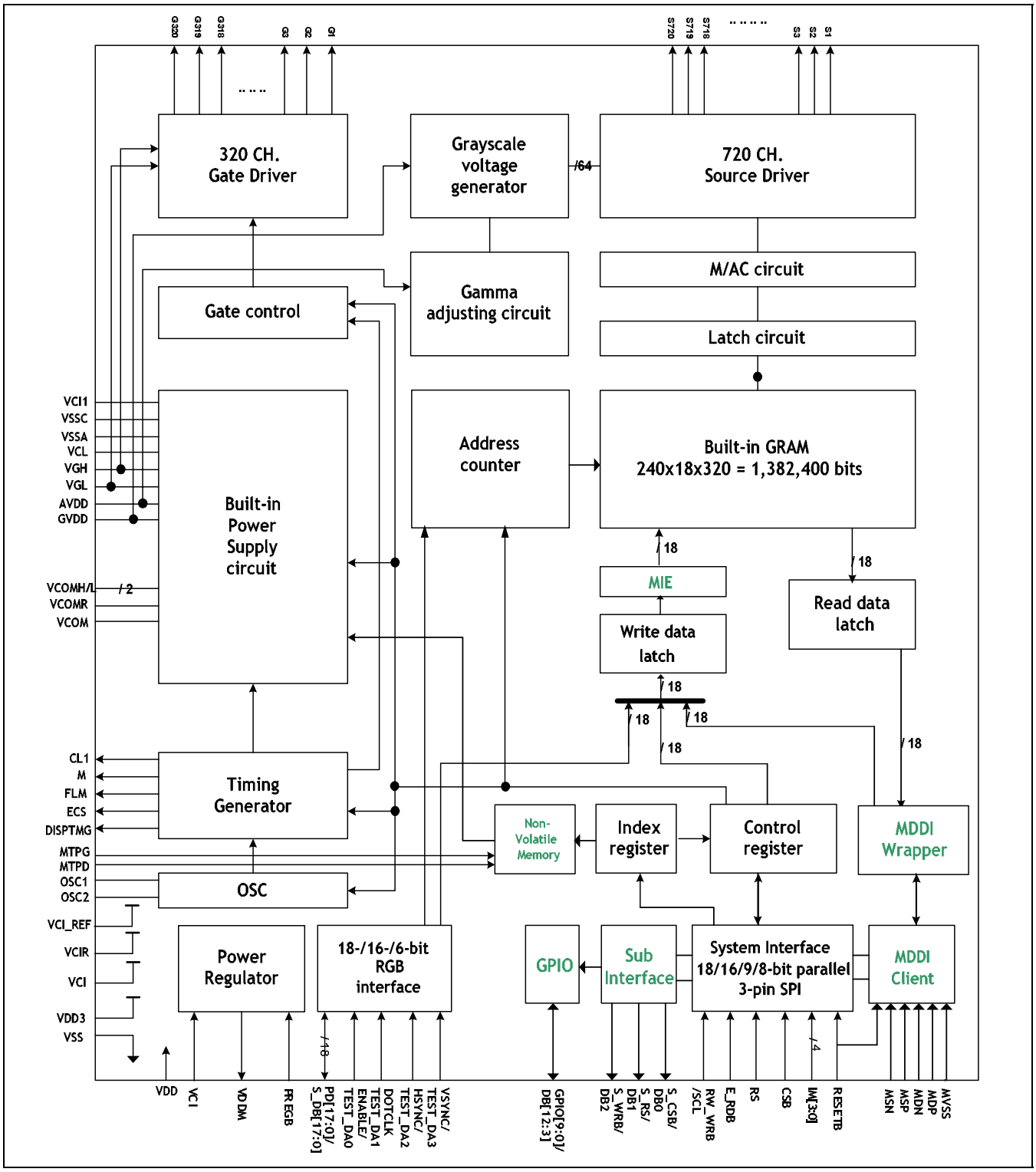

Figure1. S6D0139 Block Diagram

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PAD CONFIGURATION

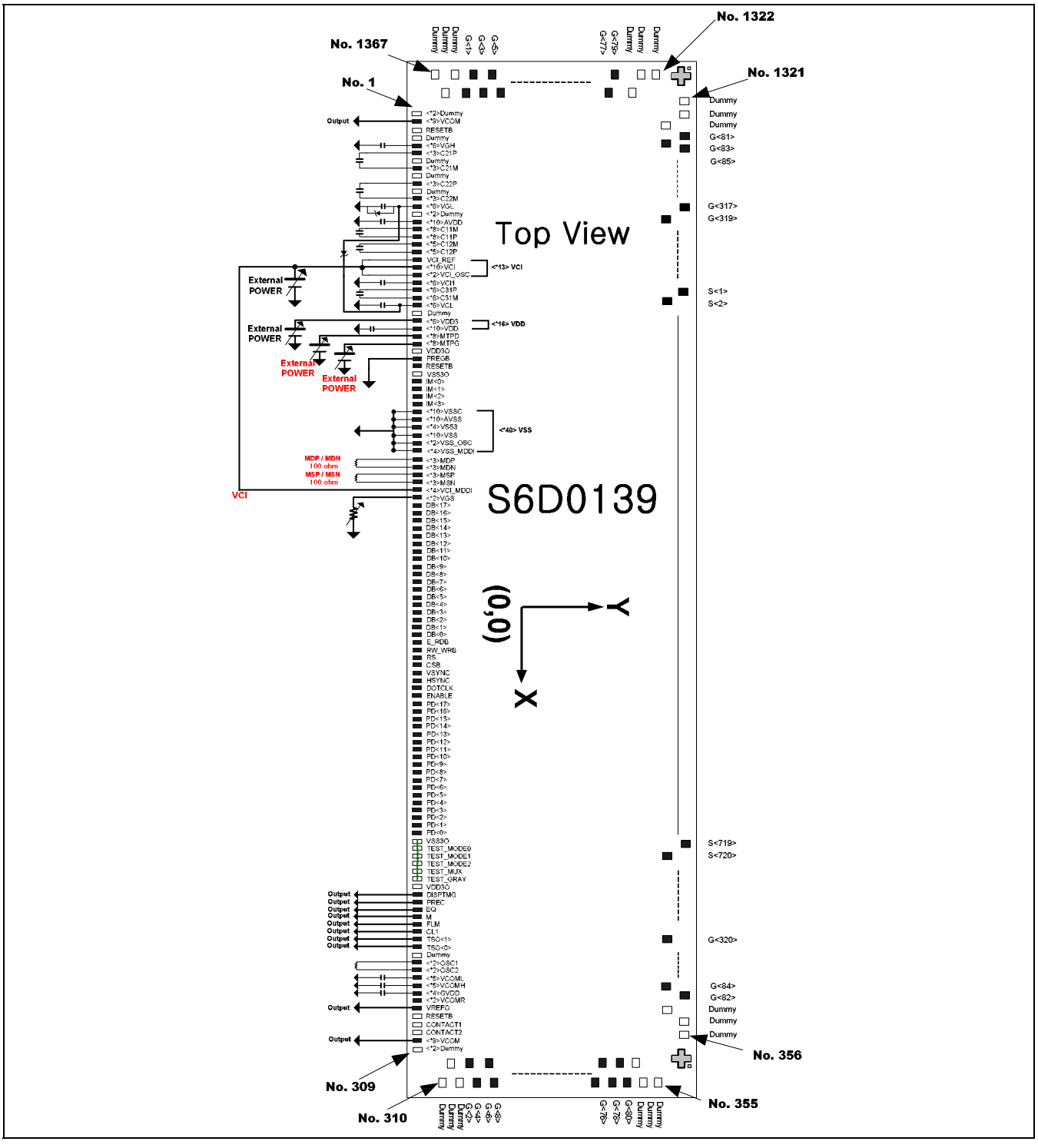

Figure 2. Pad Configuration

NOTES: Backside of the chip is kept at VGL level.

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Table 1. S6D0139 Pad Dimensions

Items	Pad name.	Size		Unit
		X	Y	
Chip size[1)]	-	19380	1430	um
Bumped Pad size	Input Pad	40	91	
	Output Pad	17/18	118/112	
Bumped Pad Height	All Pad	15(typ.) ±3		

NOTES:

1) Scribe line included in this chip size (Scribe lane: 100um)
2) There are two kinds of output bumped pads. The dimensions of bumped pads are 17umX118um and 18umX112um.

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ALIGN KEY CONFIGURATION AND COORDINATE

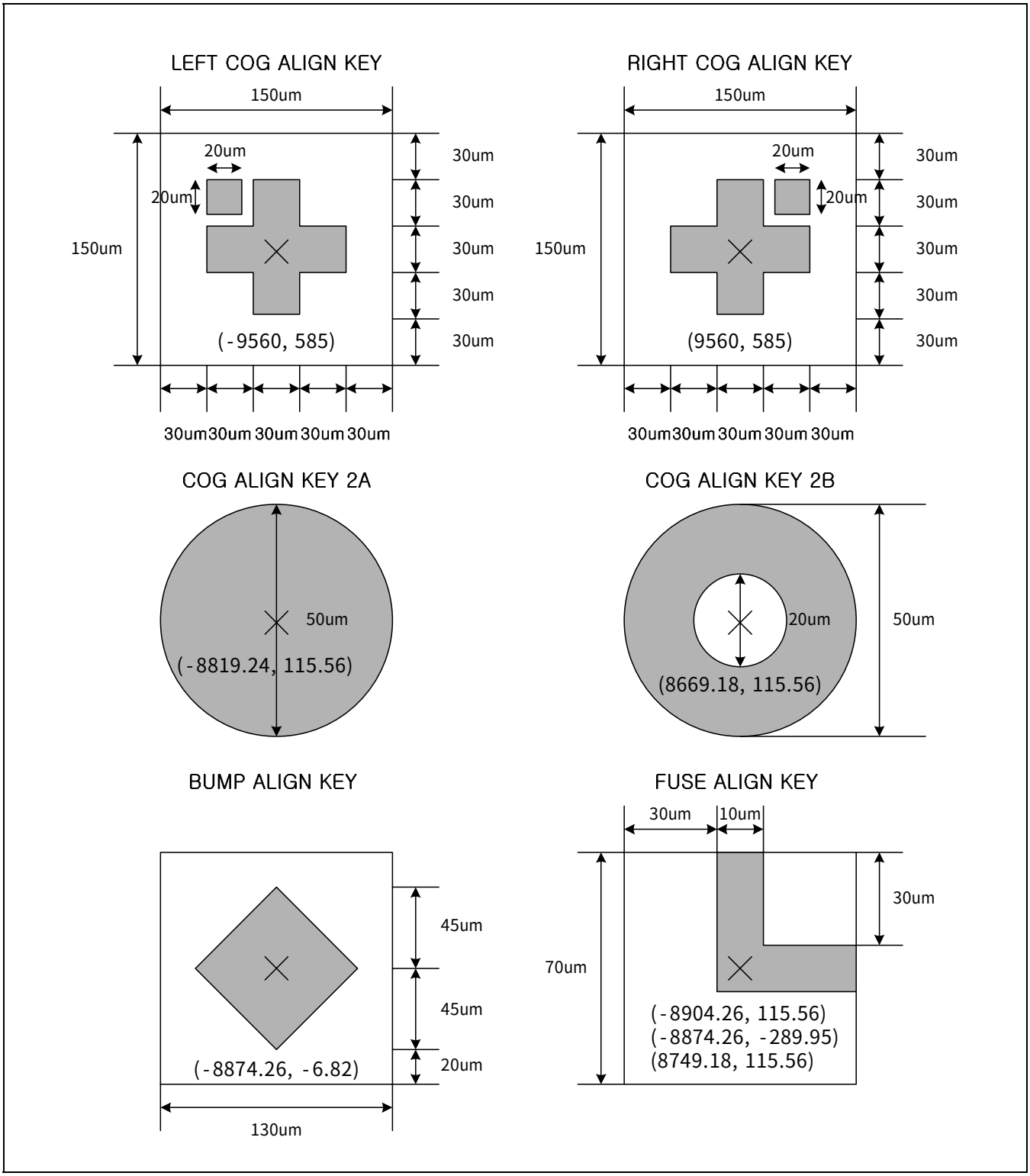

Figure 3. COG and BUMP align key

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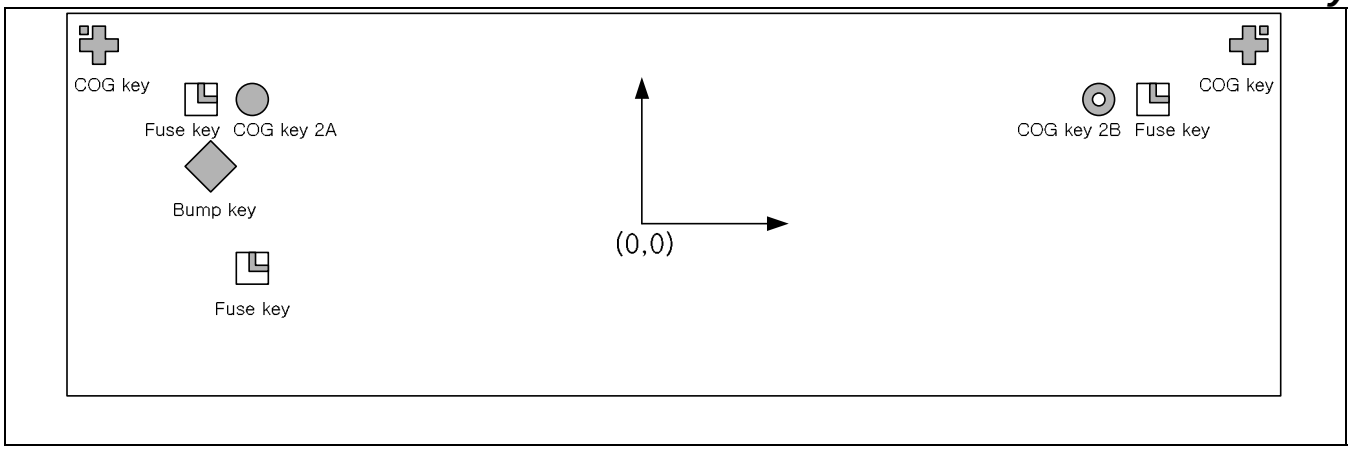

Figure 4. Align key configuration

NOTES:

1. Gold bump height: 15 ± 3 um (typical)

2. Wafer thickness: 470um

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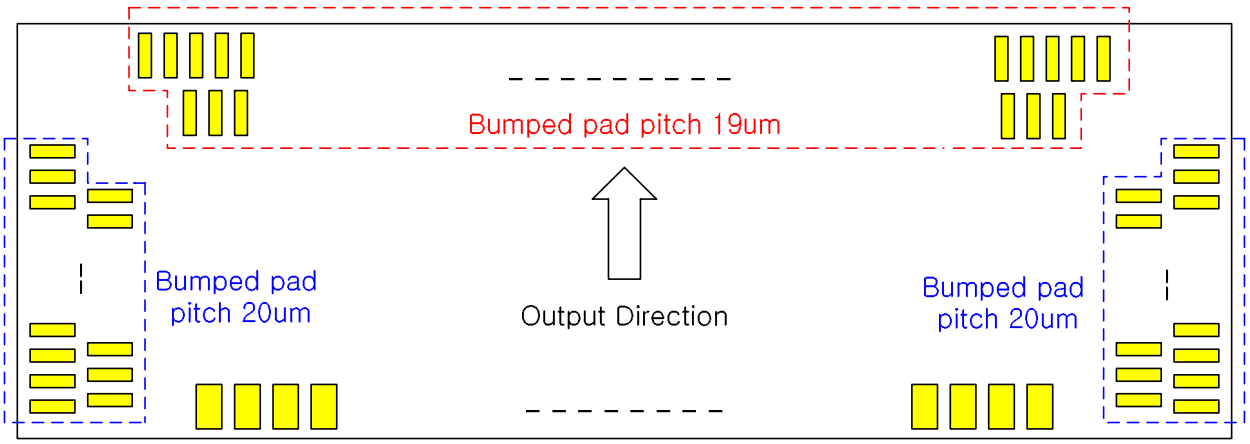
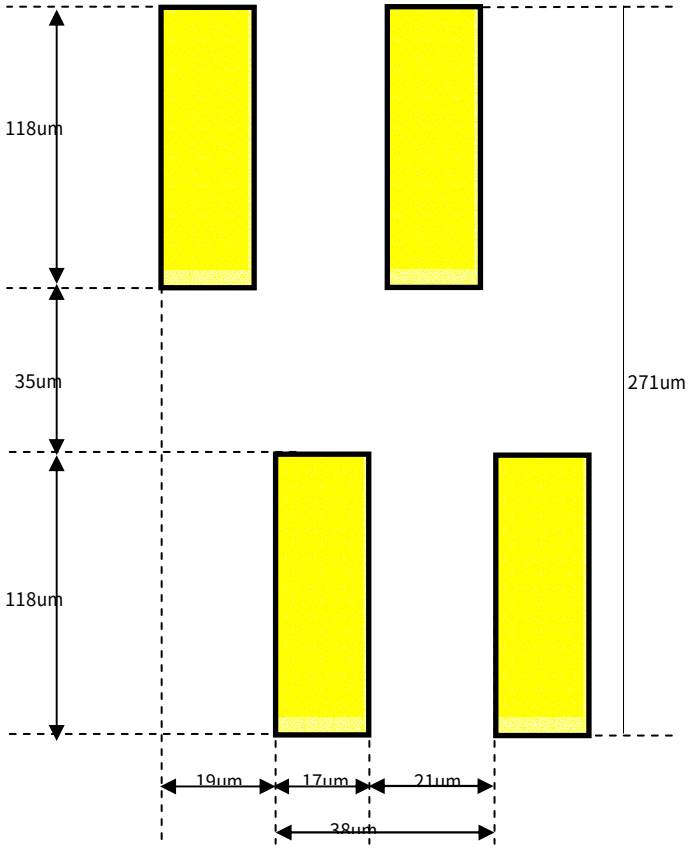
BUMP SIZE

1. Bump pad array



2. Source/Gate output side

A. Top side bumped pad pitch 19um



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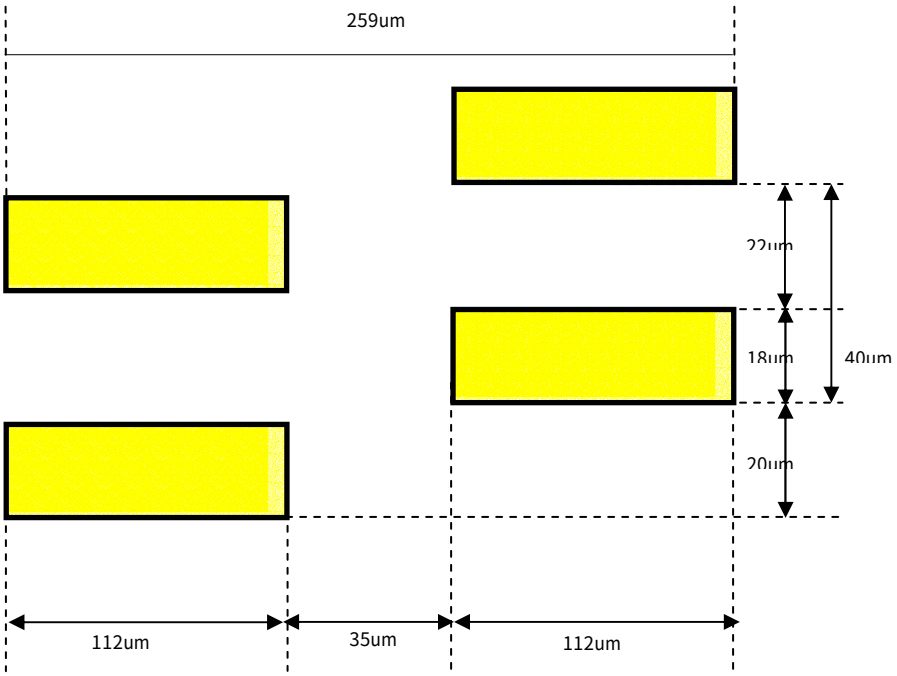
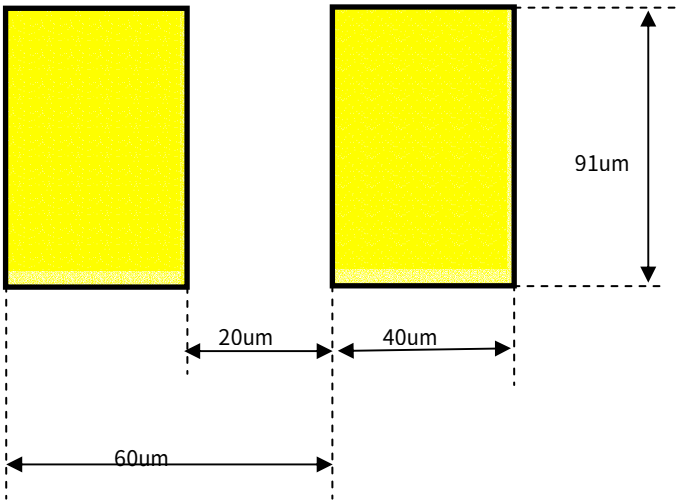
B. Left and right side bumped pad pitch 20um



2. I/O side



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PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

[Unit: um]

No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name
1	-9240	-612.5	DUMMY	65	-5400	-612.5	C11P	129	-1560	-612.5	VDD	193	2280	-612.5	VSS_MDDI
2	-9180	-612.5	DUMMY	66	-5340	-612.5	C11P	130	-1500	-612.5	VDD	194	2340	-612.5	VSS_MDDI
3	-9120	-612.5	VCOM	67	-5280	-612.5	C11P	131	-1440	-612.5	VDD	195	2400	-612.5	VSS_MDDI
4	-9060	-612.5	VCOM	68	-5220	-612.5	C11P	132	-1380	-612.5	VDD	196	2460	-612.5	VSS_MDDI
5	-9000	-612.5	VCOM	69	-5160	-612.5	C12M	133	-1320	-612.5	MTPD	197	2520	-612.5	MDP
6	-8940	-612.5	VCOM	70	-5100	-612.5	C12M	134	-1260	-612.5	MTPD	198	2580	-612.5	MDP
7	-8880	-612.5	VCOM	71	-5040	-612.5	C12M	135	-1200	-612.5	MTPD	199	2640	-612.5	MDP
8	-8820	-612.5	VCOM	72	-4980	-612.5	C12M	136	-1140	-612.5	MTPD	200	2700	-612.5	MDN
9	-8760	-612.5	VCOM	73	-4920	-612.5	C12M	137	-1080	-612.5	MTPD	201	2760	-612.5	MDN
10	-8700	-612.5	VCOM	74	-4860	-612.5	C12P	138	-1020	-612.5	MTPD	202	2820	-612.5	MDN
11	-8640	-612.5	VCOM	75	-4800	-612.5	C12P	139	-960	-612.5	MTPD	203	2880	-612.5	MSP
12	-8580	-612.5	RESETB	76	-4740	-612.5	C12P	140	-900	-612.5	MTPD	204	2940	-612.5	MSP
13	-8520	-612.5	DUMMY	77	-4680	-612.5	C12P	141	-840	-612.5	MTPG	205	3000	-612.5	MSP
14	-8460	-612.5	VGH	78	-4620	-612.5	C12P	142	-780	-612.5	MTPG	206	3060	-612.5	MSN
15	-8400	-612.5	VGH	79	-4560	-612.5	VCI_REF	143	-720	-612.5	MTPG	207	3120	-612.5	MSN
16	-8340	-612.5	VGH	80	-4500	-612.5	VCI	144	-660	-612.5	MTPG	208	3180	-612.5	MSN
17	-8280	-612.5	VGH	81	-4440	-612.5	VCI	145	-600	-612.5	MTPG	209	3240	-612.5	VCI_MDDI
18	-8220	-612.5	VGH	82	-4380	-612.5	VCI	146	-540	-612.5	MTPG	210	3300	-612.5	VCI_MDDI
19	-8160	-612.5	VGH	83	-4320	-612.5	VCI	147	-480	-612.5	MTPG	211	3360	-612.5	VCI_MDDI
20	-8100	-612.5	C21P	84	-4260	-612.5	VCI	148	-420	-612.5	MTPG	212	3420	-612.5	VCI_MDDI
21	-8040	-612.5	C21P	85	-4200	-612.5	VCI	149	-360	-612.5	VDD3O	213	3480	-612.5	VGS
22	-7980	-612.5	C21P	86	-4140	-612.5	VCI	150	-300	-612.5	PREGB	214	3540	-612.5	VGS
23	-7920	-612.5	DUMMY	87	-4080	-612.5	VCI	151	-240	-612.5	RESETB	215	3600	-612.5	DB<17>
24	-7860	-612.5	C21M	88	-4020	-612.5	VCI	152	-180	-612.5	VSS3O	216	3660	-612.5	DB<16>
25	-7800	-612.5	C21M	89	-3960	-612.5	VCI	153	-120	-612.5	IM<0>	217	3720	-612.5	DB<15>
26	-7740	-612.5	C21M	90	-3900	-612.5	VCI_OSC	154	-60	-612.5	IM<1>	218	3780	-612.5	DB<14>
27	-7680	-612.5	DUMMY	91	-3840	-612.5	VCI_OSC	155	0	-612.5	IM<2>	219	3840	-612.5	DB<13>
28	-7620	-612.5	C22P	92	-3780	-612.5	VCI1	156	60	-612.5	IM<3>	220	3900	-612.5	DB<12>
29	-7560	-612.5	C22P	93	-3720	-612.5	VCI1	157	120	-612.5	VSSC	221	3960	-612.5	DB<11>
30	-7500	-612.5	C22P	94	-3660	-612.5	VCI1	158	180	-612.5	VSSC	222	4020	-612.5	DB<10>
31	-7440	-612.5	DUMMY	95	-3600	-612.5	VCI1	159	240	-612.5	VSSC	223	4080	-612.5	DB<9>
32	-7380	-612.5	C22M	96	-3540	-612.5	VCI1	160	300	-612.5	VSSC	224	4140	-612.5	DB<8>
33	-7320	-612.5	C22M	97	-3480	-612.5	VCI1	161	360	-612.5	VSSC	225	4200	-612.5	DB<7>
34	-7260	-612.5	C22M	98	-3420	-612.5	C31P	162	420	-612.5	VSSC	226	4260	-612.5	DB<6>
35	-7200	-612.5	VGL	99	-3360	-612.5	C31P	163	480	-612.5	VSSC	227	4320	-612.5	DB<5>
36	-7140	-612.5	VGL	100	-3300	-612.5	C31P	164	540	-612.5	VSSC	228	4380	-612.5	DB<4>
37	-7080	-612.5	VGL	101	-3240	-612.5	C31P	165	600	-612.5	VSSC	229	4440	-612.5	DB<3>
38	-7020	-612.5	VGL	102	-3180	-612.5	C31P	166	660	-612.5	VSSC	230	4500	-612.5	DB<2>
39	-6960	-612.5	VGL	103	-3120	-612.5	C31P	167	720	-612.5	AVSS	231	4560	-612.5	DB<1>
40	-6900	-612.5	VGL	104	-3060	-612.5	C31M	168	780	-612.5	AVSS	232	4620	-612.5	DB<0>
41	-6840	-612.5	DUMMY	105	-3000	-612.5	C31M	169	840	-612.5	AVSS	233	4680	-612.5	E_RDB
42	-6780	-612.5	DUMMY	106	-2940	-612.5	C31M	170	900	-612.5	AVSS	234	4740	-612.5	RW_WRB
43	-6720	-612.5	AVDD	107	-2880	-612.5	C31M	171	960	-612.5	AVSS	235	4800	-612.5	RS
44	-6660	-612.5	AVDD	108	-2820	-612.5	C31M	172	1020	-612.5	AVSS	236	4860	-612.5	CSB
45	-6600	-612.5	AVDD	109	-2760	-612.5	C31M	173	1080	-612.5	AVSS	237	4920	-612.5	VSYNC
46	-6540	-612.5	AVDD	110	-2700	-612.5	VCL	174	1140	-612.5	AVSS	238	4980	-612.5	HSYNC
47	-6480	-612.5	AVDD	111	-2640	-612.5	VCL	175	1200	-612.5	AVSS	239	5040	-612.5	DOTCLK
48	-6420	-612.5	AVDD	112	-2580	-612.5	VCL	176	1260	-612.5	AVSS	240	5100	-612.5	ENABLE
49	-6360	-612.5	AVDD	113	-2520	-612.5	VCL	177	1320	-612.5	VSS3	241	5160	-612.5	PD<17>
50	-6300	-612.5	AVDD	114	-2460	-612.5	VCL	178	1380	-612.5	VSS3	242	5220	-612.5	PD<16>
51	-6240	-612.5	AVDD	115	-2400	-612.5	VCL	179	1440	-612.5	VSS3	243	5280	-612.5	PD<15>
52	-6180	-612.5	AVDD	116	-2340	-612.5	DUMMY	180	1500	-612.5	VSS3	244	5340	-612.5	PD<14>
53	-6120	-612.5	C11M	117	-2280	-612.5	VDD3	181	1560	-612.5	VSS	245	5400	-612.5	PD<13>
54	-6060	-612.5	C11M	118	-2220	-612.5	VDD3	182	1620	-612.5	VSS	246	5460	-612.5	PD<12>
55	-6000	-612.5	C11M	119	-2160	-612.5	VDD3	183	1680	-612.5	VSS	247	5520	-612.5	PD<11>
56	-5940	-612.5	C11M	120	-2100	-612.5	VDD3	184	1740	-612.5	VSS	248	5580	-612.5	PD<10>
57	-5880	-612.5	C11M	121	-2040	-612.5	VDD3	185	1800	-612.5	VSS	249	5640	-612.5	PD<9>
58	-5820	-612.5	C11M	122	-1980	-612.5	VDD3	186	1860	-612.5	VSS	250	5700	-612.5	PD<8>
59	-5760	-612.5	C11M	123	-1920	-612.5	VDD	187	1920	-612.5	VSS	251	5760	-612.5	PD<7>
60	-5700	-612.5	C11M	124	-1860	-612.5	VDD	188	1980	-612.5	VSS	252	5820	-612.5	PD<6>
61	-5640	-612.5	C11P	125	-1800	-612.5	VDD	189	2040	-612.5	VSS	253	5880	-612.5	PD<5>
62	-5580	-612.5	C11P	126	-1740	-612.5	VDD	190	2100	-612.5	VSS	254	5940	-612.5	PD<4>
63	-5520	-612.5	C11P	127	-1680	-612.5	VDD	191	2160	-612.5	VSS_OSC	255	6000	-612.5	PD<3>
64	-5460	-612.5	C11P	128	-1620	-612.5	VDD	192	2220	-612.5	VSS_OSC	256	6060	-612.5	PD<2>

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Table 3. Pad Center Coordinates (continued)

[Unit: um]

No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name
257	6120	-612.5	PD<1>	321	9430	-294	G<18>	385	8777.5	599	G<134>	449	7561.5	599	G<262>
258	6180	-612.5	PD<0>	322	9577	-274	G<20>	386	8758.5	446	G<136>	450	7542.5	446	G<264>
259	6240	-612.5	VSS3O	323	9430	-254	G<22>	387	8739.5	599	G<138>	451	7523.5	599	G<266>
260	6300	-612.5	TEST_MODE<0>	324	9577	-234	G<24>	388	8720.5	446	G<140>	452	7504.5	446	G<268>
261	6360	-612.5	TEST_MODE<1>	325	9430	-214	G<26>	389	8701.5	599	G<142>	453	7485.5	599	G<270>
262	6420	-612.5	TEST_MODE<2>	326	9577	-194	G<28>	390	8682.5	446	G<144>	454	7466.5	446	G<272>
263	6480	-612.5	TEST_MUX	327	9430	-174	G<30>	391	8663.5	599	G<146>	455	7447.5	599	G<274>
264	6540	-612.5	TEST_GRAY	328	9577	-154	G<32>	392	8644.5	446	G<148>	456	7428.5	446	G<276>
265	6600	-612.5	VDD3O	329	9430	-134	G<34>	393	8625.5	599	G<150>	457	7409.5	599	G<278>
266	6660	-612.5	DISPTMG	330	9577	-114	G<36>	394	8606.5	446	G<152>	458	7390.5	446	G<280>
267	6720	-612.5	PREC	331	9430	-94	G<38>	395	8587.5	599	G<154>	459	7371.5	599	G<282>
268	6780	-612.5	EQ	332	9577	-74	G<40>	396	8568.5	446	G<156>	460	7352.5	446	G<284>
269	6840	-612.5	M	333	9430	-54	G<42>	397	8549.5	599	G<158>	461	7333.5	599	G<286>
270	6900	-612.5	FLM	334	9577	-34	G<44>	398	8530.5	446	G<160>	462	7314.5	446	G<288>
271	6960	-612.5	CL1	335	9430	-14	G<46>	399	8511.5	599	G<162>	463	7295.5	599	G<290>
272	7020	-612.5	TSO<1>	336	9577	6	G<48>	400	8492.5	446	G<164>	464	7276.5	446	G<292>
273	7080	-612.5	TSO<0>	337	9430	26	G<50>	401	8473.5	599	G<166>	465	7257.5	599	G<294>
274	7140	-612.5	DUMMY	338	9577	46	G<52>	402	8454.5	446	G<168>	466	7238.5	446	G<296>
275	7200	-612.5	OSC1	339	9430	66	G<54>	403	8435.5	599	G<170>	467	7219.5	599	G<298>
276	7260	-612.5	OSC1	340	9577	86	G<56>	404	8416.5	446	G<172>	468	7200.5	446	G<300>
277	7320	-612.5	OSC2	341	9430	106	G<58>	405	8397.5	599	G<174>	469	7181.5	599	G<302>
278	7380	-612.5	OSC2	342	9577	126	G<60>	406	8378.5	446	G<176>	470	7162.5	446	G<304>
279	7440	-612.5	VCOML	343	9430	146	G<62>	407	8359.5	599	G<178>	471	7143.5	599	G<306>
280	7500	-612.5	VCOML	344	9577	166	G<64>	408	8340.5	446	G<180>	472	7124.5	446	G<308>
281	7560	-612.5	VCOML	345	9430	186	G<66>	409	8321.5	599	G<182>	473	7105.5	599	G<310>
282	7620	-612.5	VCOML	346	9577	206	G<68>	410	8302.5	446	G<184>	474	7086.5	446	G<312>
283	7680	-612.5	VCOML	347	9430	226	G<70>	411	8283.5	599	G<186>	475	7067.5	599	G<314>
284	7740	-612.5	VCOMH	348	9577	246	G<72>	412	8264.5	446	G<188>	476	7048.5	446	G<316>
285	7800	-612.5	VCOMH	349	9430	266	G<74>	413	8245.5	599	G<190>	477	7029.5	599	G<318>
286	7860	-612.5	VCOMH	350	9577	286	G<76>	414	8226.5	446	G<192>	478	7010.5	446	G<320>
287	7920	-612.5	VCOMH	351	9430	306	G<78>	415	8207.5	599	G<194>	479	6821.5	446	S<720>
288	7980	-612.5	VCOMH	352	9577	326	G<80>	416	8188.5	446	G<196>	480	6802.5	599	S<719>
289	8040	-612.5	GVDD	353	9430	346	DUMMY	417	8169.5	599	G<198>	481	6783.5	446	S<718>
290	8100	-612.5	GVDD	354	9577	366	DUMMY	418	8150.5	446	G<200>	482	6764.5	599	S<717>
291	8160	-612.5	GVDD	355	9577	406	DUMMY	419	8131.5	599	G<202>	483	6745.5	446	S<716>
292	8220	-612.5	GVDD	356	9347.5	599	DUMMY	420	8112.5	446	G<204>	484	6726.5	599	S<715>
293	8280	-612.5	VCOMR	357	9309.5	599	DUMMY	421	8093.5	599	G<206>	485	6707.5	446	S<714>
294	8340	-612.5	VCOMR	358	9290.5	446	DUMMY	422	8074.5	446	G<208>	486	6688.5	599	S<713>
295	8400	-612.5	VREFO	359	9271.5	599	G<82>	423	8055.5	599	G<210>	487	6669.5	446	S<712>
296	8460	-612.5	RESETB	360	9252.5	446	G<84>	424	8036.5	446	G<212>	488	6650.5	599	S<711>
297	8520	-612.5	CONTACT1	361	9233.5	599	G<86>	425	8017.5	599	G<214>	489	6631.5	446	S<710>
298	8580	-612.5	CONTACT2	362	9214.5	446	G<88>	426	7998.5	446	G<216>	490	6612.5	599	S<709>
299	8640	-612.5	VCOM	363	9195.5	599	G<90>	427	7979.5	599	G<218>	491	6593.5	446	S<708>
300	8700	-612.5	VCOM	364	9176.5	446	G<92>	428	7960.5	446	G<220>	492	6574.5	599	S<707>
301	8760	-612.5	VCOM	365	9157.5	599	G<94>	429	7941.5	599	G<222>	493	6555.5	446	S<706>
302	8820	-612.5	VCOM	366	9138.5	446	G<96>	430	7922.5	446	G<224>	494	6536.5	599	S<705>
303	8880	-612.5	VCOM	367	9119.5	599	G<98>	431	7903.5	599	G<226>	495	6517.5	446	S<704>
304	8940	-612.5	VCOM	368	9100.5	446	G<100>	432	7884.5	446	G<228>	496	6498.5	599	S<703>
305	9000	-612.5	VCOM	369	9081.5	599	G<102>	433	7865.5	599	G<230>	497	6479.5	446	S<702>
306	9060	-612.5	VCOM	370	9062.5	446	G<104>	434	7846.5	446	G<232>	498	6460.5	599	S<701>
307	9120	-612.5	VCOM	371	9043.5	599	G<106>	435	7827.5	599	G<234>	499	6441.5	446	S<700>
308	9180	-612.5	DUMMY	372	9024.5	446	G<108>	436	7808.5	446	G<236>	500	6422.5	599	S<699>
309	9240	-612.5	DUMMY	373	9005.5	599	G<110>	437	7789.5	599	G<238>	501	6403.5	446	S<698>
310	9577	-514	DUMMY	374	8986.5	446	G<112>	438	7770.5	446	G<240>	502	6384.5	599	S<697>
311	9430	-494	DUMMY	375	8967.5	599	G<114>	439	7751.5	599	G<242>	503	6365.5	446	S<696>
312	9577	-474	DUMMY	376	8948.5	446	G<116>	440	7732.5	446	G<244>	504	6346.5	599	S<695>
313	9430	-454	G<2>	377	8929.5	599	G<118>	441	7713.5	599	G<246>	505	6327.5	446	S<694>
314	9577	-434	G<4>	378	8910.5	446	G<120>	442	7694.5	446	G<248>	506	6308.5	599	S<693>
315	9430	-414	G<6>	379	8891.5	599	G<122>	443	7675.5	599	G<250>	507	6289.5	446	S<692>
316	9577	-394	G<8>	380	8872.5	446	G<124>	444	7656.5	446	G<252>	508	6270.5	599	S<691>
317	9430	-374	G<10>	381	8853.5	599	G<126>	445	7637.5	599	G<254>	509	6251.5	446	S<690>
318	9577	-354	G<12>	382	8834.5	446	G<128>	446	7618.5	446	G<256>	510	6232.5	599	S<689>
319	9430	-334	G<14>	383	8815.5	599	G<130>	447	7599.5	599	G<258>	511	6213.5	446	S<688>
320	9577	-314	G<16>	384	8796.5	446	G<132>	448	7580.5	446	G<260>	512	6194.5	599	S<687>

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Table 4. Pad Center Coordinates (continued)

[Unit: um]

No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name
513	6175.5	446	S<686>	577	4959.5	446	S<622>	641	3743.5	446	S<558>	705	2527.5	446	S<494>
514	6156.5	599	S<685>	578	4940.5	599	S<621>	642	3724.5	599	S<557>	706	2508.5	599	S<493>
515	6137.5	446	S<684>	579	4921.5	446	S<620>	643	3705.5	446	S<556>	707	2489.5	446	S<492>
516	6118.5	599	S<683>	580	4902.5	599	S<619>	644	3686.5	599	S<555>	708	2470.5	599	S<491>
517	6099.5	446	S<682>	581	4883.5	446	S<618>	645	3667.5	446	S<554>	709	2451.5	446	S<490>
518	6080.5	599	S<681>	582	4864.5	599	S<617>	646	3648.5	599	S<553>	710	2432.5	599	S<489>
519	6061.5	446	S<680>	583	4845.5	446	S<616>	647	3629.5	446	S<552>	711	2413.5	446	S<488>
520	6042.5	599	S<679>	584	4826.5	599	S<615>	648	3610.5	599	S<551>	712	2394.5	599	S<487>
521	6023.5	446	S<678>	585	4807.5	446	S<614>	649	3591.5	446	S<550>	713	2375.5	446	S<486>
522	6004.5	599	S<677>	586	4788.5	599	S<613>	650	3572.5	599	S<549>	714	2356.5	599	S<485>
523	5985.5	446	S<676>	587	4769.5	446	S<612>	651	3553.5	446	S<548>	715	2337.5	446	S<484>
524	5966.5	599	S<675>	588	4750.5	599	S<611>	652	3534.5	599	S<547>	716	2318.5	599	S<483>
525	5947.5	446	S<674>	589	4731.5	446	S<610>	653	3515.5	446	S<546>	717	2299.5	446	S<482>
526	5928.5	599	S<673>	590	4712.5	599	S<609>	654	3496.5	599	S<545>	718	2280.5	599	S<481>
527	5909.5	446	S<672>	591	4693.5	446	S<608>	655	3477.5	446	S<544>	719	2261.5	446	S<480>
528	5890.5	599	S<671>	592	4674.5	599	S<607>	656	3458.5	599	S<543>	720	2242.5	599	S<479>
529	5871.5	446	S<670>	593	4655.5	446	S<606>	657	3439.5	446	S<542>	721	2223.5	446	S<478>
530	5852.5	599	S<669>	594	4636.5	599	S<605>	658	3420.5	599	S<541>	722	2204.5	599	S<477>
531	5833.5	446	S<668>	595	4617.5	446	S<604>	659	3401.5	446	S<540>	723	2185.5	446	S<476>
532	5814.5	599	S<667>	596	4598.5	599	S<603>	660	3382.5	599	S<539>	724	2166.5	599	S<475>
533	5795.5	446	S<666>	597	4579.5	446	S<602>	661	3363.5	446	S<538>	725	2147.5	446	S<474>
534	5776.5	599	S<665>	598	4560.5	599	S<601>	662	3344.5	599	S<537>	726	2128.5	599	S<473>
535	5757.5	446	S<664>	599	4541.5	446	S<600>	663	3325.5	446	S<536>	727	2109.5	446	S<472>
536	5738.5	599	S<663>	600	4522.5	599	S<599>	664	3306.5	599	S<535>	728	2090.5	599	S<471>
537	5719.5	446	S<662>	601	4503.5	446	S<598>	665	3287.5	446	S<534>	729	2071.5	446	S<470>
538	5700.5	599	S<661>	602	4484.5	599	S<597>	666	3268.5	599	S<533>	730	2052.5	599	S<469>
539	5681.5	446	S<660>	603	4465.5	446	S<596>	667	3249.5	446	S<532>	731	2033.5	446	S<468>
540	5662.5	599	S<659>	604	4446.5	599	S<595>	668	3230.5	599	S<531>	732	2014.5	599	S<467>
541	5643.5	446	S<658>	605	4427.5	446	S<594>	669	3211.5	446	S<530>	733	1995.5	446	S<466>
542	5624.5	599	S<657>	606	4408.5	599	S<593>	670	3192.5	599	S<529>	734	1976.5	599	S<465>
543	5605.5	446	S<656>	607	4389.5	446	S<592>	671	3173.5	446	S<528>	735	1957.5	446	S<464>
544	5586.5	599	S<655>	608	4370.5	599	S<591>	672	3154.5	599	S<527>	736	1938.5	599	S<463>
545	5567.5	446	S<654>	609	4351.5	446	S<590>	673	3135.5	446	S<526>	737	1919.5	446	S<462>
546	5548.5	599	S<653>	610	4332.5	599	S<589>	674	3116.5	599	S<525>	738	1900.5	599	S<461>
547	5529.5	446	S<652>	611	4313.5	446	S<588>	675	3097.5	446	S<524>	739	1881.5	446	S<460>
548	5510.5	599	S<651>	612	4294.5	599	S<587>	676	3078.5	599	S<523>	740	1862.5	599	S<459>
549	5491.5	446	S<650>	613	4275.5	446	S<586>	677	3059.5	446	S<522>	741	1843.5	446	S<458>
550	5472.5	599	S<649>	614	4256.5	599	S<585>	678	3040.5	599	S<521>	742	1824.5	599	S<457>
551	5453.5	446	S<648>	615	4237.5	446	S<584>	679	3021.5	446	S<520>	743	1805.5	446	S<456>
552	5434.5	599	S<647>	616	4218.5	599	S<583>	680	3002.5	599	S<519>	744	1786.5	599	S<455>
553	5415.5	446	S<646>	617	4199.5	446	S<582>	681	2983.5	446	S<518>	745	1767.5	446	S<454>
554	5396.5	599	S<645>	618	4180.5	599	S<581>	682	2964.5	599	S<517>	746	1748.5	599	S<453>
555	5377.5	446	S<644>	619	4161.5	446	S<580>	683	2945.5	446	S<516>	747	1729.5	446	S<452>
556	5358.5	599	S<643>	620	4142.5	599	S<579>	684	2926.5	599	S<515>	748	1710.5	599	S<451>
557	5339.5	446	S<642>	621	4123.5	446	S<578>	685	2907.5	446	S<514>	749	1691.5	446	S<450>
558	5320.5	599	S<641>	622	4104.5	599	S<577>	686	2888.5	599	S<513>	750	1672.5	599	S<449>
559	5301.5	446	S<640>	623	4085.5	446	S<576>	687	2869.5	446	S<512>	751	1653.5	446	S<448>
560	5282.5	599	S<639>	624	4066.5	599	S<575>	688	2850.5	599	S<511>	752	1634.5	599	S<447>
561	5263.5	446	S<638>	625	4047.5	446	S<574>	689	2831.5	446	S<510>	753	1615.5	446	S<446>
562	5244.5	599	S<637>	626	4028.5	599	S<573>	690	2812.5	599	S<509>	754	1596.5	599	S<445>
563	5225.5	446	S<636>	627	4009.5	446	S<572>	691	2793.5	446	S<508>	755	1577.5	446	S<444>
564	5206.5	599	S<635>	628	3990.5	599	S<571>	692	2774.5	599	S<507>	756	1558.5	599	S<443>
565	5187.5	446	S<634>	629	3971.5	446	S<570>	693	2755.5	446	S<506>	757	1539.5	446	S<442>
566	5168.5	599	S<633>	630	3952.5	599	S<569>	694	2736.5	599	S<505>	758	1520.5	599	S<441>
567	5149.5	446	S<632>	631	3933.5	446	S<568>	695	2717.5	446	S<504>	759	1501.5	446	S<440>
568	5130.5	599	S<631>	632	3914.5	599	S<567>	696	2698.5	599	S<503>	760	1482.5	599	S<439>
569	5111.5	446	S<630>	633	3895.5	446	S<566>	697	2679.5	446	S<502>	761	1463.5	446	S<438>
570	5092.5	599	S<629>	634	3876.5	599	S<565>	698	2660.5	599	S<501>	762	1444.5	599	S<437>
571	5073.5	446	S<628>	635	3857.5	446	S<564>	699	2641.5	446	S<500>	763	1425.5	446	S<436>
572	5054.5	599	S<627>	636	3838.5	599	S<563>	700	2622.5	599	S<499>	764	1406.5	599	S<435>
573	5035.5	446	S<626>	637	3819.5	446	S<562>	701	2603.5	446	S<498>	765	1387.5	446	S<434>
574	5016.5	599	S<625>	638	3800.5	599	S<561>	702	2584.5	599	S<497>	766	1368.5	599	S<433>
575	4997.5	446	S<624>	639	3781.5	446	S<560>	703	2565.5	446	S<496>	767	1349.5	446	S<432>
576	4978.5	599	S<623>	640	3762.5	599	S<559>	704	2546.5	599	S<495>	768	1330.5	599	S<431>

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Table 5. Pad Center Coordinates (continued)

[Unit: um]

No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name
769	1311.5	446	S<430>	833	95.5	446	S<366>	897	-1120.5	446	S<302>	961	-2336.5	446	S<238>
770	1292.5	599	S<429>	834	76.5	599	S<365>	898	-1139.5	599	S<301>	962	-2355.5	599	S<237>
771	1273.5	446	S<428>	835	57.5	446	S<364>	899	-1158.5	446	S<300>	963	-2374.5	446	S<236>
772	1254.5	599	S<427>	836	38.5	599	S<363>	900	-1177.5	599	S<299>	964	-2393.5	599	S<235>
773	1235.5	446	S<426>	837	19.5	446	S<362>	901	-1196.5	446	S<298>	965	-2412.5	446	S<234>
774	1216.5	599	S<425>	838	0.5	599	S<361>	902	-1215.5	599	S<297>	966	-2431.5	599	S<233>
775	1197.5	446	S<424>	839	-18.5	446	S<360>	903	-1234.5	446	S<296>	967	-2450.5	446	S<232>
776	1178.5	599	S<423>	840	-37.5	599	S<359>	904	-1253.5	599	S<295>	968	-2469.5	599	S<231>
777	1159.5	446	S<422>	841	-56.5	446	S<358>	905	-1272.5	446	S<294>	969	-2488.5	446	S<230>
778	1140.5	599	S<421>	842	-75.5	599	S<357>	906	-1291.5	599	S<293>	970	-2507.5	599	S<229>
779	1121.5	446	S<420>	843	-94.5	446	S<356>	907	-1310.5	446	S<292>	971	-2526.5	446	S<228>
780	1102.5	599	S<419>	844	-113.5	599	S<355>	908	-1329.5	599	S<291>	972	-2545.5	599	S<227>
781	1083.5	446	S<418>	845	-132.5	446	S<354>	909	-1348.5	446	S<290>	973	-2564.5	446	S<226>
782	1064.5	599	S<417>	846	-151.5	599	S<353>	910	-1367.5	599	S<289>	974	-2583.5	599	S<225>
783	1045.5	446	S<416>	847	-170.5	446	S<352>	911	-1386.5	446	S<288>	975	-2602.5	446	S<224>
784	1026.5	599	S<415>	848	-189.5	599	S<351>	912	-1405.5	599	S<287>	976	-2621.5	599	S<223>
785	1007.5	446	S<414>	849	-208.5	446	S<350>	913	-1424.5	446	S<286>	977	-2640.5	446	S<222>
786	988.5	599	S<413>	850	-227.5	599	S<349>	914	-1443.5	599	S<285>	978	-2659.5	599	S<221>
787	969.5	446	S<412>	851	-246.5	446	S<348>	915	-1462.5	446	S<284>	979	-2678.5	446	S<220>
788	950.5	599	S<411>	852	-265.5	599	S<347>	916	-1481.5	599	S<283>	980	-2697.5	599	S<219>
789	931.5	446	S<410>	853	-284.5	446	S<346>	917	-1500.5	446	S<282>	981	-2716.5	446	S<218>
790	912.5	599	S<409>	854	-303.5	599	S<345>	918	-1519.5	599	S<281>	982	-2735.5	599	S<217>
791	893.5	446	S<408>	855	-322.5	446	S<344>	919	-1538.5	446	S<280>	983	-2754.5	446	S<216>
792	874.5	599	S<407>	856	-341.5	599	S<343>	920	-1557.5	599	S<279>	984	-2773.5	599	S<215>
793	855.5	446	S<406>	857	-360.5	446	S<342>	921	-1576.5	446	S<278>	985	-2792.5	446	S<214>
794	836.5	599	S<405>	858	-379.5	599	S<341>	922	-1595.5	599	S<277>	986	-2811.5	599	S<213>
795	817.5	446	S<404>	859	-398.5	446	S<340>	923	-1614.5	446	S<276>	987	-2830.5	446	S<212>
796	798.5	599	S<403>	860	-417.5	599	S<339>	924	-1633.5	599	S<275>	988	-2849.5	599	S<211>
797	779.5	446	S<402>	861	-436.5	446	S<338>	925	-1652.5	446	S<274>	989	-2868.5	446	S<210>
798	760.5	599	S<401>	862	-455.5	599	S<337>	926	-1671.5	599	S<273>	990	-2887.5	599	S<209>
799	741.5	446	S<400>	863	-474.5	446	S<336>	927	-1690.5	446	S<272>	991	-2906.5	446	S<208>
800	722.5	599	S<399>	864	-493.5	599	S<335>	928	-1709.5	599	S<271>	992	-2925.5	599	S<207>
801	703.5	446	S<398>	865	-512.5	446	S<334>	929	-1728.5	446	S<270>	993	-2944.5	446	S<206>
802	684.5	599	S<397>	866	-531.5	599	S<333>	930	-1747.5	599	S<269>	994	-2963.5	599	S<205>
803	665.5	446	S<396>	867	-550.5	446	S<332>	931	-1766.5	446	S<268>	995	-2982.5	446	S<204>
804	646.5	599	S<395>	868	-569.5	599	S<331>	932	-1785.5	599	S<267>	996	-3001.5	599	S<203>
805	627.5	446	S<394>	869	-588.5	446	S<330>	933	-1804.5	446	S<266>	997	-3020.5	446	S<202>
806	608.5	599	S<393>	870	-607.5	599	S<329>	934	-1823.5	599	S<265>	998	-3039.5	599	S<201>
807	589.5	446	S<392>	871	-626.5	446	S<328>	935	-1842.5	446	S<264>	999	-3058.5	446	S<200>
808	570.5	599	S<391>	872	-645.5	599	S<327>	936	-1861.5	599	S<263>	1000	-3077.5	599	S<199>
809	551.5	446	S<390>	873	-664.5	446	S<326>	937	-1880.5	446	S<262>	1001	-3096.5	446	S<198>
810	532.5	599	S<389>	874	-683.5	599	S<325>	938	-1899.5	599	S<261>	1002	-3115.5	599	S<197>
811	513.5	446	S<388>	875	-702.5	446	S<324>	939	-1918.5	446	S<260>	1003	-3134.5	446	S<196>
812	494.5	599	S<387>	876	-721.5	599	S<323>	940	-1937.5	599	S<259>	1004	-3153.5	599	S<195>
813	475.5	446	S<386>	877	-740.5	446	S<322>	941	-1956.5	446	S<258>	1005	-3172.5	446	S<194>
814	456.5	599	S<385>	878	-759.5	599	S<321>	942	-1975.5	599	S<257>	1006	-3191.5	599	S<193>
815	437.5	446	S<384>	879	-778.5	446	S<320>	943	-1994.5	446	S<256>	1007	-3210.5	446	S<192>
816	418.5	599	S<383>	880	-797.5	599	S<319>	944	-2013.5	599	S<255>	1008	-3229.5	599	S<191>
817	399.5	446	S<382>	881	-816.5	446	S<318>	945	-2032.5	446	S<254>	1009	-3248.5	446	S<190>
818	380.5	599	S<381>	882	-835.5	599	S<317>	946	-2051.5	599	S<253>	1010	-3267.5	599	S<189>
819	361.5	446	S<380>	883	-854.5	446	S<316>	947	-2070.5	446	S<252>	1011	-3286.5	446	S<188>
820	342.5	599	S<379>	884	-873.5	599	S<315>	948	-2089.5	599	S<251>	1012	-3305.5	599	S<187>
821	323.5	446	S<378>	885	-892.5	446	S<314>	949	-2108.5	446	S<250>	1013	-3324.5	446	S<186>
822	304.5	599	S<377>	886	-911.5	599	S<313>	950	-2127.5	599	S<249>	1014	-3343.5	599	S<185>
823	285.5	446	S<376>	887	-930.5	446	S<312>	951	-2146.5	446	S<248>	1015	-3362.5	446	S<184>
824	266.5	599	S<375>	888	-949.5	599	S<311>	952	-2165.5	599	S<247>	1016	-3381.5	599	S<183>
825	247.5	446	S<374>	889	-968.5	446	S<310>	953	-2184.5	446	S<246>	1017	-3400.5	446	S<182>
826	228.5	599	S<373>	890	-987.5	599	S<309>	954	-2203.5	599	S<245>	1018	-3419.5	599	S<181>
827	209.5	446	S<372>	891	-1006.5	446	S<308>	955	-2222.5	446	S<244>	1019	-3438.5	446	S<180>
828	190.5	599	S<371>	892	-1025.5	599	S<307>	956	-2241.5	599	S<243>	1020	-3457.5	599	S<179>
829	171.5	446	S<370>	893	-1044.5	446	S<306>	957	-2260.5	446	S<242>	1021	-3476.5	446	S<178>
830	152.5	599	S<369>	894	-1063.5	599	S<305>	958	-2279.5	599	S<241>	1022	-3495.5	599	S<177>
831	133.5	446	S<368>	895	-1082.5	446	S<304>	959	-2298.5	446	S<240>	1023	-3514.5	446	S<176>
832	114.5	599	S<367>	896	-1101.5	599	S<303>	960	-2317.5	599	S<239>	1024	-3533.5	599	S<175>

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Table 6. Pad Center Coordinates (continued)

[Unit: um]

No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name
1025	-3552.5	446	S<174>	1089	-4768.5	446	S<110>	1153	-5984.5	446	S<46>	1217	-7352.5	446	G<283>
1026	-3571.5	599	S<173>	1090	-4787.5	599	S<109>	1154	-6003.5	599	S<45>	1218	-7371.5	599	G<281>
1027	-3590.5	446	S<172>	1091	-4806.5	446	S<108>	1155	-6022.5	446	S<44>	1219	-7390.5	446	G<279>
1028	-3609.5	599	S<171>	1092	-4825.5	599	S<107>	1156	-6041.5	599	S<43>	1220	-7409.5	599	G<277>
1029	-3628.5	446	S<170>	1093	-4844.5	446	S<106>	1157	-6060.5	446	S<42>	1221	-7428.5	446	G<275>
1030	-3647.5	599	S<169>	1094	-4863.5	599	S<105>	1158	-6079.5	599	S<41>	1222	-7447.5	599	G<273>
1031	-3666.5	446	S<168>	1095	-4882.5	446	S<104>	1159	-6098.5	446	S<40>	1223	-7466.5	446	G<271>
1032	-3685.5	599	S<167>	1096	-4901.5	599	S<103>	1160	-6117.5	599	S<39>	1224	-7485.5	599	G<269>
1033	-3704.5	446	S<166>	1097	-4920.5	446	S<102>	1161	-6136.5	446	S<38>	1225	-7504.5	446	G<267>
1034	-3723.5	599	S<165>	1098	-4939.5	599	S<101>	1162	-6155.5	599	S<37>	1226	-7523.5	599	G<265>
1035	-3742.5	446	S<164>	1099	-4958.5	446	S<100>	1163	-6174.5	446	S<36>	1227	-7542.5	446	G<263>
1036	-3761.5	599	S<163>	1100	-4977.5	599	S<99>	1164	-6193.5	599	S<35>	1228	-7561.5	599	G<261>
1037	-3780.5	446	S<162>	1101	-4996.5	446	S<98>	1165	-6212.5	446	S<34>	1229	-7580.5	446	G<259>
1038	-3799.5	599	S<161>	1102	-5015.5	599	S<97>	1166	-6231.5	599	S<33>	1230	-7599.5	599	G<257>
1039	-3818.5	446	S<160>	1103	-5034.5	446	S<96>	1167	-6250.5	446	S<32>	1231	-7618.5	446	G<255>
1040	-3837.5	599	S<159>	1104	-5053.5	599	S<95>	1168	-6269.5	599	S<31>	1232	-7637.5	599	G<253>
1041	-3856.5	446	S<158>	1105	-5072.5	446	S<94>	1169	-6288.5	446	S<30>	1233	-7656.5	446	G<251>
1042	-3875.5	599	S<157>	1106	-5091.5	599	S<93>	1170	-6307.5	599	S<29>	1234	-7675.5	599	G<249>
1043	-3894.5	446	S<156>	1107	-5110.5	446	S<92>	1171	-6326.5	446	S<28>	1235	-7694.5	446	G<247>
1044	-3913.5	599	S<155>	1108	-5129.5	599	S<91>	1172	-6345.5	599	S<27>	1236	-7713.5	599	G<245>
1045	-3932.5	446	S<154>	1109	-5148.5	446	S<90>	1173	-6364.5	446	S<26>	1237	-7732.5	446	G<243>
1046	-3951.5	599	S<153>	1110	-5167.5	599	S<89>	1174	-6383.5	599	S<25>	1238	-7751.5	599	G<241>
1047	-3970.5	446	S<152>	1111	-5186.5	446	S<88>	1175	-6402.5	446	S<24>	1239	-7770.5	446	G<239>
1048	-3989.5	599	S<151>	1112	-5205.5	599	S<87>	1176	-6421.5	599	S<23>	1240	-7789.5	599	G<237>
1049	-4008.5	446	S<150>	1113	-5224.5	446	S<86>	1177	-6440.5	446	S<22>	1241	-7808.5	446	G<235>
1050	-4027.5	599	S<149>	1114	-5243.5	599	S<85>	1178	-6459.5	599	S<21>	1242	-7827.5	599	G<233>
1051	-4046.5	446	S<148>	1115	-5262.5	446	S<84>	1179	-6478.5	446	S<20>	1243	-7846.5	446	G<231>
1052	-4065.5	599	S<147>	1116	-5281.5	599	S<83>	1180	-6497.5	599	S<19>	1244	-7865.5	599	G<229>
1053	-4084.5	446	S<146>	1117	-5300.5	446	S<82>	1181	-6516.5	446	S<18>	1245	-7884.5	446	G<227>
1054	-4103.5	599	S<145>	1118	-5319.5	599	S<81>	1182	-6535.5	599	S<17>	1246	-7903.5	599	G<225>
1055	-4122.5	446	S<144>	1119	-5338.5	446	S<80>	1183	-6554.5	446	S<16>	1247	-7922.5	446	G<223>
1056	-4141.5	599	S<143>	1120	-5357.5	599	S<79>	1184	-6573.5	599	S<15>	1248	-7941.5	599	G<221>
1057	-4160.5	446	S<142>	1121	-5376.5	446	S<78>	1185	-6592.5	446	S<14>	1249	-7960.5	446	G<219>
1058	-4179.5	599	S<141>	1122	-5395.5	599	S<77>	1186	-6611.5	599	S<13>	1250	-7979.5	599	G<217>
1059	-4198.5	446	S<140>	1123	-5414.5	446	S<76>	1187	-6630.5	446	S<12>	1251	-7998.5	446	G<215>
1060	-4217.5	599	S<139>	1124	-5433.5	599	S<75>	1188	-6649.5	599	S<11>	1252	-8017.5	599	G<213>
1061	-4236.5	446	S<138>	1125	-5452.5	446	S<74>	1189	-6668.5	446	S<10>	1253	-8036.5	446	G<211>
1062	-4255.5	599	S<137>	1126	-5471.5	599	S<73>	1190	-6687.5	599	S<9>	1254	-8055.5	599	G<209>
1063	-4274.5	446	S<136>	1127	-5490.5	446	S<72>	1191	-6706.5	446	S<8>	1255	-8074.5	446	G<207>
1064	-4293.5	599	S<135>	1128	-5509.5	599	S<71>	1192	-6725.5	599	S<7>	1256	-8093.5	599	G<205>
1065	-4312.5	446	S<134>	1129	-5528.5	446	S<70>	1193	-6744.5	446	S<6>	1257	-8112.5	446	G<203>
1066	-4331.5	599	S<133>	1130	-5547.5	599	S<69>	1194	-6763.5	599	S<5>	1258	-8131.5	599	G<201>
1067	-4350.5	446	S<132>	1131	-5566.5	446	S<68>	1195	-6782.5	446	S<4>	1259	-8150.5	446	G<199>
1068	-4369.5	599	S<131>	1132	-5585.5	599	S<67>	1196	-6801.5	599	S<3>	1260	-8169.5	599	G<197>
1069	-4388.5	446	S<130>	1133	-5604.5	446	S<66>	1197	-6820.5	446	S<2>	1261	-8188.5	446	G<195>
1070	-4407.5	599	S<129>	1134	-5623.5	599	S<65>	1198	-6839.5	599	S<1>	1262	-8207.5	599	G<193>
1071	-4426.5	446	S<128>	1135	-5642.5	446	S<64>	1199	-7010.5	446	G<319>	1263	-8226.5	446	G<191>
1072	-4445.5	599	S<127>	1136	-5661.5	599	S<63>	1200	-7029.5	599	G<317>	1264	-8245.5	599	G<189>
1073	-4464.5	446	S<126>	1137	-5680.5	446	S<62>	1201	-7048.5	446	G<315>	1265	-8264.5	446	G<187>
1074	-4483.5	599	S<125>	1138	-5699.5	599	S<61>	1202	-7067.5	599	G<313>	1266	-8283.5	599	G<185>
1075	-4502.5	446	S<124>	1139	-5718.5	446	S<60>	1203	-7086.5	446	G<311>	1267	-8302.5	446	G<183>
1076	-4521.5	599	S<123>	1140	-5737.5	599	S<59>	1204	-7105.5	599	G<309>	1268	-8321.5	599	G<181>
1077	-4540.5	446	S<122>	1141	-5756.5	446	S<58>	1205	-7124.5	446	G<307>	1269	-8340.5	446	G<179>
1078	-4559.5	599	S<121>	1142	-5775.5	599	S<57>	1206	-7143.5	599	G<305>	1270	-8359.5	599	G<177>
1079	-4578.5	446	S<120>	1143	-5794.5	446	S<56>	1207	-7162.5	446	G<303>	1271	-8378.5	446	G<175>
1080	-4597.5	599	S<119>	1144	-5813.5	599	S<55>	1208	-7181.5	599	G<301>	1272	-8397.5	599	G<173>
1081	-4616.5	446	S<118>	1145	-5832.5	446	S<54>	1209	-7200.5	446	G<299>	1273	-8416.5	446	G<171>
1082	-4635.5	599	S<117>	1146	-5851.5	599	S<53>	1210	-7219.5	599	G<297>	1274	-8435.5	599	G<169>
1083	-4654.5	446	S<116>	1147	-5870.5	446	S<52>	1211	-7238.5	446	G<295>	1275	-8454.5	446	G<167>
1084	-4673.5	599	S<115>	1148	-5889.5	599	S<51>	1212	-7257.5	599	G<293>	1276	-8473.5	599	G<165>
1085	-4692.5	446	S<114>	1149	-5908.5	446	S<50>	1213	-7276.5	446	G<291>	1277	-8492.5	446	G<163>
1086	-4711.5	599	S<113>	1150	-5927.5	599	S<49>	1214	-7295.5	599	G<289>	1278	-8511.5	599	G<161>
1087	-4730.5	446	S<112>	1151	-5946.5	446	S<48>	1215	-7314.5	446	G<287>	1279	-8530.5	446	G<159>
1088	-4749.5	599	S<111>	1152	-5965.5	599	S<47>	1216	-7333.5	599	G<285>	1280	-8549.5	599	G<157>

Preliminary

Table 7. Pad Center Coordinates (continued)

[Unit: um]

No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name	No.	X	Y	Pad Name
1281	-8568.5	446	G<155>	1345	-9577	-74	G<39>								
1282	-8587.5	599	G<153>	1346	-9430	-94	G<37>								
1283	-8606.5	446	G<151>	1347	-9577	-114	G<35>								
1284	-8625.5	599	G<149>	1348	-9430	-134	G<33>								
1285	-8644.5	446	G<147>	1349	-9577	-154	G<31>								
1286	-8663.5	599	G<145>	1350	-9430	-174	G<29>								
1287	-8682.5	446	G<143>	1351	-9577	-194	G<27>								
1288	-8701.5	599	G<141>	1352	-9430	-214	G<25>								
1289	-8720.5	446	G<139>	1353	-9577	-234	G<23>								
1290	-8739.5	599	G<137>	1354	-9430	-254	G<21>								
1291	-8758.5	446	G<135>	1355	-9577	-274	G<19>								
1292	-8777.5	599	G<133>	1356	-9430	-294	G<17>								
1293	-8796.5	446	G<131>	1357	-9577	-314	G<15>								
1294	-8815.5	599	G<129>	1358	-9430	-334	G<13>								
1295	-8834.5	446	G<127>	1359	-9577	-354	G<11>								
1296	-8853.5	599	G<125>	1360	-9430	-374	G<9>								
1297	-8872.5	446	G<123>	1361	-9577	-394	G<7>								
1298	-8891.5	599	G<121>	1362	-9430	-414	G<5>								
1299	-8910.5	446	G<119>	1363	-9577	-434	G<3>								
1300	-8929.5	599	G<117>	1364	-9430	-454	G<1>								
1301	-8948.5	446	G<115>	1365	-9577	-474	DUMMY								
1302	-8967.5	599	G<113>	1366	-9430	-494	DUMMY								
1303	-8986.5	446	G<111>	1367	-9577	-514	DUMMY								
1304	-9005.5	599	G<109>												
1305	-9024.5	446	G<107>												
1306	-9043.5	599	G<105>												
1307	-9062.5	446	G<103>												
1308	-9081.5	599	G<101>												
1309	-9100.5	446	G<99>												
1310	-9119.5	599	G<97>												
1311	-9138.5	446	G<95>												
1312	-9157.5	599	G<93>												
1313	-9176.5	446	G<91>												
1314	-9195.5	599	G<89>												
1315	-9214.5	446	G<87>												
1316	-9233.5	599	G<85>												
1317	-9252.5	446	G<83>												
1318	-9271.5	599	G<81>												
1319	-9290.5	446	DUMMY												
1320	-9309.5	599	DUMMY												
1321	-9347.5	599	DUMMY												
1322	-9577	406	DUMMY												
1323	-9577	366	DUMMY												
1324	-9430	346	DUMMY												
1325	-9577	326	G<79>												
1326	-9430	306	G<77>												
1327	-9577	286	G<75>												
1328	-9430	266	G<73>												
1329	-9577	246	G<71>												
1330	-9430	226	G<69>												
1331	-9577	206	G<67>												
1332	-9430	186	G<65>												
1333	-9577	166	G<63>												
1334	-9430	146	G<61>												
1335	-9577	126	G<59>												
1336	-9430	106	G<57>												
1337	-9577	86	G<55>												
1338	-9430	66	G<53>												
1339	-9577	46	G<51>												
1340	-9430	26	G<49>												
1341	-9577	6	G<47>												
1342	-9430	-14	G<45>												
1343	-9577	-34	G<43>												
1344	-9430	-54	G<41>												

Preliminary

PIN DESCRIPTION

POWER SUPPLY PIN

Table 8. Power supply pin description

Symbol	I/O	Description
VDD	I Power	System Logic power supply. (1.4 ~ 1.5 ~ 1.6 V) Connect a capacitor for stabilization. When internal regulator is not used, connect an external power supply. (1.4 ~1.5 ~ 1.6V)
PREGB	I	Internal power regulator control input pin. When the internal regulated power is used as VDD, PREGB is fixed to “low” level. When the external logic power is used as VDD (1.4V ~ 1.5V ~ 1.6V), PREGB is fixed to “high” level.
VDD3	I Power	I/O power supply for external interface. (VDD3: +1.65 ~ +3.3 V)
AVDD	O Power	A power output pin for source driver block that is generated from power block. Connect a capacitor for stabilization. (AVDD: +3.5 ~ +6.0 V)
GVDD	O Power	A standard level for grayscale voltage generator. Connect a capacitor for stabilization. When internal GVDD generator is not used, connect an external power supply. (GVDD = 3.0 ~ 5.0V & AVDD – 0.5 V)
VCI	I Power	Analog power supply (VCI : 2.5 ~ 3.3V)
VCI_REF	I Power	A Reference voltage for VCI. Must connect to VCI at FPC
VCI_OSC	I Power	Power supply for oscillator circuit. (VCI_OSC : 2.5 ~ 3.3V)
VCI_MDDI	I Power	Analog power supply (VCI_MDDI : 2.5 ~ 3.3V)
VSS	I Power	System ground. (0V)
VSS3	I Power	System ground level for I/O.
VSS_MDDI	I Power	System ground level for I/O
VSSC	I Power	System ground level for step up circuit block.
MTPG	I Power	Power supply for Non-volatile Memory. (19V) If MTP is not used, this pad should be floated.
MTPD	I Power	Power supply for Non-volatile Memory (16V) If MTP is not used, this pad should be floated.

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Table 9. Power supply pin description (continued)

Symbol	I/O	Description
VSS_OSC	I Power	System ground level for oscillator circuit.
AVSS	I Power	System ground level for source driver block.
VGS	I Power	Gamma ground level.
VCI1	O Power	A reference voltage in step-up circuit 1. Connect a capacitor for stabilization.
VCL	O Power	A power supply pin for generating VCOML. Connect a capacitor for stabilization.
VREFO	O	A reference voltage for GVDD, VCOMH, VCOML.
VCOM	O	A power supply for the TFT-display counter electrode. The M pin can set the alternating cycle. Connect this pin to the TFT-display counter electrode.
VCOMR	I/O	A reference voltage of VCOMH. When VCOMH is externally adjusted, halt the internal adjuster of VCOMH by setting the register and insert a variable resistor between GVDD and VSS. When this pin is not externally adjusted, leave it open and adjust VCOMH by setting the internal register.
VCOMH	O	This pin indicates a high level of VCOM that is generated from driving the VCOM alternation. Connect this pin to the capacitor for stabilization.
VCOML	O	When the VCOM alternation is driven, this pin indicates a low level of VCOM. An internal register can be used to adjust the voltage. Connect this pin to a capacitor for stabilization. At that time, take care of the polarity of capacitor for available voltage (-2 ~ 0V)
VGH	O Power	A positive power output pin for gate driver, internal step-up circuits, bias circuits, and operational amplifiers. Connect a capacitor for stabilization.

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Table 10. Power supply pin description (continued)

Symbol	I/O	Description
VGL	O Power	A Negative power output pin for gate driver, bias circuits, and operational amplifiers. Connect a capacitor for stabilization. To protect IC against Latch up, connect the cathode of the schottky diode to the VSS pad and the anode of the schottky diode to the VGL pad. Refer to the application circuit. Connect a capacitor for stabilization.
OSC1, OSC2	I/O	Connect an external resistor for R-C oscillation. When using DOTCLK, connect OSC1 pin to VSS3 and open OSC2 pin. When the external clock is given as input from outside, Apply the clock into OSC1 as the VCI voltage level (2.5 ~ 3.3V) and open OSC2 pin.
C11M, C11P C12M,C12P	-	Connect the step-up capacitor for generating the AVDD level. C12M & C12P can be used as an option only for high current consumption.
C21M, C21P C22M, C22P	-	Connect a step-up capacitor for generating the VGH, VGL level.
C31M, C31P	-	Connect a step-up capacitor for generating the VCL level.

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SYSTEM/EXTERNAL INTERFACE PIN

Table 11. System interface pin description

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>IM3-1, IM0/ID</td><td>I</td><td>Selects the MPU interface mode:
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0/ID</th><th>MPU interface mode</th><th>DB PIN assign</th></tr>
<tr><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td><td>68-system 16-bit bus interface</td><td>DB17-10, DB8-1</td></tr>
<tr><td>VSS</td><td>VSS</td><td>VSS</td><td>VDD3</td><td>68-system 8-bit bus interface</td><td>DB17-10</td></tr>
<tr><td>VSS</td><td>VSS</td><td>VDD3</td><td>VSS</td><td>80-system 16-bit bus interface</td><td>DB17-10, DB8-1</td></tr>
<tr><td>VSS</td><td>VSS</td><td>VDD3</td><td>VDD3</td><td>80-system 8-bit bus interface</td><td>DB17-10</td></tr>
<tr><td>VSS</td><td>VDD3</td><td>VSS</td><td>ID</td><td>Serial peripheral interface (SPI)</td><td>DB1-0</td></tr>
<tr><td>VSS</td><td>VDD3</td><td>VDD3</td><td>*</td><td>Non-selecting</td><td>-</td></tr>
<tr><td>VDD3</td><td>VSS</td><td>VSS</td><td>VSS</td><td>68-system 18-bit bus interface</td><td>DB17-0</td></tr>
<tr><td>VDD3</td><td>VSS</td><td>VSS</td><td>VDD3</td><td>68-system 9-bit bus interface</td><td>DB17-9</td></tr>
<tr><td>VDD3</td><td>VSS</td><td>VDD3</td><td>VSS</td><td>80-system 18-bit bus interface</td><td>DB17-0</td></tr>
<tr><td>VDD3</td><td>VSS</td><td>VDD3</td><td>VDD3</td><td>80-system 9-bit bus interface</td><td>DB17-9</td></tr>
<tr><td>VDD3</td><td>VDD3</td><td>VSS</td><td>*</td><td>MDDI interface</td><td>-</td></tr>
</table>
When a SPI mode is selected, the IM0 pin is used as ID setting bit for a device code.</td></tr>
<tr><td>CSB</td><td>I</td><td>Input pin for chip selection signal.
Low: S6D0139 is selected and can be accessed.
High: S6D0139 is not selected, and cannot be accessed.</td></tr>
<tr><td>RS</td><td>I</td><td>Register select pin.
Low: Index/status, High: Control
Must be fixed at VSS level, when this signal is not used.</td></tr>
<tr><td>RW_WRB/ SCL</td><td>I</td><td>
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>Pin function</th><th>MPU type</th><th>Pin description</th></tr>
<tr><td>*</td><td>VSS</td><td>VSS</td><td>RW</td><td>68-system</td><td>Read/Write operation selection pin.
Low: Write, High: Read</td></tr>
<tr><td>*</td><td>VSS</td><td>VDD3</td><td>WRB</td><td>80-system</td><td>Write strobe signal. (Input pin)
Data is fetched at the rising edge.</td></tr>
<tr><td>VSS</td><td>VDD3</td><td>VSS</td><td>SCL</td><td>Serial Peripheral Interface (SPI)</td><td>The synchronous clock signal.
(Input pin)</td></tr>
</table>
</td></tr>
<tr><td>E_RDB</td><td>I</td><td>
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>Pin function</th><th>MPU type</th><th>Pin description</th></tr>
<tr><td>*</td><td>VSS</td><td>VSS</td><td>E</td><td>68-system</td><td>Read/Write operation enable pin.</td></tr>
<tr><td>*</td><td>VSS</td><td>VDD3</td><td>RDB</td><td>80-system</td><td>Read strobe signal. (Input pin)
Read out data at the low level.</td></tr>
</table>
When SPI mode is selected, fix this pin at VSS level.</td></tr>
<tr><td>DB0/SDI</td><td>I/O</td><td>Bi-directional data bus.
18-bit interface: DB 17-0
16-bit interface: DB 17-10, DB 8-1
9-bit interface: DB 17-9
8-bit interface: DB 17-10
Fix DB0 to the VDD3 or VSS level, if the pin is not in use.
For a serial peripheral interface (SPI), input data is fetched at the rising edge of SCL signal.</td></tr>
<tr><td>RESETB</td><td>I</td><td>Reset pin. Initializes the IC, when this signal is low. Must be reset after the power is stable.
Note These three pins are connected together inside the chip. So when one is used as a reset pin, the other one should be left floating.</td></tr>
</table>

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Table 12. System interface pin description (Continued)

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>DB1/SDO/</td><td>I/O</td><td>Bi-directional data bus.
18-bit interface: DB 17-0
16-bit interface: DB 17-10, DB 8-1
9-bit interface: DB 17-9
8-bit interface: DB 17-10
Fix DB1 to the VDD3 or VSS level, if the pin is not in use.
For a serial peripheral interface (SPI), DB1/SDO serves as the serial data output pin. Successive bits are output at the falling edge of the SCL signal.</td></tr>
<tr><td>DB17-DB2</td><td>I/O</td><td>Bi-directional data bus.
18-bit interface: DB 17-0
16-bit interface: DB 17-10, DB 8-1
9-bit interface: DB 17-9
8-bit interface: DB 17-10
Fix unused pin to the VDD3 or VSS level.</td></tr>
<tr><td>ENABLE</td><td>I</td><td>Data enable signal pin for RGB interface.
EPL=”0”: Only in case of ENABLE=”Low”, the IC can be accessed via RGB interface.
EPL=”1”: Only in case of ENABLE=”High”, the IC can be accessed via RGB interface.
<table>
<tr><th>EPL</th><th>ENABLE</th><th>GRAM write</th><th>GRAM address</th></tr>
<tr><td>0</td><td>0</td><td>Valid</td><td>Updated</td></tr>
<tr><td>0</td><td>1</td><td>Invalid</td><td>Held</td></tr>
<tr><td>1</td><td>0</td><td>Invalid</td><td>Held</td></tr>
<tr><td>1</td><td>1</td><td>Valid</td><td>Updated</td></tr>
</table>
Fix ENABLE pin at VDD3 or VSS level, if the pin is not used.</td></tr>
<tr><td>GPIO[9:0]
(DB[12:3])</td><td>I/O</td><td>General purpose input/output</td></tr>
<tr><td>MDP</td><td>I/O</td><td>Positive MDDI data input/output. If MDDI is not used, this pad should be floated.</td></tr>
<tr><td>MDN</td><td>I/O</td><td>Negative MDDI data input/output. If MDDI is not used, this pad should be floated.</td></tr>
<tr><td>MSP</td><td>I</td><td>Positive MDDI strobe input. If MDDI is not used, this pad should be floated.</td></tr>
<tr><td>MSN</td><td>I</td><td>Negative MDDI strobe input. If MDDI is not used, this pad should be floated.</td></tr>
<tr><td>S_CSB /
DB2</td><td>O</td><td>Chip select for Sub Panel Driver IC
Low: Sub Panel Driver IC is selected and can be accessed.
High: Sub Panel Driver IC is not selected and can not be accessed.</td></tr>
<tr><td>S_RS /
DB1</td><td>O</td><td>Register select for Sub Panel Driver IC
Low : Index/status, High : Control
Must be fixed at VSS level, when this signal is not used.</td></tr>
<tr><td>S_WRB /
DB0</td><td>O</td><td>Write Strobe signal for Sub Panel Driver IC
Only 80-system 18/16 bit mode is enabled, so Data is fetched at the rising edge.</td></tr>
<tr><td>VSYNC</td><td>I</td><td>Synchronous signal of frame.
VSPL= “0”: Low active, VSPL=”1”: High active
Fix this pin at VDD3 or VSS level, if the pin is not used.</td></tr>
</table>

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HSYNC	I	Synchronous signal of line. HSPL="0": Low active, HSPL="1": High active Fix this pin at VDD3 or VSS level, if the pin is not used.
DOTCLK	I	Input pin for clock signal of external interface: dot clock. DPL="0": Display data is fetched at rising edge of DOTCLK. DPL="1": Display data is fetched at falling edge of DOTCLK. Fix this pin at VDD3 or VSS level, if the pin is not used.
PD17-PD0 /S_DB17-0	I	RGB data input bus. 18-bit interface: PD 17-0 16-bit interface: PD 17-13, PD 11-1 6-bit interface: PD 17-12 Fix unused pin to the VDD3 or VSS level. For Sub Panel, this pin can be used to transfer DB[17:0] data to Sub Panel Driver IC

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DISPLAY PIN

Table 13. Display pin description

Symbol	I/O	Description
S1 – S720	O	Source driver output pins. The SS bit can change the shift direction of the source signal. Example] If SS = 0, gray data of S1 is read from RAM address 0000h. If SS = 1, contents of RAM address 0000h is out from S720. S1, S4, S7, ... S (3n-1): display Red (R) (BGR = 0) S2, S5, S8, ... S (3n-2): display Green (G) (BGR = 0) S3, S6, S9, ... S (3n): display Blue (B) (BGR = 0)
G1 – G320	O	Gate driver output pins. The output of driving circuit is either VGH or VGL. VGH: gate-ON level VGL: gate-OFF level

MISCELLANEOUS PIN

Table 14. Oscillator and internal power regulator pin description

Symbol	I/O	Description
TEST_MODE0 TEST_MODE1 TEST_MODE2 TEST_MUX/ TEST_GRAY	I	Input pin for test. In normal operation, connect this pin to VSS3.
DISPTMG/M/ CL1/ESC/ FLM/ TSO1/TSO0/ PREC/EQ	O	Output pin for test. In normal operation, leave this pin open.
DUMMY	-	Dummy pin. Open or connect VSS3.

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FUNCTIONAL DESCRIPTION

SYSTEM INTERFACE

The S6D0139 has nine high-speed system interfaces: a 80-system 18-/16-/9-/8-bit bus, a 68-system 18-/16-/9-/8-bit bus, and a serial interface (SPI: Serial Peripheral Interface). The IM3-0 pins select the interface mode.
The S6D0139 has three 18-bit registers: an index register (IR), a write data register (WDR), and a read data register (RDR). The IR is a register to store index information from each control register. The WDR is a register that temporarily stores data to be written into each control register and GRAM. The RDR is a register to temporarily store data which is read from the GRAM. The data to be written to GRAM from MPU is once written to the WDR and then automatically written to GRAM by internal operation. Since the data is read from GRAM through the RDR, the data read out first is invalid and the data following that is read out normally.

Table 15. Register Selection (18-/16-/9-/8- Parallel Interface)

SYSTEM	RW_WRB	E_RDB	RS	Operations
68	0	1	0	Write index to IR
	1	1	0	Read internal status
	0	1	1	Write to control register and GRAM through WDR
	1	1	1	Read from GRAM through RDR
80	0	1	0	Write index to IR
	1	0	0	Read internal status
	0	1	1	Write to control register and GRAM through WDR
	1	0	1	Read from GRAM through RDR

Table 16. CSB signal (GRAM update control)

CSB	Operation
0	Data is written to GRAM, GRAM address is updated
1	Data is not written to GRAM, GRAM address is not updated

Table 17. Register Selection (Serial Peripheral Interface)

R/W bit	RS bit	Operation
0	0	Write index to IR
1	0	Read internal status
0	1	Write data to control register and GRAM through WDR
1	1	Read data from GRAM through RDR

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HIGH SPEED SERIAL INTERFACE (MDDI)

This interface will be introduced, see the section “Description of MDDI Interface”

SUB PANEL CONTROL

Sub panel control block will be introduced, see the section “Description of Sub Panel Control”

MIE FUNCTION

The S6D0139 has a special image enhancement function, MIE (Mobile Image Enhancement) which enhances the luminance/contrast adaptively by extracting the image’s brightness information and reduces power consumption of the backlight. When MIE enabled, the original image data is written on RAM after being enhanced. MIE is able to operate without regard to interface mode like either the RGB I/F or CPU I/F.

EXTERNAL INTERFACE (RGB-I/F, VSYNC-I/F)

The S6D0139 incorporates RGB and VSYNC interface as external interface for motion picture display.
When the RGB interface is selected, the synchronization signals (VSYNC, HSYNC, and DOTCLK) are available for display. The RGB data for display (PD17-0) is written according to enable signal (ENABLE) and data valid signal (VLD) in synchronization with VSYNC, HSYNC, and DOTCLK signal. This allows flicker-free updating of the screen.
When the VSYNC interface is selected, internal operation is normally synchronized with internal clock except for the operation related to frame synchronization: It is synchronized with the VSYNC signal. The data for display is written to GRAM via conventional system interface. There are some limitations on the timing and methods for writing to GRAM in VSYNC interface. See the section on the EXTERNAL DISPLAY INTERFACE.

ADDRESS COUNTER (AC)

The address counter (AC) assigns address to GRAM. When an address-set-instruction is written to the IR, the address information is sent from IR to AC. After writing to the GRAM, the address value of AC is automatically increased/ decreased by 1 according to ID1-0 bit of control register. After reading data from GRAM, the AC is not updated. A window address function allows data to be written only to a window area specified by GRAM.

GRAPHICS RAM (GRAM)

The graphics RAM (GRAM) has 18-bits/pixel and stores the bit-pattern data for 240-RGB x 320 dot display.

GRAYSCALE VOLTAGE GENERATOR

The grayscale voltage circuit generates a certain voltage level that is specified by the grayscale Υ-adjusting resistor for LCD driver circuit. By use of the generator, 262,144 colors can be displayed at the same time. For details, see the GAMMA-ADJUSTING RESISTOR section.

TIMING GENERATOR

The timing generator generates timing signals for the operation of internal circuits such as GRAM.
The GRAM read timing for display and the internal operation timing for MPU access is generated separately to avoid interference with one another. Several important timing signals can be monitored via signal monitoring pin (M, FLM, CL1, EQ, DISPTMG).

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OSCILLATION CIRCUIT (OSC)

The S6D0139 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pin. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulse can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the OSCILLATION CIRCUIT section.

SOURCE DRIVER CIRCUIT

The liquid crystal display source driver circuit consists of 720 drivers (S1 to S720).
Display pattern data is latched when 720-channel data has arrived. The latched data then enables the source drivers to generate drive waveform outputs. The SS bit can change the shift direction of 720-channel data by selecting an appropriate direction for the device-mounted configuration.

GATE DRIVER CIRCUIT

The liquid crystal display gate driver circuit consists of 320 gate drivers (G1 to G320).
The VGH or VGL level is output by the signal from the gate control circuit.

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SYSTEM/RGB INTERFACE AND GRAM ADDRESS SETTING

GRAM ADDRESS SETTING (SS="0")

When SS bit is 0 (source output shift direction: right) and BGR bit is 0 (RGB sequence: right), both of which can be set in R01h register, GRAM address is set as follows:

Table 18. GRAM address (SS="0")

S/G Output		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB 17 ..... DB 0			DB 17 ..... DB 0			DB 17 ..... DB 0			DB 17 ..... DB 0				DB 17 ..... DB 0			DB 17 ..... DB 0			DB 17 ..... DB 0			DB 17 ..... DB 0		
G1	G320	"0000"H			"0001"H			"0002"H			"0003"H			.....	"00EC"H			"00ED"H			"00EE"H			"00EF"H		
G2	G319	"0100"H			"0101"H			"0102"H			"0103"H			.....	"01EC"H			"01ED"H			"01EE"H			"01EF"H		
G3	G318	"0200"H			"0201"H			"0202"H			"0203"H			.....	"02EC"H			"02ED"H			"02EE"H			"02EF"H		
G4	G317	"0300"H			"0301"H			"0302"H			"0303"H			.....	"03EC"H			"03ED"H			"03EE"H			"03EF"H		
G5	G316	"0400"H			"0401"H			"0402"H			"0403"H			.....	"04EC"H			"04ED"H			"04EE"H			"04EF"H		
G6	G315	"0500"H			"0501"H			"0502"H			"0503"H			.....	"05EC"H			"05ED"H			"05EE"H			"05EF"H		
G7	G314	"0600"H			"0601"H			"0602"H			"0603"H			.....	"06EC"H			"06ED"H			"06EE"H			"06EF"H		
G8	G313	"0700"H			"0701"H			"0702"H			"0703"H			.....	"07EC"H			"07ED"H			"07EE"H			"07EF"H		
G9	G312	"0800"H			"0801"H			"0802"H			"0803"H			.....	"08EC"H			"08ED"H			"08EE"H			"08EF"H		
G10	G311	"0900"H			"0901"H			"0902"H			"0903"H			.....	"09EC"H			"09ED"H			"09EE"H			"09EF"H		
G11	G310	"0A00"H			"0A01"H			"0A02"H			"0A03"H			.....	"0AEC"H			"0AED"H			"0AEE"H			"0EEF"H		
G12	G309	"0B00"H			"0B01"H			"0B02"H			"0B03"H			.....	"0BEC"H			"0BED"H			"0BEE"H			"0BEF"H		
G13	G308	"0C00"H			"0C01"H			"0C02"H			"0C03"H			.....	"0CEC"H			"0CED"H			"0CEE"H			"0CEF"H		
G14	G307	"0D00"H			"0D01"H			"0D02"H			"0D03"H			.....	"0DEC"H			"0DED"H			"0DEE"H			"0DEF"H		
G15	G306	"0E00"H			"0E01"H			"0E02"H			"0E03"H			.....	"0EEC"H			"0EED"H			"0EEE"H			"0EEF"H		
G16	G305	"0F00"H			"0F01"H			"0F02"H			"0F03"H			.....	"0FEC"H			"0FED"H			"0FEE"H			"0FEF"H		
G17	G304	"1000"H			"1001"H			"1002"H			"1003"H			.....	"10EC"H			"10ED"H			"10EE"H			"10EF"H		
G18	G303	"1100"H			"1101"H			"1102"H			"1103"H			.....	"11EC"H			"11ED"H			"11EE"H			"11EF"H		
G19	G302	"1200"H			"1201"H			"1202"H			"1203"H			.....	"12EC"H			"12ED"H			"12EE"H			"12EF"H		
G20	G301	"1300"H			"1301"H			"1302"H			"1303"H			.....	"13EC"H			"13ED"H			"13EE"H			"13EF"H		
⋮	⋮	⋮			⋮			⋮			⋮				⋮			⋮			⋮			⋮		
G313	G8	"13800"H			"13801"H			"13802"H			"13803"H			.....	"138EC"H			"138ED"H			"138EE"H			"138EF"H		
G314	G7	"13900"H			"13901"H			"13902"H			"13903"H			.....	"139EC"H			"139ED"H			"139EE"H			"139EF"H		
G315	G6	"13A00"H			"13A01"H			"13A02"H			"13A03"H			.....	"13AEC"H			"13AED"H			"13AEE"H			"13AEF"H		
G316	G5	"13B00"H			"13B01"H			"13B02"H			"13B03"H			.....	"13BEC"H			"13BED"H			"13BEE"H			"13BEF"H		
G317	G4	"13C00"H			"13C01"H			"13C02"H			"13C03"H			.....	"13CEC"H			"13CED"H			"13CEE"H			"13CEF"H		
G318	G3	"13D00"H			"13D01"H			"13D02"H			"13D03"H			.....	"13DEC"H			"13DED"H			"13DEE"H			"13DEF"H		
G319	G2	"13E00"H			"13E01"H			"13E02"H			"13E03"H			.....	"13EEC"H			"13EED"H			"13EEE"H			"13EEF"H		
G320	G1	"13F00"H			"13F01"H			"13F02"H			"13F03"H			.....	"13FEC"H			"13FED"H			"13FEE"H			"13FEF"H		

Data fetch from GRAM for display when SS=0 is shown in the following figure.

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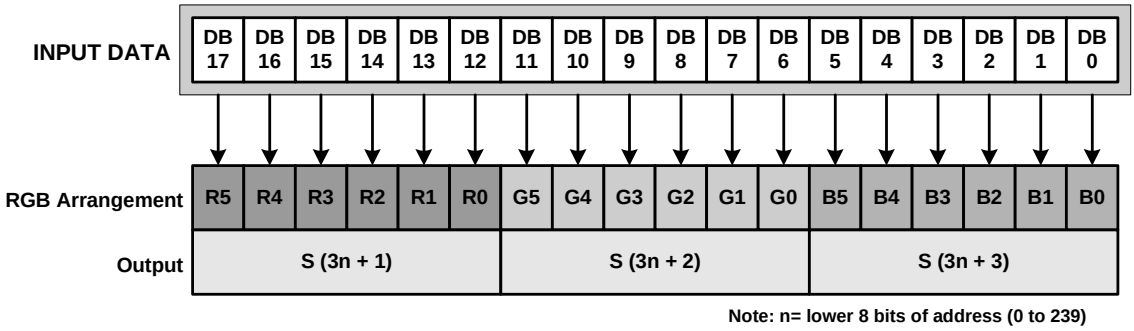
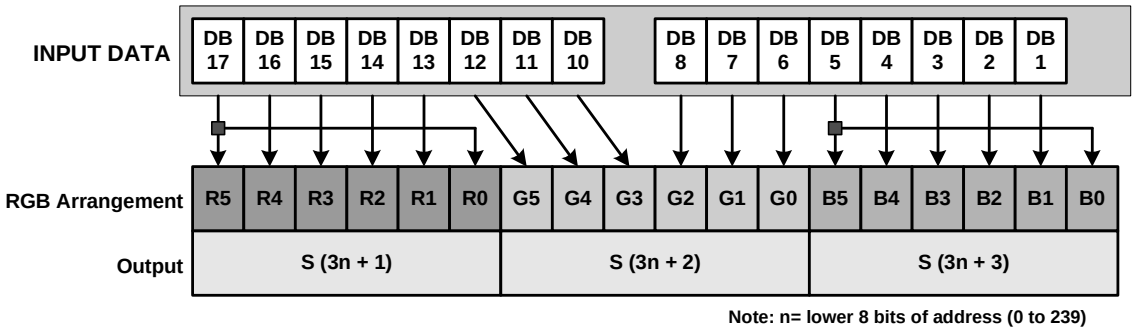
SYSTEM INTERFACE

68/80-system 18-bit interface (TRI=0, DFM=0)



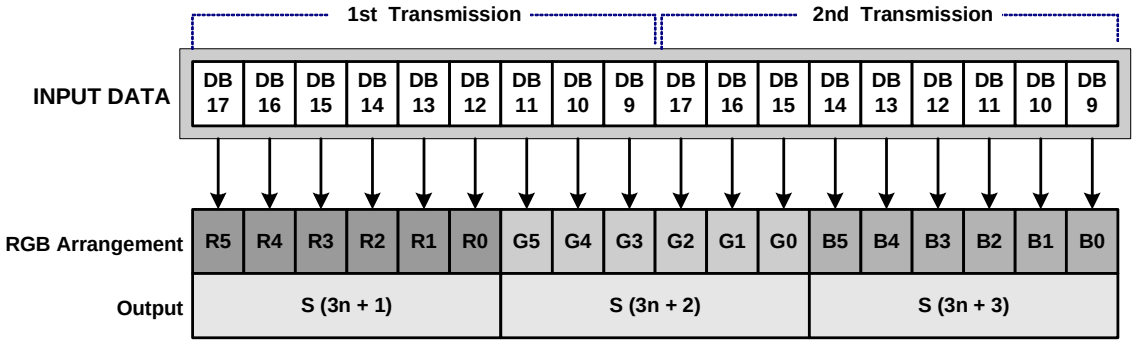
Note: n= lower 8 bits of address (0 to 239)

68/80-system 16-bit interface (TRI=0, DFM=0)



Note: n= lower 8 bits of address (0 to 239)

68/80-system 9-bit interface (TRI=0, DFM=0)



Note: n= lower 8 bits of address (0 to 239)

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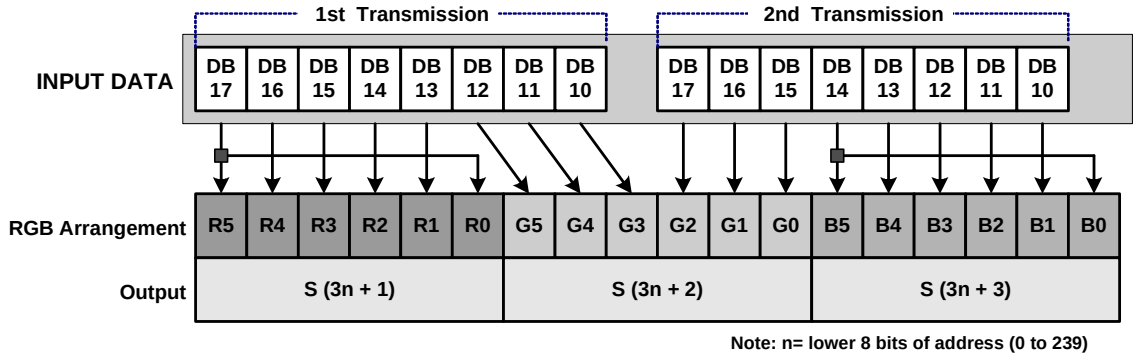
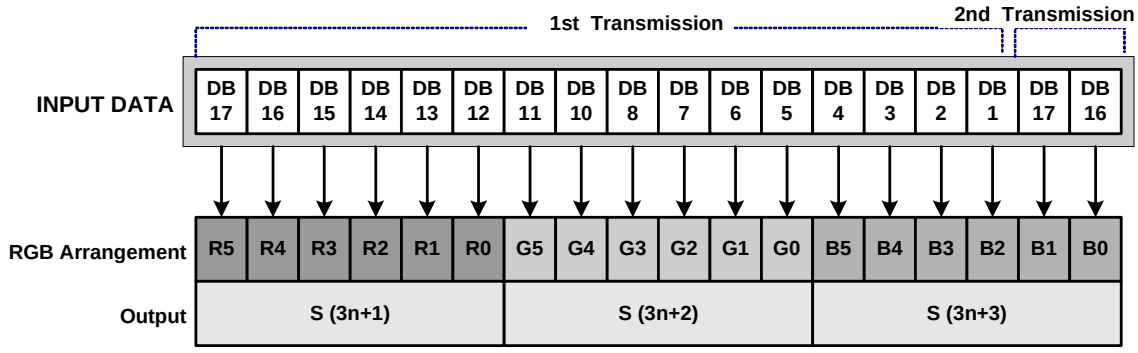
68/80-system 8-bit interface (TRI=0, DFM=0)



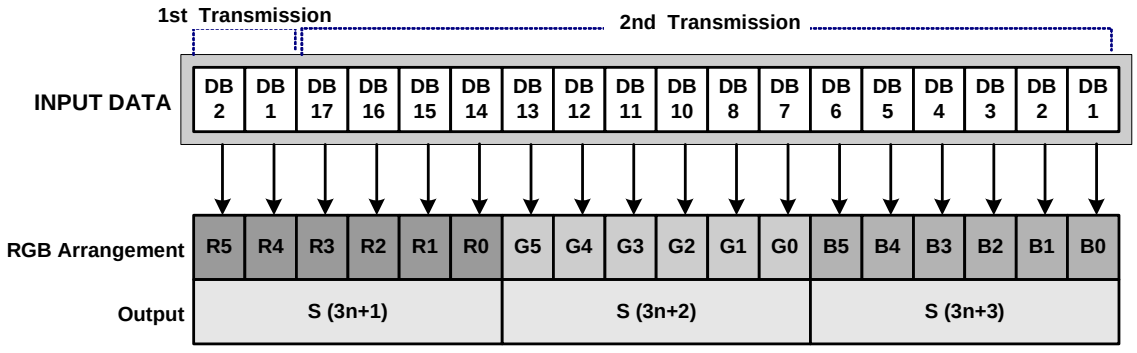
Note: n= lower 8 bits of address (0 to 239)

80-system 16-bit interface (TRI=1, DFM=0): 2 times transmission (262 K color)



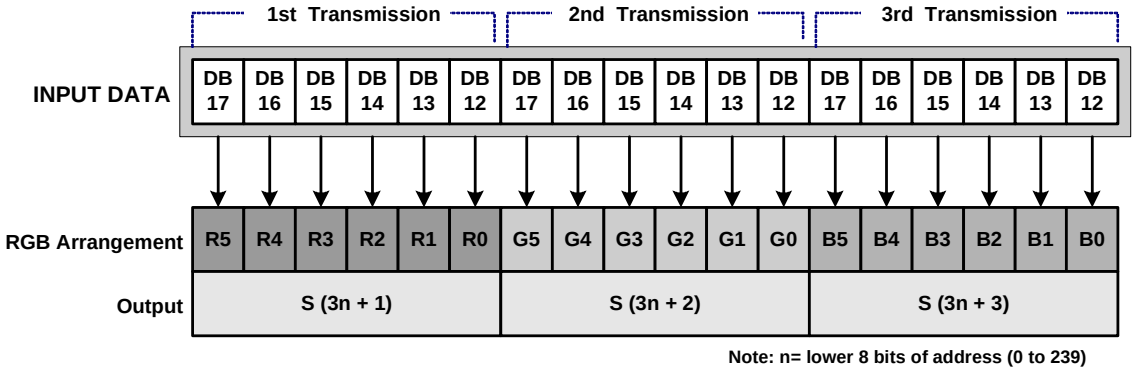
Note: n= lower 8 bits of address (0 to 239)

80-system 16-bit interface (TRI=1, DFM=1): 2 times transmission (262 K color)



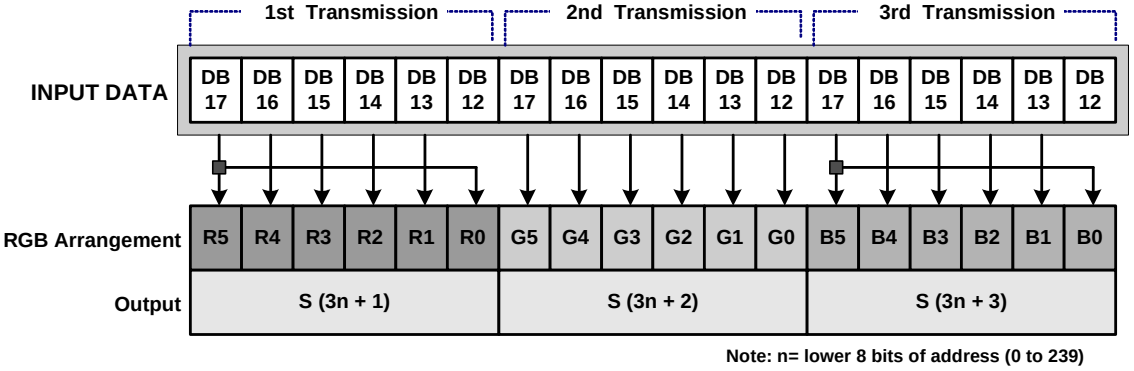
Note: n= lower 8 bits of address (0 to 239)

80-system 8-bit interface (TRI=1, DFM=0)



Note: n= lower 8 bits of address (0 to 239)

80-system 8-bit interface (TRI=1, DFM=1)



Note: n= lower 8 bits of address (0 to 239)

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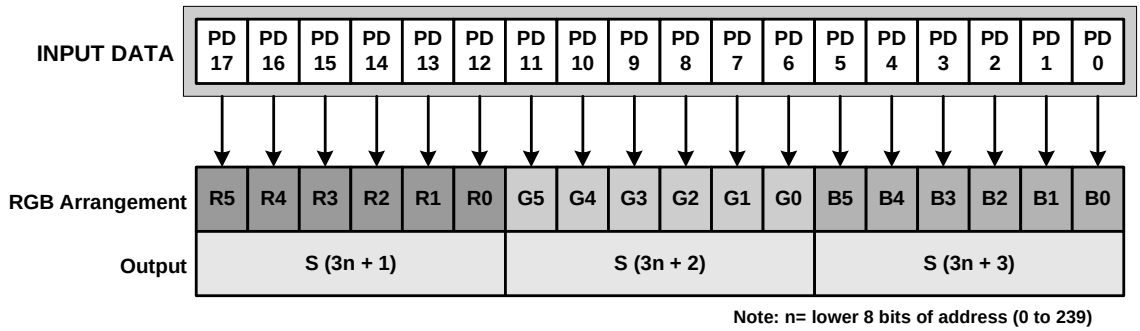
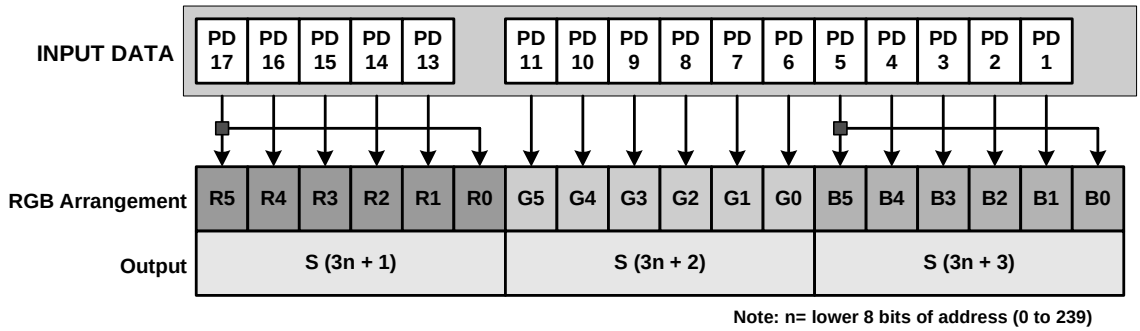
RGB INTERFACE

18-bit RGB interface



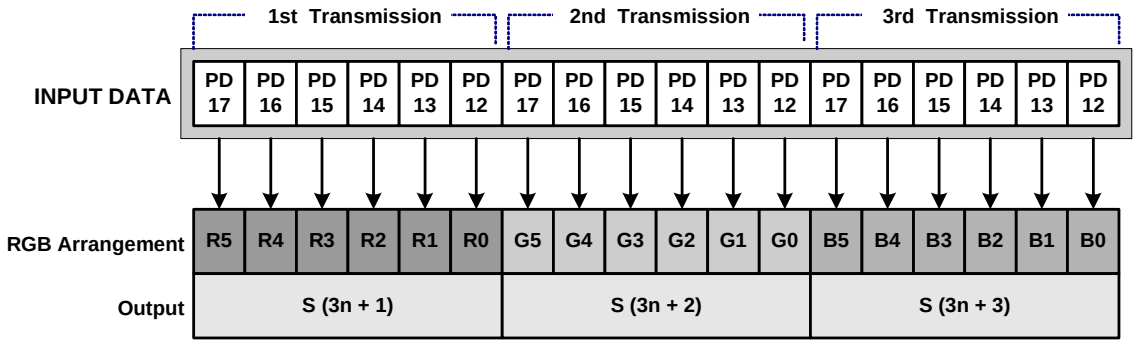
Note: n= lower 8 bits of address (0 to 239)

16-bit RGB interface



Note: n= lower 8 bits of address (0 to 239)

6-bit RGB interface



Note: n= lower 8 bits of address (0 to 239)

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GRAM ADDRESS SETTING (SS="1")

When SS bit is 1 (source output shift direction: reversed) and BGR bit is 1 (RGB sequence: reversed), which is set in R01h register, GRAM address is set as follows:

Table 19. GRAM address (SS="1")

S/G Output		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S709	S710	S711	S712	S713	S714	S715	S716	S717	S718	S719	S720
GS=0	GS=1	DB 0 ..... DB 17			DB 0 ..... DB 17			DB 0 ..... DB 17			DB 0 ..... DB 17				DB 0 ..... DB 17			DB 0 ..... DB 17			DB 0 ..... DB 17			DB 0 ..... DB 17		
G1	G320	"00EF"H			"00EE"H			"00ED"H			"00EC"H			.....	"0003"H			"0002"H			"0001"H			"0000"H		
G2	G319	"01EF"H			"01EE"H			"01ED"H			"01EC"H			.....	"0103"H			"0102"H			"0101"H			"0100"H		
G3	G318	"02EF"H			"02EE"H			"02ED"H			"02EC"H			.....	"0203"H			"0202"H			"0201"H			"0200"H		
G4	G317	"03EF"H			"03EE"H			"03ED"H			"03EC"H			.....	"0303"H			"0302"H			"0301"H			"0300"H		
G5	G316	"04EF"H			"04EE"H			"04ED"H			"04EC"H			.....	"0403"H			"0402"H			"0401"H			"0400"H		
G6	G315	"05EF"H			"05EE"H			"05ED"H			"05EC"H			.....	"0503"H			"0502"H			"0501"H			"0500"H		
G7	G314	"06EF"H			"06EE"H			"06ED"H			"06EC"H			.....	"0603"H			"0602"H			"0601"H			"0600"H		
G8	G313	"07EF"H			"07EE"H			"07ED"H			"07EC"H			.....	"0703"H			"0702"H			"0701"H			"0700"H		
G9	G312	"08EF"H			"08EE"H			"08ED"H			"08EC"H			.....	"0803"H			"0802"H			"0801"H			"0800"H		
G10	G311	"09EF"H			"09EE"H			"09ED"H			"09EC"H			.....	"0903"H			"0902"H			"0901"H			"0900"H		
G11	G310	"0EEF"H			"0AEE"H			"0AED"H			"0AEC"H			.....	"0A03"H			"0A02"H			"0A01"H			"0A00"H		
G12	G309	"0BEF"H			"0BEE"H			"0BED"H			"0BEC"H			.....	"0B03"H			"0B02"H			"0B01"H			"0B00"H		
G13	G308	"0CEF"H			"0CEE"H			"0CED"H			"0CEC"H			.....	"0C03"H			"0C02"H			"0C01"H			"0C00"H		
G14	G307	"0DEF"H			"0DEE"H			"0DED"H			"0DEC"H			.....	"0D03"H			"0D02"H			"0D01"H			"0D00"H		
G15	G306	"0EEF"H			"0EEE"H			"0EED"H			"0EEC"H			.....	"0E03"H			"0E02"H			"0E01"H			"0E00"H		
G16	G305	"0FEF"H			"0FEE"H			"0FED"H			"0FEC"H			.....	"0F03"H			"0F02"H			"0F01"H			"0F00"H		
G17	G304	"10EF"H			"10EE"H			"10ED"H			"10EC"H			.....	"1003"H			"1002"H			"1001"H			"1000"H		
G18	G303	"11EF"H			"11EE"H			"11ED"H			"11EC"H			.....	"1103"H			"1102"H			"1101"H			"1100"H		
G19	G302	"12EF"H			"12EE"H			"12ED"H			"12EC"H			.....	"1203"H			"1202"H			"1201"H			"1200"H		
G20	G301	"13EF"H			"13EE"H			"13ED"H			"13EC"H			.....	"1303"H			"1302"H			"1301"H			"1300"H		
⋮	⋮	⋮			⋮			⋮			⋮				⋮			⋮			⋮			⋮		
G313	G8	"138EF"H			"138EE"H			"138ED"H			"138EC"H			.....	"13803"H			"13802"H			"13801"H			"13800"H		
G314	G7	"139EF"H			"139EE"H			"139ED"H			"139EC"H			.....	"13903"H			"13902"H			"13901"H			"13900"H		
G315	G6	"13AEF"H			"13AEE"H			"13AED"H			"13AEC"H			.....	"13A03"H			"13A02"H			"13A01"H			"13A00"H		
G316	G5	"13BEF"H			"13BEE"H			"13BED"H			"13BEC"H			.....	"13B03"H			"13B02"H			"13B01"H			"13B00"H		
G317	G4	"13CEF"H			"13CEE"H			"13CED"H			"13CEC"H			.....	"13C03"H			"13C02"H			"13C01"H			"13C00"H		
G318	G3	"13DEF"H			"13DEE"H			"13DED"H			"13DEC"H			.....	"13D03"H			"13D02"H			"13D01"H			"13D00"H		
G319	G2	"13EEF"H			"13EEE"H			"13EED"H			"13EEC"H			.....	"13E03"H			"13E02"H			"13E01"H			"13E00"H		
G320	G1	"13FEF"H			"13FEE"H			"13FED"H			"13FEC"H			.....	"13F03"H			"13F02"H			"13F01"H			"13F00"H		

Data fetch from GRAM for display when SS=1 is shown in the following figure.

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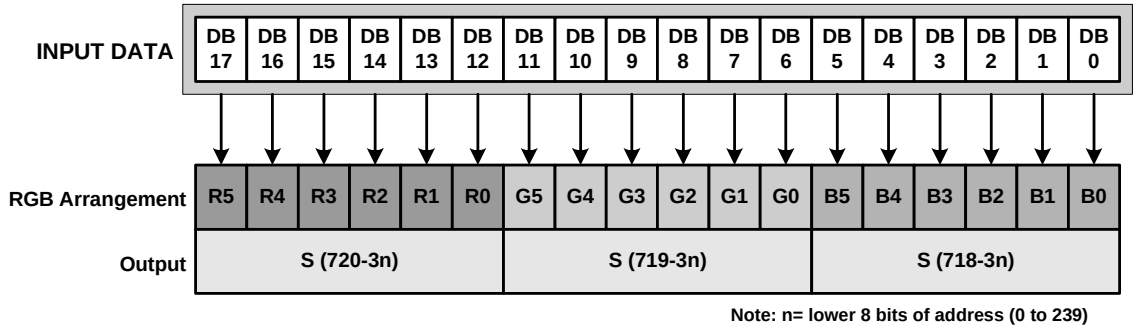
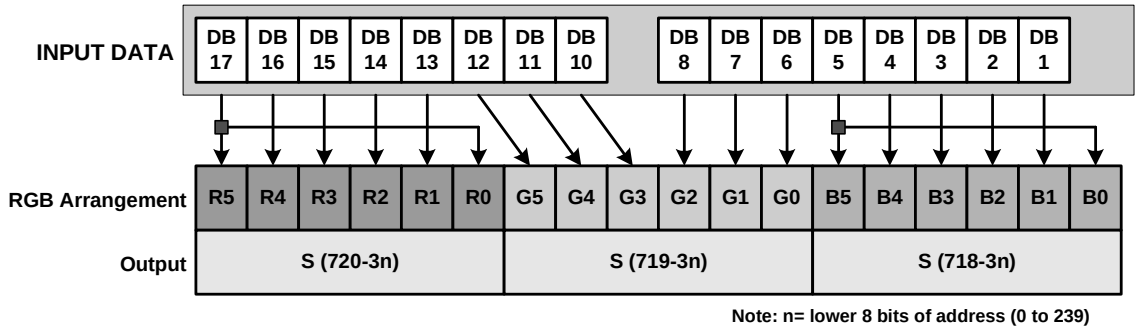
SYSTEM INTERFACE

68/80-system 18-bit interface (TRI=0, DFM=0)



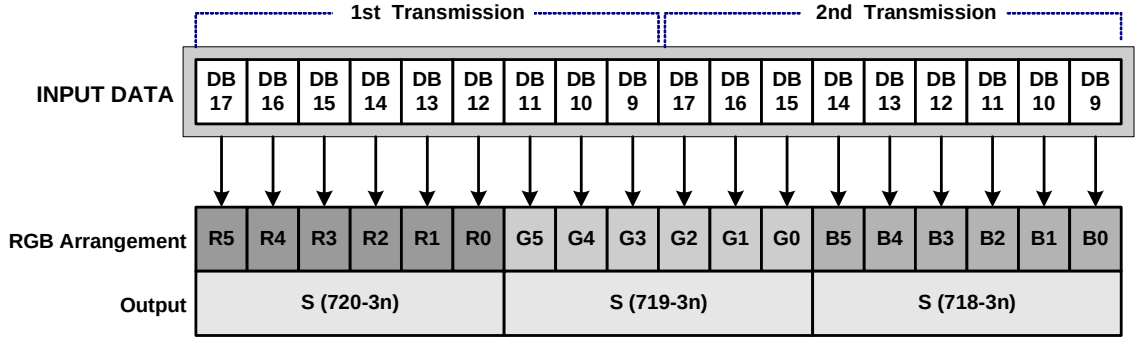
Note: n= lower 8 bits of address (0 to 239)

68/80-system 16-bit interface (TRI=0, DFM=0)



Note: n= lower 8 bits of address (0 to 239)

68/80-system 9-bit interface (TRI=0, DFM=0)



Note: n= lower 8 bits of address (0 to 239)

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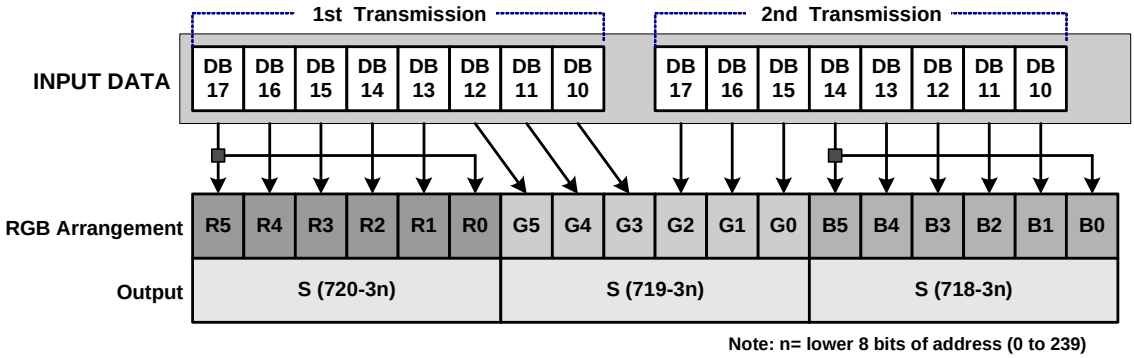
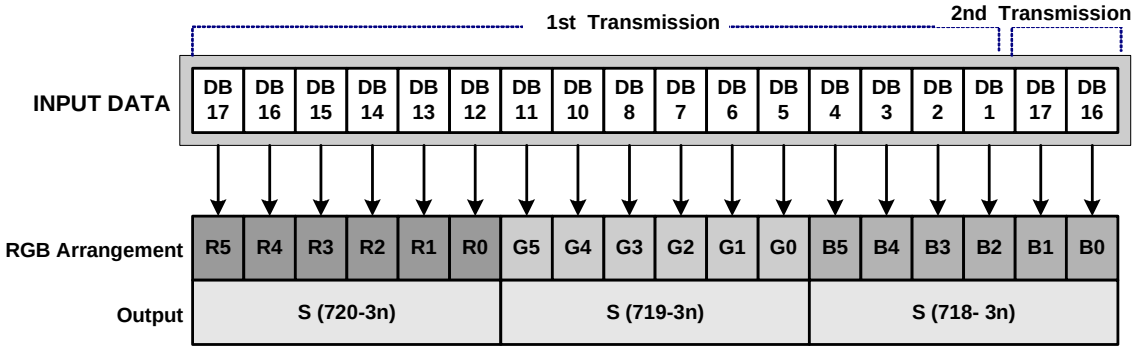
68/80-system 8-bit interface (TRI=0, DFM=0)



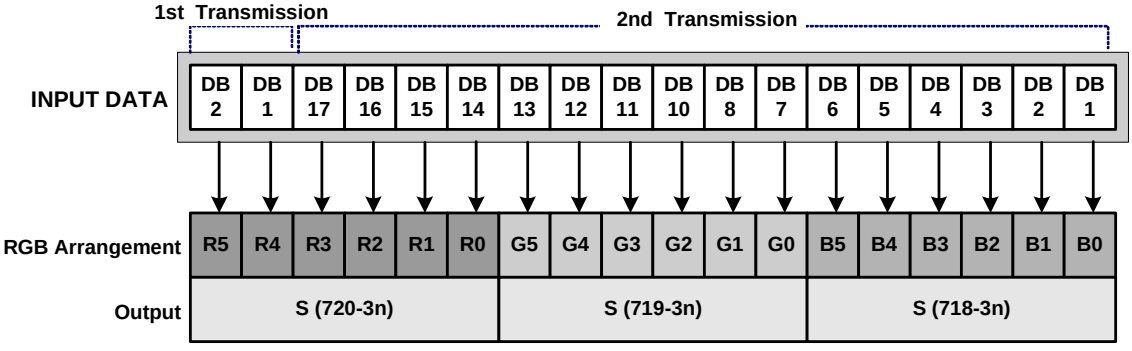
Note: n= lower 8 bits of address (0 to 239)

80-system 16-bit interface (TRI=1, DFM=0): 2 times transmission (262 K color)



Note: n= lower 8 bits of address (0 to 239)

80-system 16-bit interface (TRI=1, DFM=1): 2 times transmission (262 K color)



Note: n= lower 8 bits of address (0 to 239)

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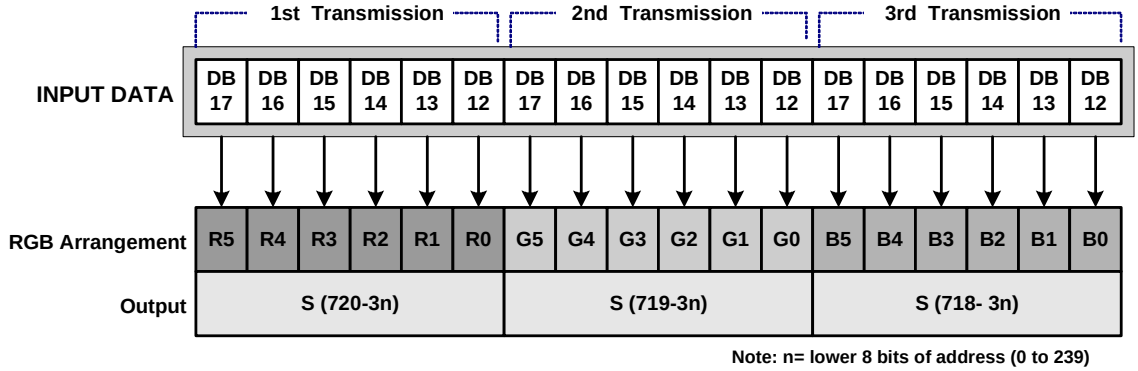
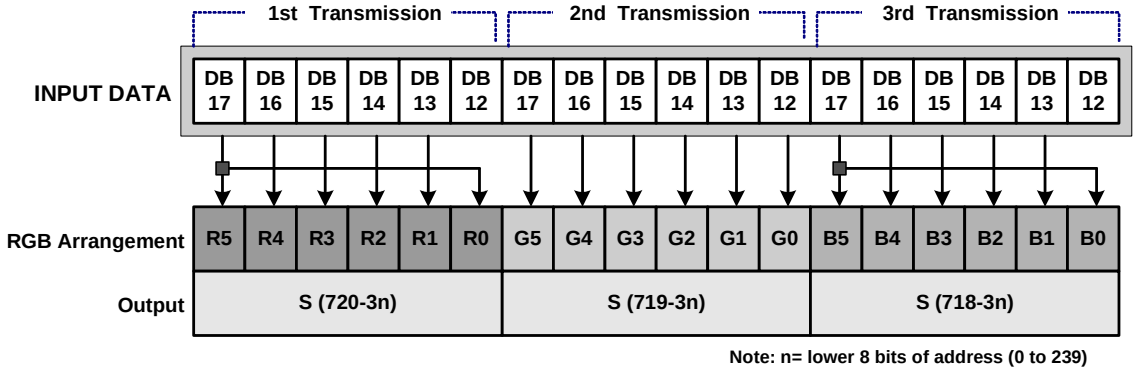
80-system 8-bit interface (TRI=1, DFM=0): 3 times transmission (262 K color)



Note: n= lower 8 bits of address (0 to 239)

80-system 8-bit interface (TRI=1, DFM=1): 3 times transmission (65 K color)



Note: n= lower 8 bits of address (0 to 239)

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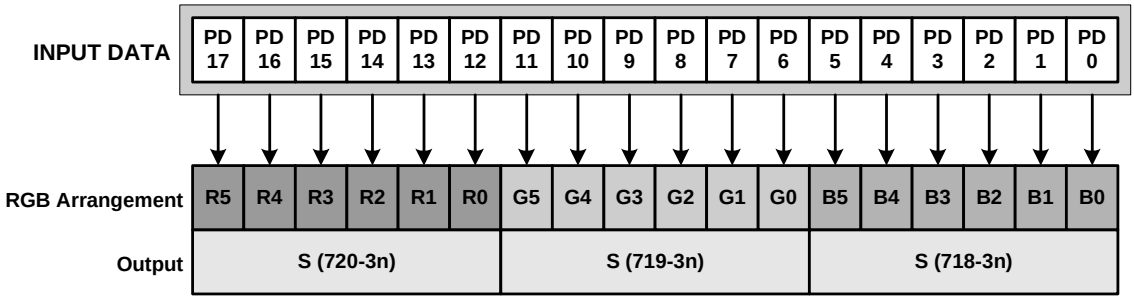
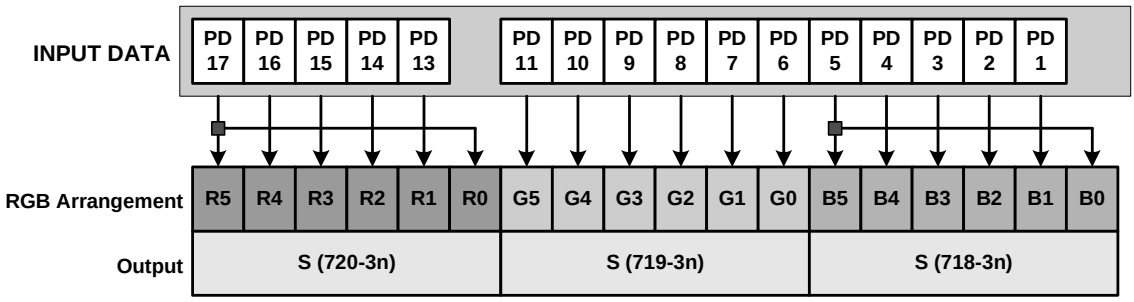
RGB INTERFACE

18-bit interface



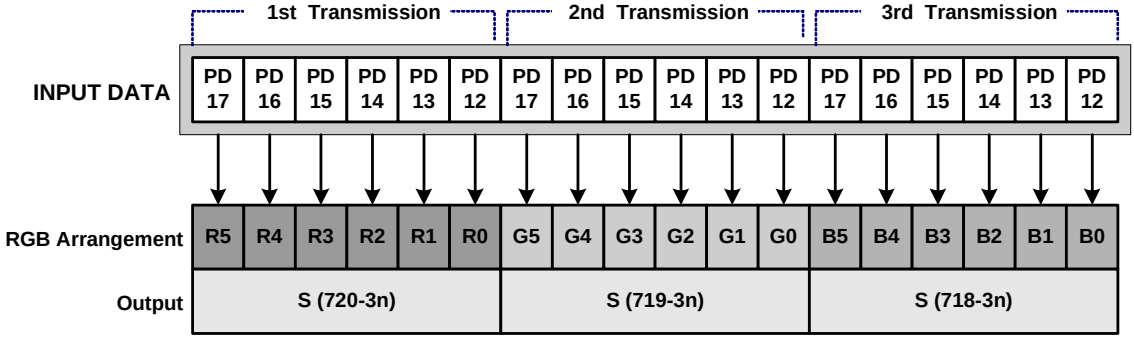
Note: n= lower 8 bits of address (0 to 239)

16-bit interface



Note: n= lower 8 bits of address (0 to 239)

6-bit interface



Note: n= lower 8 bits of address (0 to 239)

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INSTRUCTIONS

The S6D0139 uses the 18-bit bus architecture. Before the internal operation of the S6D0139 starts, control information is temporarily stored in the registers described below to allow high-speed interfacing with a high-performance microcomputer. The internal operation of the S6D0139 is determined by signals sent from the microcomputer. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signals (DB17 to DB0), make up the S6D0139 instructions.
There are nine categories of instructions that:

- Specify the index
- Read the status
- Control the display
- Control power management
- Set internal GRAM addresses
- Transfer data to and from the internal GRAM
- Set grayscale level for the internal grayscale palette table
- Interface with the gate driver and power supply IC

Normally, instructions that write data are used the most. However, an auto-update of internal GRAM addresses after each data write can lighten the microcomputer program load. As instructions are executed in 0 cycles, they can be written in succession.

The 16-bit instruction assignment differs from interface-setup (18-/16-/9-/8-/SPI), so instructions should be fetched according to the data format shown below:

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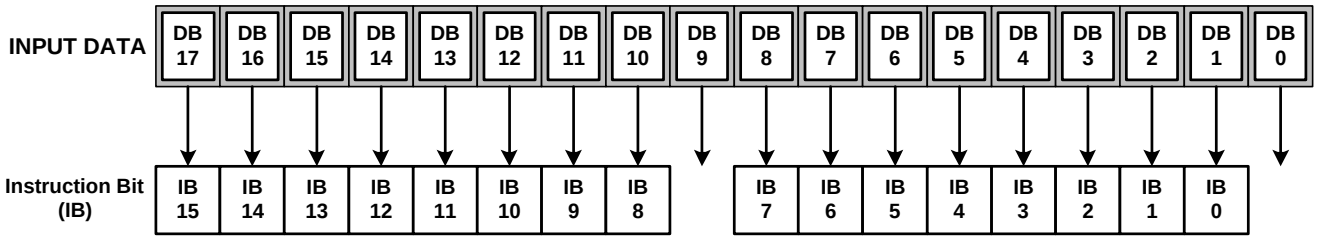
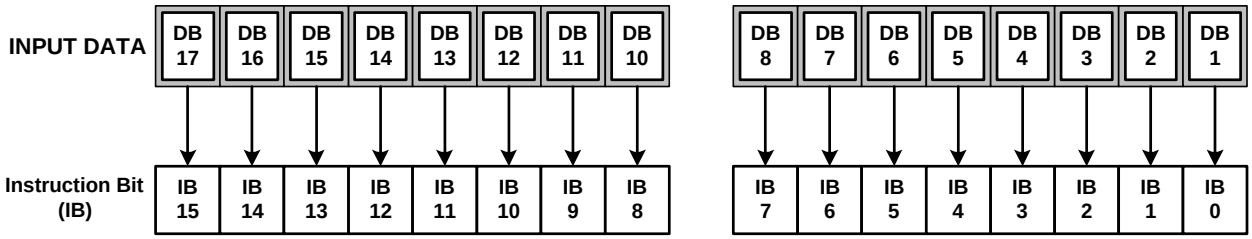
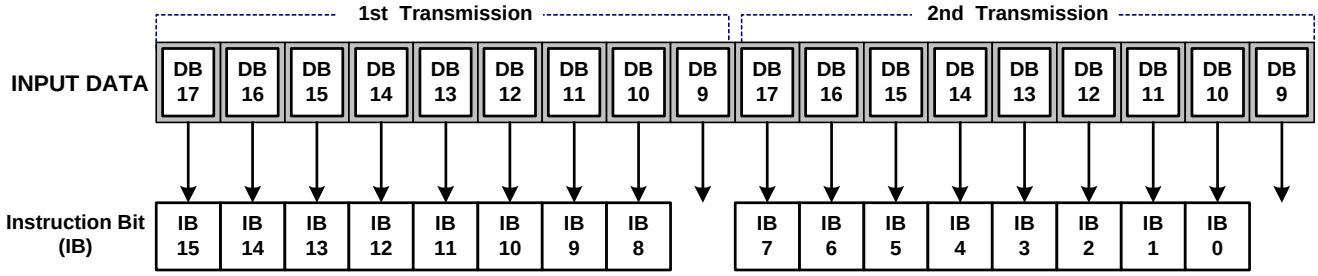
68/80-system 18-bit Interface



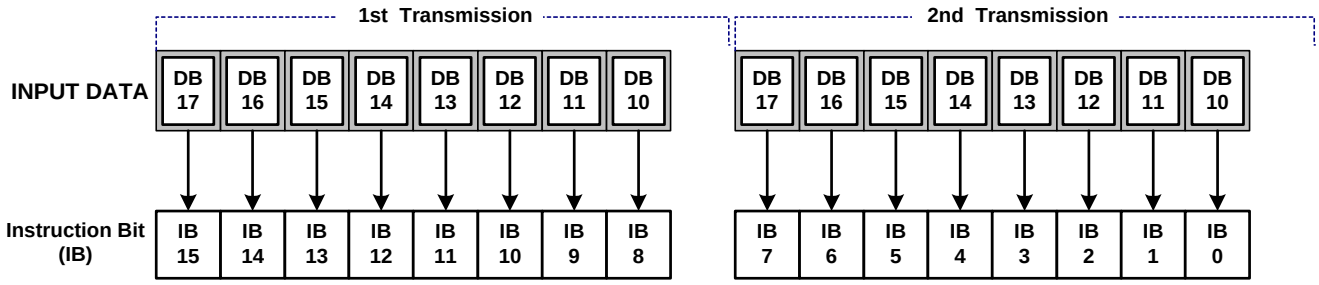
68/80-system 16-bit Interface



68/80-system 9-bit Interface



68/80-system 8-bit Interface/SPI



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INSTRUCTION TABLE

Table 20. Instruction Table

Reg. No	R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0	Register Name / Description
IR	0	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	**Index /** Sets the index register value
SR	1	0	0	0	0	0	0	0	0	L8	L7	L6	L5	L4	L3	L2	L1	L0	**Status read /** Reads the internal status of the S6D0139
R00h	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	**Start oscillation(R00H) /** Starts the oscillation circuit
	1	1	0	0	0	0	0	0	0	1	0	0	1	1	1	0	0	1	**Device code read /** Read 0139H
R01h	0	1	0	VSPL	HSPL	DPL	EPL	SM	GS	SS	0	0	NL5	NL4	NL3	NL2	NL1	NL0	**Driver output control(R01H) /** VSPL: set polarity of VSYNC pin. HSPL: set polarity of HSYNC pin. DPL: set polarity of DOTCLK pin. EPL: set polarity of ENABLE pin SM: gate driver division drive control GS: gate driver shift direction SS: source driver shift direction NL5-0: number of driving lines
R02h	0	1	0	0	0	0	FLD1	FLD0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0	**LCD-Driving-waveform control (R02H)/** FLD1-0: number of interlaced field B/C: LCD drive AC waveform EOR: Exclusive OR-ing the AC waveform NW5-0: n raster row inversion
R03h	0	1	TRI	DFM	0	BGR	0	0	0	0	0	0	I/D1	I/D0	0	0	0	0	**Entry mode(R03H) /** TRI: 8-bit interface mode DFM: defines color depth for the IC BGR: RGB swap control I/D1-0: address counter Increment / Decrement control
R07h	0	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	0	GON	CL	REV	D1	D0	**Display control (R07H) /** PT1-0: Non-display area source output control VLE2-1: 1st /2nd partial vertical scroll SPT: 1st /2nd partial display enable GON: gate on/off control CL: 8-color display mode enable REV: display area inversion drive D1-0: source output control
R08h	0	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0	**Blank period control 1 (R08H)/** FP3-0: Front porch setting BP3-0: Back porch setting
R0Bh	0	1	NO1	NO0	SDT1	SDT0	ECS2	ECS1	ECS0	DIV1	DIV0	0	DCR_EX	DCR2	DCR1	DCR0	RTN1	RTN0	**Frame cycle control (R0BH)/** NO1-0: specify the amount of non-overlap SDT1-0: set amount of source delay ECS2-0: VCI recycling period setting DIV1-0: division ratio of internal clock setting DCR_EX: Input signal selection. DCR2-0:Set clock cycle for step-up circuit. RTN20: set the 1-H period
R0Ch	0	1	0	0	0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0	**External interface control(R0CH) /** RM: specify the interface for RAM access DM1-0: specify display operation mode RIM1-0: specify RGB-I/F mode
R10h	0	1	BT3	0	SAP2	SAP1	SAP0	BT2	BT1	BT0	DC2	DC1	DC0	0	0	0	SLP	STB	**Power control 1 (R10H) /** SAP2-0:Adjust fixed current BT2-0:Adjust scale factor BT3:Support VGH/VGL(-6Vci~6Vci) DC2-0:Adjust the frequency SLP: sleep mode control STB: standby mode control
R11h	0	1	0	0	GVD5	GVD4	GVD3	GVD2	GVD1	GVD0	0	0	0	0	0	VC2	VC1	VC0	**Power control 2 (R11H)/** GVD5-0:set GVDD voltage VC2-0:set VCI1 voltage
R13h	0	1	0	0	0	0	0	0	0	0	0	PON	PON1	AON	0	0	0	0	**Power control 3 (R13H)/** PON: booster circuit control PON1: booster circuit control AON: operation start bit for the amplifier.
R14h	0	1	0	VCMR	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	0	0	VML5	VML4	VML3	VML2	VML1	VML0	**Power control 4 (R14H)/** VCMR: VCOMH control VCM5-0:set the VCOMH voltage VML5-0:set the amplitude of VCOM voltage
R15h	0	1	0	0	0	0	0	0	0	0	FCV_EN	0	0	0	MPU_MODE	STN_EN	SUB_IM1	SUB_IM0	**Sub panel control (R15H)** SUB_IM1-0 interface mode STN_EN: set the panel MPU_MODE: set mpu_mode FCV_EN: format conversion

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Table 21. Instruction Table (Continued)

Reg. No	R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0	Register Name / Description
R20h	0	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	**RAM address set (R20H&R21H)/** AD16-0: Set GRAM address.
R21h	0	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	
R22h	0	1	**WD17-0 : Pin assignment varies according to the interface method**																**Write data to GRAM (R22H)/** WD17-0:Input data for GRAM
	1	1	**RD17-0 : Pin assignment varies according to the interface method**																**Read data from GRAM (R22H)/** RD17-0:Read data from GRAM
R30h	0	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	RATIOP02	RATIOP01	RATIOP00	0	0	PKP 02	PKP 01	PKP 00	**Gamma control 1 (R30H)/** Adjust Gamma voltage
R31h	0	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	RATIOP12	RATIOP11	RATIOP10	0	0	PKP 22	PKP 21	PKP 20	**Gamma control 2 (R31H)/** Adjust Gamma voltage
R32h	0	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40	**Gamma control 3 (R32H)/** Adjust Gamma voltage
R33h	0	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00	**Gamma control 4 (R33H)/** Adjust Gamma voltage
R34h	0	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	RATION02	RATION01	RATION00	0	0	PKN 02	PKN 01	PKN 00	**Gamma control 5 (R34H)/** Adjust Gamma voltage
R35h	0	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	RATION12	RATION11	RATION10	0	0	PKN 22	PKN 21	PKN 20	**Gamma control 6 (R35H)/** Adjust Gamma voltage
R36h	0	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0-	0	0	0	0	PKN 42	PKN 41	PKN 40	**Gamma control 7 (R36H)/** Adjust Gamma voltage
R37h	0	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00	**Gamma control 8 (R37H)/** Adjust Gamma voltage
R38h	0	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00	**Gamma control 9 (R38H)/** Adjust Amplitude voltage
R39h	0	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00	**Gamma control 10 (R39H)/** Adjust Amplitude voltage
R40h	0	1	0	0	0	0	0	0	0	0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0	**Gate scan position (R40H)/** SCN5-0: scan starting position of gate
R41h	0	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	**Vertical scroll control (R41H)/** VL8-0:
R42h	0	1	0	0	0	0	0	0	0	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	**1st screen driving position (R42H, R43H)** SE18-10: 1st screen end position SS18-10: 1st screen start position
R43h	0	1	0	0	0	0	0	0	0	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10	
R44h	0	1	0	0	0	0	0	0	0	SE28	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	**2nd screen driving position (R44H, R45H)** SE28-20: 2nd screen end position SS28-20: 2nd screen start position
R45h	0	1	0	0	0	0	0	0	0	SS28	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20	
R46h	0	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0	**Horizontal window address (R46H)** HSA7-0: Horizontal window address start position HEA7-0: Horizontal window address end position
R47h	0	1	0	0	0	0	0	0	0	VEA8	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	**Vertical window Address (R47H, R48H)** VEA8-0: Vertical window address end position VSA8-0: Vertical window address start position
R48h	0	1	0	0	0	0	0	0		VSA8	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	
R50h	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VWAKE_EN	When VWAKE_EN = 1, client initiated wakeup is enabled.
R51h	0	1	WKL8	WKL7	WKL6	WKL5	WKL4	WKL3	WKL2	WKL1	WKL0	0	WKF3	WKF2	WKF1	WKF0	0	0	**WKF** : The frame that data is written **WKL** : The line that data is written
R60h	0	1	0	0	0	0	0	0	0	0	SUB_SEL								**Sub panel selection index** SUB_SEL: select main/sub panel
R61h	0	1	0	0	0	0	0	0	0	0	SUB_WR								**Sub panel data write index** SUB_WR: GRAM write data sub frame
R71h	0	1	Test command1																**Don't use this command**
R72h	0	1	Test command2																**Don't use this command**
R73h	0	1	MIE_MODE[1]	MIE_MODE[0]	SEL_TABLE[1]	SEL_TABLE[0]	MIE_S_M	0	0	0	0	0	0	0	MIE_GAMMA[3]	MIE_GAMMA[2]	MIE_GAMMA[1]	MIE_GAMMA[0]	**MIE function(R73h)**
R75h	0	1	0	0	0	0	0	0	GPIO[9]	GPIO[8]	GPIO[7]	GPIO[6]	GPIO[5]	GPIO[4]	GPIO[3]	GPIO[2]	GPIO[1]	GPIO[0]	**GPIO value(R75H)** GPIO 9-0
R76h	0	1	0	0	0	0	0	0	GPIO_CON[9]	GPIO_CON[8]	GPIO_CON[7]	GPIO_CON[6]	GPIO_CON[5]	GPIO_CON[4]	GPIO_CON[3]	GPIO_CON[2]	GPIO_CON[1]	GPIO_CON[0]	**GPIO in/output control(R76H)** GPIO 9-0
R77h	0	1	0	0	0	0	0	0	GPLCR[9]	GPLCR[8]	GPLCR[7]	GPLCR[6]	GPLCR[5]	GPLCR[4]	GPLCR[3]	GPLCR[2]	GPLCR[1]	GPLCR[0]	**GPIO Clear(R77H)** GPCLR 9-0
R78h	0	1	0	0	0	0	0	0	GPIO_EN[9]	GPIO_EN[8]	GPIO_EN[7]	GPIO_EN[6]	GPIO_EN[5]	GPIO_EN[4]	GPIO_EN[3]	GPIO_EN[2]	GPIO_EN[1]	GPIO_EN[0]	**GPIO interrupt enable(R78H)** GPIO_EN 9-0
R79h	0	1	0	0	0	0	0	0	GPPOL[9]	GPPOL[8]	GPPOL[7]	GPPOL[6]	GPPOL[5]	GPPOL[4]	GPPOL[3]	GPPOL[2]	GPPOL[1]	GPPOL[0]	**GPIO polarity selection (R79H)** GPPOL 9-0

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Reg. No	R/W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0	Register Name / Description
R90h	W	1	0	0	0	0	0	0	0	0	0	0	0	0	MTP_ LOAD	MTP_ WRB	MTP_ SELB	MTP_I NI	**MTP INIT(R90h)** MTP_LOAD: MTP data load. MTP_WRB**:** MTP program enable signal MTP_SELB : VCOMH selection MTP_INI: MTP initial mode control
R91h	W	1	0	0	0	0	0	0	0	0	0	D6	D5	D4	D3	D2	D1	D0	**MTP VCOMH read(R91h)** Dummy:
R92h	W	1	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0	**Set MTP Test Key(R94h)** 8Ch

INSTRUCTION DESCRIPTIONS

Index

The index instruction specifies the RAM control indexes (R00h to R94h). It sets the register number in the range of 0000000 to 11111111 in binary form. However, R71h to R72h are used for test registers.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Status Read

The status read instruction reads out the internal status of the IC.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	0	0	0	0	0	0	0	L8	L7	L6	L5	L4	L3	L2	L1	L0

L8–0: Indicate the driving raster-row position where the liquid crystal display is being driven.

Start Oscillation (R00h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	0	0	0	0	0	0	1	0	0	1	1	1	0	0	1

The start oscillation instruction restarts the oscillator from the Halt State in the stand-by mode. After this instruction, wait for at least 10 ms for the oscillation to stabilize before giving the next instruction.
(See the Power Control 1 Register (R10h))

If this register is read forcibly, *0139h is read.

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DRIVER OUTPUT CONTROL (R01H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	VSPL	HSPL	DPL	EPL	SM	GS	SS	0	0	NL5	NL4	NL3	NL2	NL1	NL0

VSPL: reverses the polarity of the VSYNC signal.
VSPL= “0”: VSYNC is low active.
VSPL= “1”: VSYNC is high active.

HSPL: reverses the polarity of the HSYNC signal.
HSPL= “0”: HSYNC is low active.
HSPL= “1”: HSYNC is high active.

DPL: reverses the polarity of the DOTCLK signal.
DPL= “0”: Display data is fetched on the rising edge of DOTCLK.
DPL= “1”: Display data is fetched on the falling edge of DOTCLK.

EPL: Set the polarity of ENABLE pin while using RGB interface.

EPL = “0”: ENABLE = ”Low” / write data of PD17-0
ENABLE = ”High” / don’t write data of PD17-0
EPL = “1”: ENABLE = ”High” / write data of PD17-0
ENABLE = ”Low” / don’t write data of PD17-0

Table 22. Relationship between EPL, ENABLE and RAM access

EPL	ENABLE	RAM write	RAM address
0	0	Valid	Updated
0	1	Invalid	Held
1	1	Valid	Updated
1	0	Invalid	Held

GS: Selects the output shift direction of the gate driver. When GS = 0, G1 shifts to G320. When GS = 1, G320 shifts to G1.

SM: Select the division drive method of the gate driver. When SM = 0, even/odd division is selected; SM = 1, upper/lower division drive is selected. Various connections between TFT panel and the IC can be supported with the combination of SM and GS bit.

SS: Selects the output shift direction of the source driver. When SS = 0, S1 shifts to S720. When SS = 1, S720 shifts to S1. In addition, SS and BGR bits should be specified in case of any change in the RGB order. When SS = 0 and BGR = 0, <R><G><B> are assigned in order from S1 pin. When SS = 1 and BGR = 1, <R><G><B> are assigned in order from S720. Re-write data to GRAM whenever SS and BGR bit are changed.

Preliminary

NL5–0: Specify the number of raster-rows to be driven. The number of raster-row can be adjusted in units of eight. The address mapping of GRAM is independent of this setting. The set value should be higher than the panel size.

Table 23. NL bit and Drive Duty (SCN5-0=00_0000)

NL5	NL4	NL3	NL2	NL1	NL0	Display Size	LCD Raster Rows	Gate- Lines Used
0	0	0	0	0	0	Setting disabled	Setting disabled	Setting disabled
0	0	0	0	0	1	240RGB X 16	16	G1 to G16
0	0	0	0	1	0	240RGB X 24	24	G1 to G24
0	0	0	0	1	1	240RGB X 32	32	G1 to G32
0	0	0	1	0	0	240RGB X 40	40	G1 to G40
0	0	0	1	0	1	240RGB X 48	48	G1 to G48
0	0	0	1	1	0	240RGB X 56	56	G1 to G56
0	0	0	1	1	1	240RGB X 64	64	G1 to G64
0	0	1	0	0	0	240RGB X 72	72	G1 to G72
0	0	1	0	0	1	240RGB X 80	80	G1 to G80
0	0	1	0	1	0	240RGB X 88	88	G1 to G88
0	0	1	0	1	1	240RGB X 96	96	G1 to G96
0	0	1	1	0	0	240RGB X 104	104	G1 to G104
0	0	1	1	0	1	240RGB X 112	112	G1 to G112
0	0	1	1	1	0	240RGB X 120	120	G1 to G120
0	0	1	1	1	1	240RGB X 128	128	G1 to G128
0	1	0	0	0	0	240RGB X 136	136	G1 to G136
0	1	0	0	0	1	240RGB X 144	144	G1 to G144
0	1	0	0	1	0	240RGB X 152	152	G1 to G152
0	1	0	0	1	1	240RGB X 160	160	G1 to G160
0	1	0	1	0	0	240RGB X 168	168	G1 to G168
0	1	0	1	0	1	240RGB X 176	176	G1 to G176
0	1	0	1	1	0	240RGB X 184	184	G1 to G184
0	1	0	1	1	1	240RGB X 192	192	G1 to G192
0	1	1	0	0	0	240RGB X 200	200	G1 to G200
0	1	1	0	0	1	240RGB X 208	208	G1 to G208
0	1	1	0	1	0	240RGB X 216	216	G1 to G216
0	1	1	0	1	1	240RGB X 224	224	G1 to G224
0	1	1	1	0	0	240RGB X 232	232	G1 to G232
0	1	1	1	0	1	240RGB X 240	240	G1 to G240
0	1	1	1	1	0	240RGB X 248	248	G1 to G248
0	1	1	1	1	1	240RGB X 256	256	G1 to G256
1	0	0	0	0	0	240RGB X 264	264	G1 to G264
1	0	0	0	0	1	240RGB X 272	272	G1 to G272
1	0	0	0	1	0	240RGB X 280	280	G1 to G280
1	0	0	0	1	1	240RGB X 288	288	G1 to G288
1	0	0	1	0	0	240RGB X 296	296	G1 to G296
1	0	0	1	0	1	240RGB X 304	304	G1 to G304
1	0	0	1	1	0	240RGB X 312	312	G1 to G312
1	0	0	1	1	1	240RGB X 320	320	G1 to G320

NOTE: A FP (front porch) and BP (back porch) period will be inserted as blanking period (All gates output VGL level) before / after the driver scan through all of the scans.

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LCD-DRIVING-WAVEFORM CONTROL (R02H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FLD1	FLD0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

FLD1-0: These bits are for the set up of the interlaced driver's n raster-row. See the following table and figure for the set up value, field raster-row and scanning method.

Notes : 1. This function is not available when the external display interface(i.e. RGB or VSYNC interface) is in use

2. It is possible that the display is not normal by FLD[1:0]=11

Table 24. Association chart for scanning FLD1-0 and n raster-row

FLD1	FLD0	Scanning method
0	0	Setting disabled
0	1	1 field
1	0	Setting disabled
1	1	3 field (interlaced)

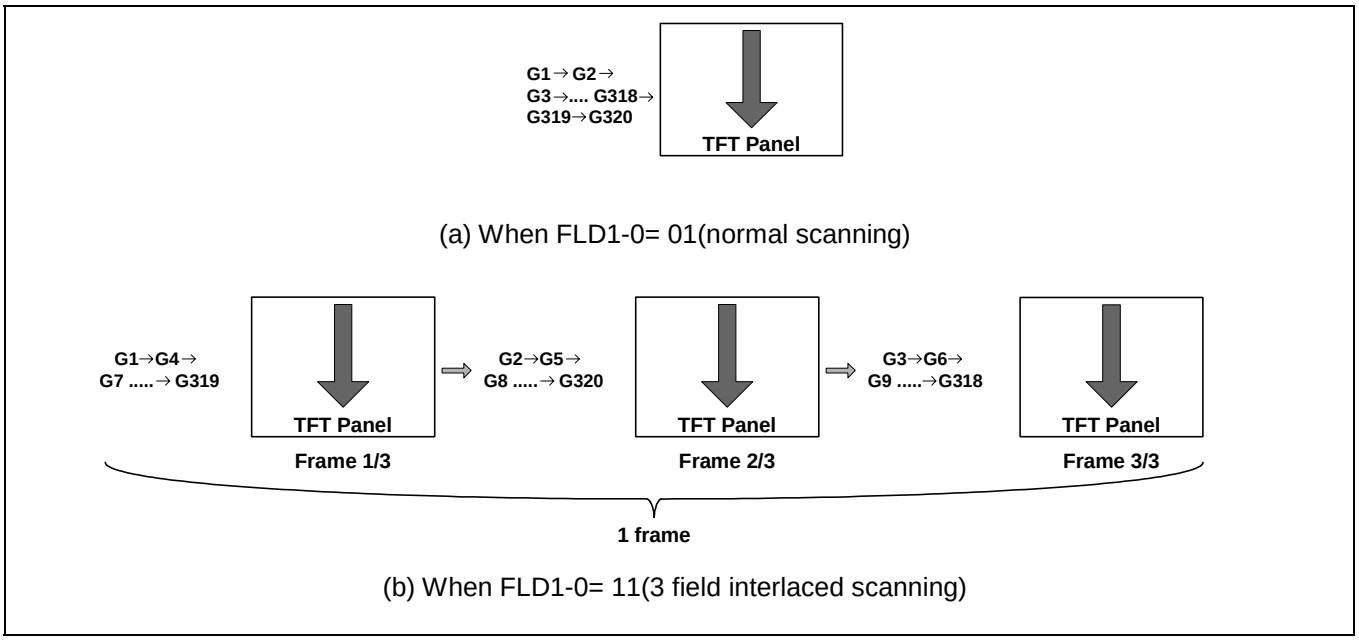


Figure 5. Interlaced scanning method

B/C: When B/C = 0, a frame inversion waveform is generated and it alternates at every frame. When B/C = 1, n raster-row AC waveform is generated and alternates in each raster-row specified by bits EOR in the LCD-driving-waveform control register (R02h). For details, see the N-RASTER-ROW REVERSED AC DRIVE section.

EOR: When the line inversion waveform is set (B/C = 1) and EOR = 1, the odd/even frame-select signals is selected, and the n-raster-row reversed signals are being Exclusive-OR'ed (EOR) for alternating drive. When the EOR is used, the number of the LCD drive raster-row and the n raster-row alternates the LCD. For details, see the ONE-RASTER- ROW REVERSED AC DRIVE section.

NW5–0: Specify the number of raster-rows that will alternate in the line inversion waveform setting (B/C = 1). NW5–NW0 alternates for every set value + 1 raster-row, and the first to the 64th raster-rows can be selected. For details, refer to N-RASTER ROW REVERSED AC DRIVE section

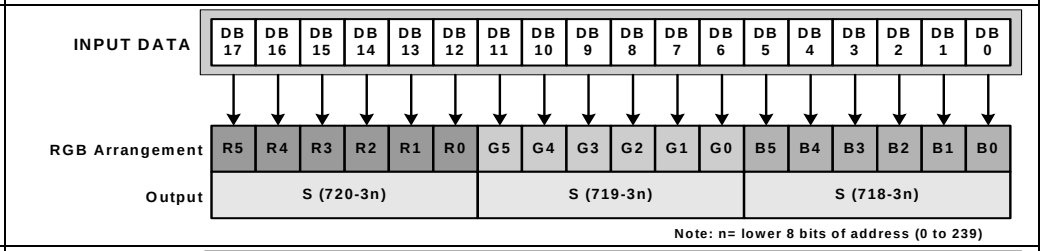
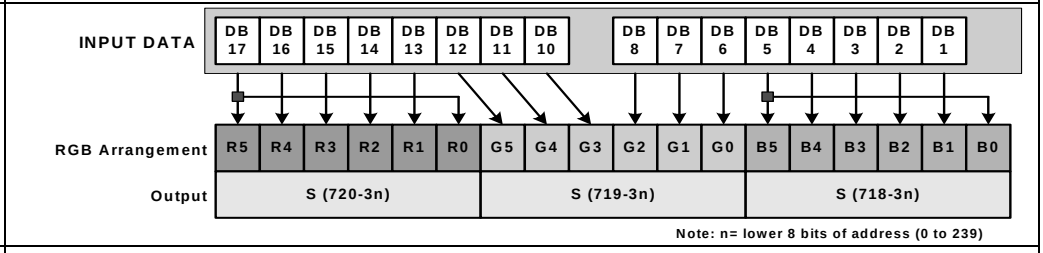
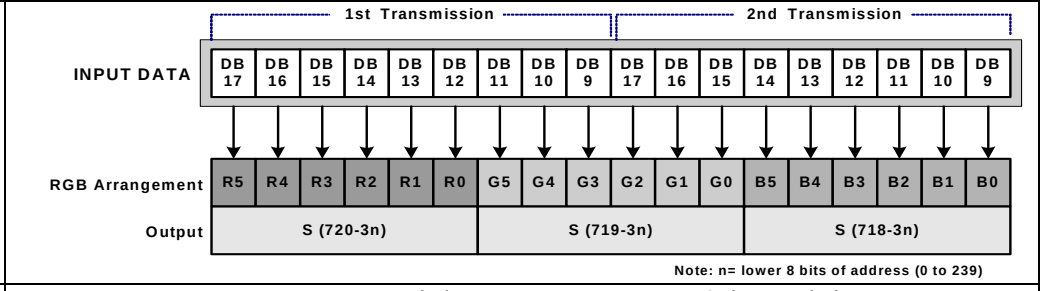
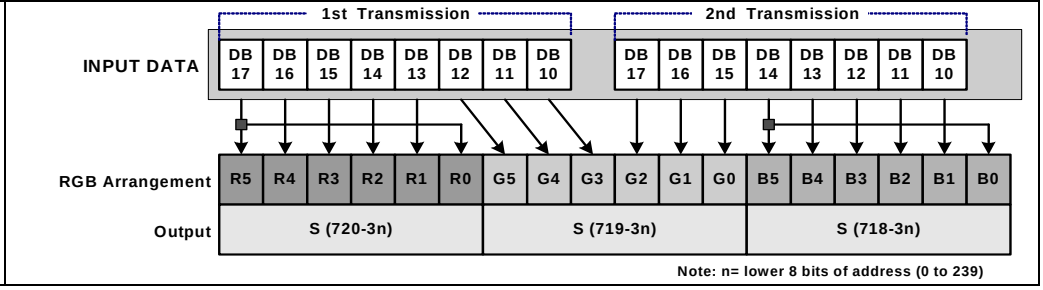
ENTRY MODE (R03H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	TRI	DFM	0	BGR	0	0	0	0	0	0	I/D1	I/D0	0	0	0	0

TRI: This bit is active on the 80-system of 8-bit bus interface and the data for 1-pixel is transported to the memory for 3 write cycles. This bit is on the 80-system of 16-bit interface and the data for 1-pixel is transported to the memory for 2 write cycles. When the 80-system interface mode is not set in the 8-bit or16-bit mode, set TRI bit to be “0”.

DFM: When 8-bit or 16-bit 80 interface mode and TRI bit =1, DFM defines color depth for the IC.
16-bit (80-system), DFM = 0: 262k-color mode (16-bit, 2-bit data transfer to GRAM)
16-bit (80-system), DFM = 1: 262k-color mode (2-bit, 16-bit data transfer to GRAM)

8-bit (80-system), DFM = 0: 262k-color mode (3 times of 6-bit data transfer to GRAM)
8-bit (80-system), DFM = 1: 65k-color mode (5-bit, 6-bit, 5-bit data transfer to GRAM)

TRI	DFM	Interface Mode	Write data to GRAM
0	0	68/80 System 18bit	
		68/80 System 16bit	
		68/80 System 9bit	
		68/80 System 8bit	

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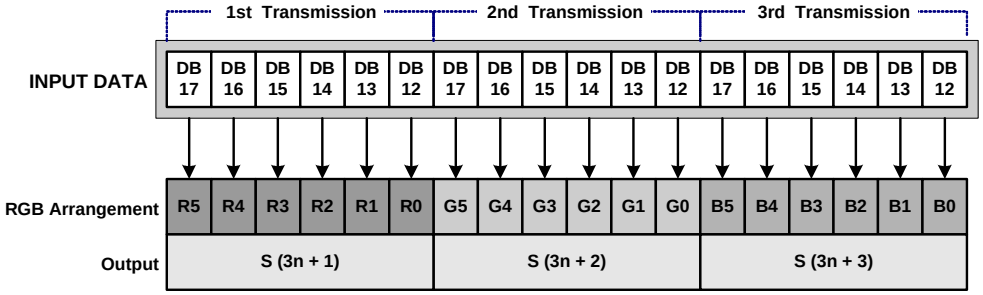
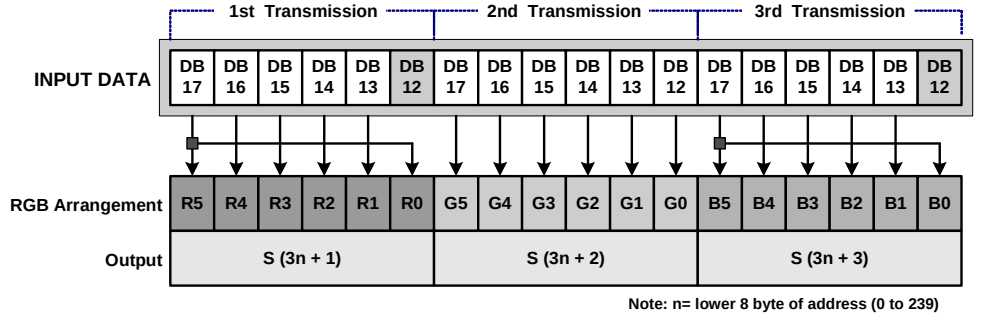
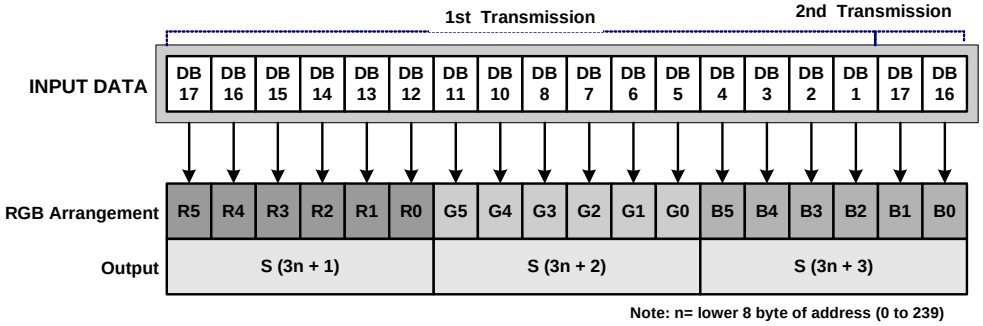
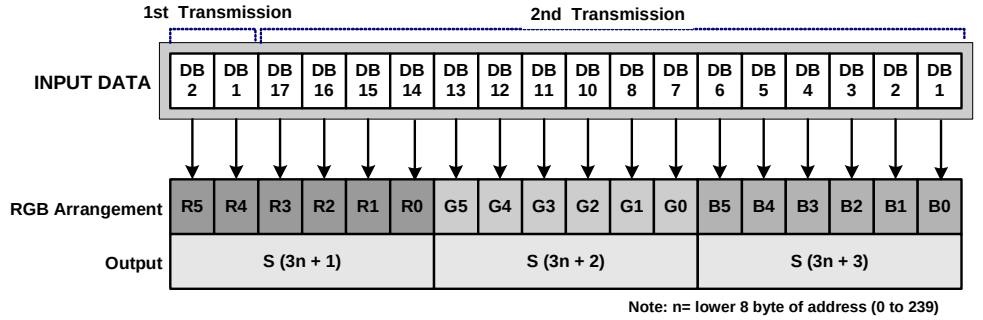
TRI	DFM	Interface Mode	Write data to GRAM
1	0	80-system 8-bit	
	1	80-system 8-bit	
	0	80-system 16-bit	
	1	80-system 16-bit	

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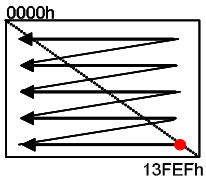
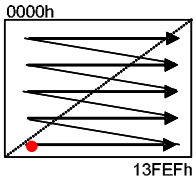
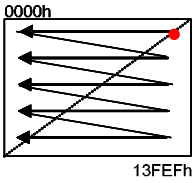
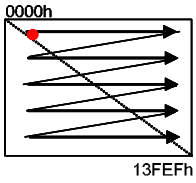
I/D1-0: When I/D1-0 = 1, the address counter (AC) is automatically increased by 1 after the data is written to the GRAM. When I/D1-0 = 0, the AC is automatically decreased by 1 after the data is written to the GRAM. Automatic address counter updating is not performed when reading data from GRAM. The increment/decrement setting of the address counter by I/D1-0 bits is performed independently for the upper (AD15-8) and lower (AD7-0) addresses.

Table 25. Address Direction Setting

	I/D1-0=”00” H: decrement V: decrement	I/D1-0=”01” H: increment V: decrement	I/D1-0=”10” H: decrement V: increment	I/D1-0=”11” H: increment V: increment
Horizontal				

BGR: After writing 18-bit data to GRAM, it is changed from <R><G><B> into <B><G><R>.

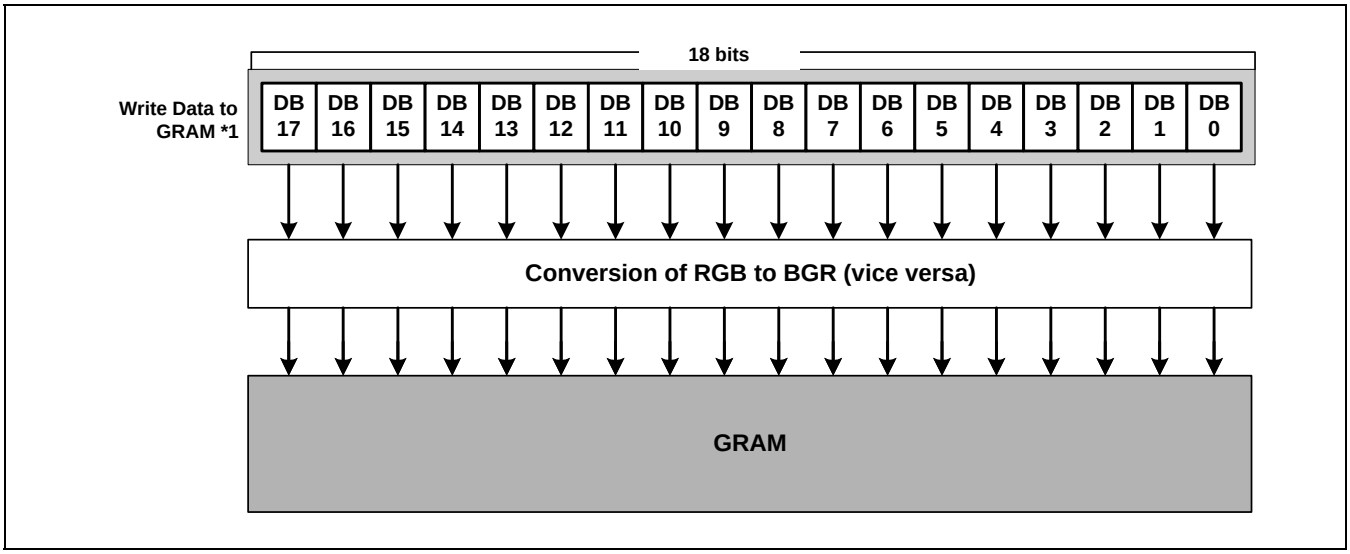


Figure 6. Write data to GRAM via RGB swapping block

Preliminary

DISPLAY CONTROL (R07H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	0	GON	CL	REV	D1	D0

PT1-0: Normalize the source outputs when non-displayed area of the partial display is driven. For details, see the SCREEN-DIVISION DRIVING FUNCTION section.

CL	PT1	PT0	Source Output on Non-display Area		VCOM Output on Non-display Area		Gate Output for Non-display Area
			Positive	Negative	Positive	Negative	
0	0	0	VGS	VGS	VCOML	VCOML	operating
0	0	1	VGS	GVDD	VCOML	VCOMH	
0	1	0	GVDD	VGS	VCOML	VCOMH	
0	1	1	Setting disable				
1	0	0	AVSS	AVSS	VCOML	VCOML	operating
1	0	1	AVSS	GVDD	VCOML	VCOMH	
1	1	0	GVDD	AVSS	VCOML	VCOMH	
1	1	1	Setting disable				

VLE2–1: When VLE1 = 1, a vertical scroll is performed in the 1st screen. When VLE2 = 1, a vertical scroll is performed in the 2nd screen. Vertical scrolling on the two screens cannot be controlled at the same time.

VLE2	VLE1	2nd Screen	1st Screen
0	0	Fixed display	Fixed display
0	1	Fixed display	Scroll
1	0	Scroll	Fixed display
1	1	Setting disabled	Setting disabled

SPT: When SPT = 1, the 2-division LCD drive is performed. For details, see the SCREEN-DIVISION DRIVING FUNCTION section.

Note: this function is not available when the external display interface (i.e. RGB interface or VSYNC interface) is in use.

GON: Gate on/off control signal. All gate outputs are set to be gate off level when GON = 0.
When GON = 1, gate driver is working: G1 to G320 output is either VGH or VGL level. See the Instruction set up flow for further description on the display on/off flow.

GON	Gate Output
0	All gates off (All gates outputs are set to VGL)
1	Gate on(VGH / VGL)

CL: CL = 1 selects 8-color display mode. For details, see the section on 8-COLOR DISPLAY MODE.

CL	Number of display colors
0	262,144 colors
1	8 colors

REV: When the REV = 1, all character and graphics display sections display with reversal. Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels.

REV	GRAM Data	Display Area	
		Positive	**Negative**
0	6'b000000 : 6'b111111	V63 : V0	V0 : V63
1	6'b000000 : 6'b111111	V0 : V63	V63 : V0

D1–0: When D1 is 1, display is on. And, when D1 is 0, display is off. When display is off, the display data remains in the GRAM, and can be re-displayed instantly by setting "D1 = 1". When D1 is 0, the display is off with the entire source outputs set to the VSS level. Because of this, the S6D0139 can control the charging current for the LCD with AC driving. Control the display on/off while control GON. For details, see the Instruction set up flow.

When D1–0 = 01, the internal display of the S6D0139 is performed although the display is off. When D1-0 = 00, the internal display operation halts and the display is off.

D1	D0	GON	Source output	Gate Output	VCOM Output	Internal display operation
0	0	0	AVSS	VGL	AVSS	Halt
0	1	1	AVSS	Operate	AVSS	Operate
1	0	1	Blank Display	Operate	Operate	Operate
1	1	1	Normal Display	Operate	Operate	Operate

Notes:

1. Writing from MCU to GRAM is independent of D1–0.
2. In sleep and stand-by mode, D1–0 = 00. However, the register contents of D1–0 are not modified.
3. When source output is in the same phase with VCOM, white screen is displayed at normally white LCD panel

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DISPLAY CONTROL 2 (R08H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

The blanking period in the start and end of the display area can be defined using this register.
When N-raster-row is driving, a blank period is inserted after all screens are drawn. Front and Back porch can be adjusted using FP3-0 and BP3-0 bits (R08h).

FP3-0/BP3-0: Set the periods of blanking (the front and back porch), which are placed at the beginning and end of the display. FP3-0 is for a front porch and BP3-0 is for a back porch. When front and back porches are set, the settings should meet the following conditions.

$2 \leq BP + FP \leq 16$ raster-rows

$FP \geq 1$ raster-rows
$BP \geq 1$ raster-rows

When the external display interface is in use, the back porch (BP) will start on the falling edge of the VSYNC signal and the display operation will commence at the end of the back-porch period. The front porch (FP) will start when data for the number of raster-rows specified by the NL bits has been displayed. During the period between the completion of the front-porch period and the next VSYNC signal, the display will remain blank.

NOTE: In the interlace drive mode, FP and BP setting is ignored: total sum of blanking period between 3 frames is automatically set to be 16 raster-rows. In the case of internal display mode, FP and BP settings are automatically set to be 8 raster-rows.

Table 26. Front/Back Porch

FP3 BP3	FP2 BP2	FP1 BP1	FP0 BP0	# of Raster Periods In the Front Porch # of Raster Periods In the Back Porch
0	0	0	0	Setting Disabled
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
. . .	. . .	. . .	. . .	. . .
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	Setting Disabled

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FRAME CYCLE CONTROL (R0BH)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO1	NO0	SDT1	SDT0	ECS 2	ECS 1	ECS 0	DI V1	DIV 0	0	DCR _EX	DCR 2	DCR 1	DCR 0	RTN1	RTN0

NO1-0: Set amount of non-overlay for the gate output.

NO1	NO0	Amount of non-overlap	
		Internal Operation (synchronized with internal clock)	RGB I/F Operation (synchronized with DOTCLK)
0	0	2 clock cycle	16 clock cycle
0	1	4 clock cycle	32 clock cycle
1	0	6 clock cycle	48 clock cycle
1	1	8 clock cycle	64 clock cycle

Note: The amount of non-overlap time is defined from the falling edge of the CL1

SDT1-0: Set delay amount from gate edge (end) to source output.

SDT1	SDT0	Delay amount of the source output	
		Internal Operation (synchronized with internal clock)	RGB I/F Operation (synchronized with DOTCLK)
0	0	1 clock cycle	8 clock cycle
0	1	2 clock cycle	16 clock cycle
1	0	3 clock cycle	24 clock cycle
1	1	4 clock cycle	32 clock cycle

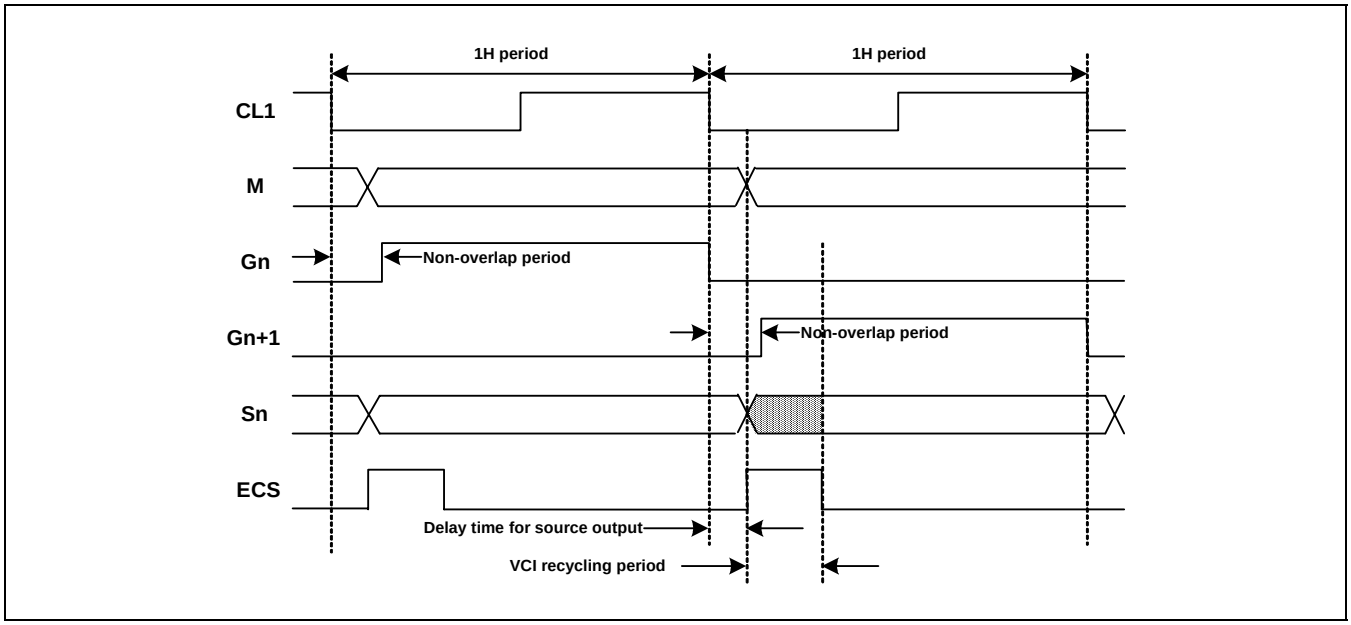

Figure 7. Set Delay from Gate Output to Source Output and ECS signal

Note: The values specified by the bits of ECS, SDT1-0 and NO1-0 vary in a reference clock for each interface mode.

Internal operation mode: Internal R-C oscillation clock
RGB-I/F mode : DOTCLK
VSYNC-I/F : Internal R-C oscillation clock

ECS: ECS period is sustained for the number of clock cycle which is set on ECS 2-0.

ECS2	ECS1	ECS0	ECS period	
			Internal Operation (synchronized with internal clock)	RGB I/F Operation (synchronized with DOTCLK)
0	0	0	0	0
0	0	1	2 clock cycle	8 clock cycle
0	1	0	4 clock cycle	16 clock cycle
0	1	1	6 clock cycle	24 clock cycle
1	0	0	8 clock cycle	32 clock cycle
1	0	1	12 clock cycle	48 clock cycle
1	1	0	14 clock cycle	56 clock cycle
1	1	1	Setting disabled	Setting disabled

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DIV1-0: Set the division ratio of clocks for internal operation (DIV1-0). Internal operations are driven by clocks, which are frequency divided according to the DIV1-0 setting. Frame frequency can be adjusted along with the 1H period (RTN3-0). When changing number of the drive cycle, adjust the frame frequency. For details, see the Frame Frequency Adjustment Function section.

DIV1	DIV0	Division Ratio	Internal operation clock frequency(INCLK)
0	0	1	fosc/1
0	1	2	fosc/2
1	0	4	fosc/4
1	1	8	fosc/8

*fosc = R-C oscillation frequency

$$\text{Frame Frequency} = \frac{f_{osc}}{\text{Clock cycles per raster-row x division ratio x (Line+B)}} \text{ [Hz]}$$

f_{osc}: R-C oscillation frequency
Line: Number of raster-rows (NL bit)
Clock cycles per raster-row: RTN bit
Division ratio: DIV bit
B: Blank period(Back porch + Front Porch)

Figure 8. Formula for the frame frequency

DCR_EX: Input selection signal for external interface mode. (0: internal operation clock, 1: External clock)
Set DCR_EX bit to 1 for external clock. The external clock is the DCCLK (clock cycle for step-up circuit) source, when external interface mode is in use (DM [1:0]="01").

*In RGB mode, DCR_EX should be set before power setting.

DCR 2-0: Set clock cycle for step-up circuit in external interface mode. Please set DCR_EX bit to "1" and DCR1-0 value when external interface is in use. In this case, DOTCLK must be input periodically and continuously.

DCR2	DCR1	DCR0	Clock cycle for step-up circuits (DCCLK) in external interface mode
0	0	0	DOTCLK/32
0	0	1	DOTCLK/64
0	1	0	DOTCLK/128
0	1	1	DOTCLK/256
1	*	*	DOTCLK/512

Note: If external input clock cycle is variable or discontinuous, clock cycle for step-up circuit must be generated internally (DCR_EX=0).

RTN1-0: Set the 1H period (1 raster-row).

RTN1	RTN0	Horizontal clock frequency(CL1)	Clock frequency for step-up circuits(DCCLK)
0	0	INCLK/16	fosc/8
0	1	INCLK/20	fosc/10
1	0	INCLK/24	fosc/12
1	1	INCLK/28	fosc/14

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External Display Interface Control (R0Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0

RM: Specifies the interface for RAM accesses. When the display data is written via the RGB interface, RM bit should be set (RM = 1). This bit and the DM bits can be set independently. The display data can be written via the system interface by clearing this bit while the RGB interface is used.

RM	Interface for RAM Access
0	System interface / VSYNC interface
1	RGB interface

DM1-0: Specify the display operation mode. The interface operation is based on the bits of DM1-0. This setting enables switching interface between internal operation and the external display interface. Switching among two external display interfaces (RGB and VSYNC interface) should not be done.

Note : “RM=0 & DM[1:0]=01” is not supported.

DM1	DM0	Display Operation Mode	Display Operation Mode in MDDI
0	0	Internal clock operation	Internal clock operation
0	1	RGB interface	disable
1	0	VSYNC interface	VSYNC interface
1	1	disable	disable

Note: In case of “RM=0 and DM [1:0] =01”
Must be write 1 frame image data to GRAM in 1 frame before

RIM1-0: Specify the RGB interface mode when the RGB interface is used. Specifically, this setting specifies the mode when the bits of DM and RM are set to RGB interface. These bits should be set before display operation through the RGB interface and should not be set during operation.

RIM1	RIM0	RGB Interface Mode
0	0	18-bit RGB interface (one transfer/pixel)
0	1	16-bit RGB interface (one transfer /pixel)
1	0	6-bit RGB interface (three transfers /pixel)
1	1	Setting disable

Depending on the external display interface setting, various interfaces can be specified to match the display state. While displaying motion pictures (RGB /VSYNC interface), the data for display can be written in high-speed write mode, which achieves both low power consumption and high-speed access.

Table 27. Display State and Interface

Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM1-0)
Still Pictures	Internal Clock	System interface (RM=0)	Internal clock (DM1-0=00)
Motion Pictures	RGB interface	RGB interface (RM=1)	RGB interface (DM1-0=01)
Motion Picture Display	VSYNC interface	System interface (RM=0)	VSYNC interface (DM1-0=10)-

NOTE: 1) The instruction register can only be set through the system interface.
2) Switching among RGB and VSYNC interface cannot be done.
3) RGB interface modes should not be set during operation.
4) For the transition flow for each operation mode, see the External Display Interface section.

Internal Clock Mode

All display operations are controlled by signals that are generated by the internal clock in internal clock mode. All inputs through the external display interface are invalid. The internal RAM can be accessed only via the system interface.

RGB Interface Mode

The display operations are controlled by the frame synchronization clock (VSYNC), raster-row synchronization signal (HSYNC), and dot clock (DOTCLK) in RGB interface mode. These signals should be supplied during display operation in this mode.

The display data is transferred to the internal RAM via PD17-0 for each pixel. Combining the function of the high-speed write mode and the window address enables display of both the motion picture area and the internal RAM area simultaneously. In this method, data is only transferred when the screen is updated, which reduces the amount of data transferred.

The periods of the front (FP), back (BP) porch, and the display are automatically generated in the S6D0139 by counting the raster-row synchronization signal (HSYNC) based on the frame synchronization signal (VSYNC).

VSYNC Interface Mode

The internal display operation is synchronized with the frame synchronization signal (VSYNC) in VSYNC interface mode. When data is written to the internal RAM with the required speed after the falling edge of VSYNC, motion pictures can be displayed via the conventional interface. There are some limitations on the timing and methods of writing to RAM. See the section on the external display interface.

In VSYNC interface mode, the VSYNC input pin is the only valid pin. The other input signals for the external display interface are invalid.

The front and back porch period and the display period is automatically generated by the frame synchronization signal (VSYNC) according to the setting of the S6D0139 registers.
x

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MDDI Interface Mode

The MDDI standard, an optimized high-speed serial interconnection technology developed by Qualcomm, increases reliability and reduces power consumption, which interface for forward and reverse data transmission. Internal bus architecture provides a way to read and write registers via MDDI.

The MDDI has a differential pair to get low EMI, low power and high speed, increasing the speed of forward direction, encodes data to strobe signal in host.

The front and back porch period and the display period is automatically generated by the frame synchronization signal (VSYNC) according to the setting of the S6D0139 registers.

Preliminary

POWER CONTROL 1 (R10H)
POWER CONTROL 2 (R11H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	BT3	0	SAP2	SAP1	SAP0	BT2	BT1	BT0	DC2	DC1	DC0	0	0	0	SLP	STB
W	1	0	0	GVD 5	GVD 4	GVD 3	GVD 2	GVD 1	GVD 0	0	0	0	0	0	VC2	VC1	VC0

SAP2-0: Adjust the amount of fixed current from the fixed current source in the operational amplifier for the source driver. When the amount of fixed current is large, LCD driving ability and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption. During non-display, when SAP2-0 = “000”, the current consumption can be reduced by ending the operational amplifier and step-up circuit operation.

SAP2	SAP1	SAP0	Amount of Current in Operational Amplifier
0	0	0	Source amp halt
0	0	1	Low
0	1	0	Medium Low
0	1	1	Medium
1	0	0	Medium High
1	0	1	Large
1	1	0	Medium Large
1	1	1	Largest

BT3–0: The factor of output is switched. You can adjust scale factor of the step-up circuit according to the used voltage value. When the step-up operating frequency is high, the driving ability of the step-up circuit and the display quality become high, but the current consumption is increased. You should adjust the frequency considering the display quality and the current consumption.

BT3	BT2	BT1	BT0	VGH	VGL
0	0	0	0	4 X Vci1	-3X Vci1
0	0	0	1	4 X Vci1	-4X Vci1
0	0	1	0	5 X Vci1	-3X Vci1
0	0	1	1	5 X Vci1	-4X Vci1
0	1	0	0	5 X Vci1	-5X Vci1
0	1	0	1	6 X Vci1	-3X Vci1
0	1	1	0	6 X Vci1	-4X Vci1
0	1	1	1	6 X Vci1	-5X Vci1
1	0	0	0	6 X Vci1	-6X Vci1
1	0	1	1	5 X Vci1	-2X Vci1
1	1	0	1	4 X Vci1	-2X Vci1

Note : The value is maximum by register setting

DC2-0: The operating frequency in the step-up circuit is selected. When the step-up operating frequency is high, the driving ability of the step-up circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

DC2	DC1	DC0	Step-up Cycle in Step-up Circuit 1,3	Step-up Cycle in Step-up Circuit 2
0	0	0	DCCLK / 1	DCCLK / 1
0	0	1	DCCLK / 1	DCCLK / 2
0	1	0	DCCLK / 1	DCCLK / 4
0	1	1	DCCLK / 2	DCCLK / 2
1	0	0	DCCLK / 2	DCCLK / 4
1	0	1	DCCLK / 4	DCCLK / 4
1	1	0	DCCLK / 4	DCCLK / 8
1	1	1	DCCLK / 4	DCCLK / 16

Note: DCCLK is Clock frequency for step-up circuits

SLP: When SLP is high, the S6D0139 enters the sleep mode. The internal display operations are halted except for the R-C oscillator for reducing current consumption. Only the following instructions can be executed during the sleep mode. During the sleep mode, the other GRAM data cannot be updated. Register set-up is maintained.

STB: When STB is high, the S6D0139 enters the standby mode, where display operation completely stops. This mode can halt all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, see the Standby Mode section.

Level	Condition
VCOM	AVSS
Gate	AVSS
Source	AVSS

GVD5-0: Set the amplified factor of the GVDD voltage (the voltage for the Gamma voltage). It allows to amplify from 3.0v to 5.0v

GVD 5	GVD 4	GVD 3	GVD 2	GVD 1	GV D 0	GVDD Voltage	GVD 5	GVD 4	GVD 3	GVD 2	GVD 1	GVD 0	GVDD Voltage
0	0	0	0	0	0	3.00V	1	0	0	0	0	0	4.01V
0	0	0	0	0	1	3.03V	1	0	0	0	0	1	4.05V
0	0	0	0	1	0	3.06V	1	0	0	0	1	0	4.08V
0	0	0	0	1	1	3.09V	1	0	0	0	1	1	4.11V
0	0	0	1	0	0	3.12V	1	0	0	1	0	0	4.14V
0	0	0	1	0	1	3.16V	1	0	0	1	0	1	4.17V
0	0	0	1	1	0	3.19V	1	0	0	1	1	0	4.21V
0	0	0	1	1	1	3.22V	1	0	0	1	1	1	4.24V
0	0	1	0	0	0	3.25V	1	0	1	0	0	0	4.27V
0	0	1	0	0	1	3.28V	1	0	1	0	0	1	4.30V

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GVD 5	GVD 4	GVD 3	GVD 2	GVD 1	GV D 0	GVDD Voltage	GVD 5	GVD 4	GVD 3	GVD 2	GVD 1	GVD 0	GVDD Voltage
0	0	1	0	1	0	3.31V	1	0	1	0	1	0	4.33V
0	0	1	0	1	1	3.35V	1	0	1	0	1	1	4.36V
0	0	1	1	0	0	3.38V	1	0	1	1	0	0	4.40V
0	0	1	1	0	1	3.41V	1	0	1	1	0	1	4.43V
0	0	1	1	1	0	3.44V	1	0	1	1	1	0	4.46V
0	0	1	1	1	1	3.47V	1	0	1	1	1	1	4.49V
0	1	0	0	0	0	3.51V	1	1	0	0	0	0	4.52V
0	1	0	0	0	1	3.54V	1	1	0	0	0	1	4.56V
0	1	0	0	1	0	3.57V	1	1	0	0	1	0	4.59V
0	1	0	0	1	1	3.60V	1	1	0	0	1	1	4.62V
0	1	0	1	0	0	3.63V	1	1	0	1	0	0	4.65V
0	1	0	1	0	1	3.66V	1	1	0	1	0	1	4.68V
0	1	0	1	1	0	3.70V	1	1	0	1	1	0	4.71V
0	1	0	1	1	1	3.73V	1	1	0	1	1	1	4.75V
0	1	1	0	0	0	3.76V	1	1	1	0	0	0	4.78V
0	1	1	0	0	1	3.79V	1	1	1	0	0	1	4.81V
0	1	1	0	1	0	3.82V	1	1	1	0	1	0	4.84V
0	1	1	0	1	1	3.86V	1	1	1	0	1	1	4.87V
0	1	1	1	0	0	3.89V	1	1	1	1	0	0	4.91V
0	1	1	1	0	1	3.92V	1	1	1	1	0	1	4.94V
0	1	1	1	1	0	3.95V	1	1	1	1	1	0	4.97V
0	1	1	1	1	1	3.98V	1	1	1	1	1	1	5.00V

VC2-0: Set the VCI1 voltage. These bits set the VCI1 voltage from 0.68 to 1 times of the VCI_REF voltage

VC2	VC1	VC0	VCI1
0	0	0	0.68 X VCI_REF
0	0	1	0.73 X VCI_REF
0	1	0	0.83 X VCI_REF
0	1	1	0.92 X VCI_REF
1	0	0	1.00 X VCI_REF

Note: Don't set any higher VCI1 level than 3.0V

Preliminary

POWER CONTROL 4 (R13H)
POWER CONTROL 5 (R14H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	PON	PON1	AON	0	0	0	0
W	1	0	VCMR	VCM5	VCM4	VCM3	VCM2	VCM1	VCM0	0	0	VML5	VML4	VML3	VML2	VML1	VML0

PON: This is an operation-starting bit for the booster circuit1. In case of PON = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the PON = 1, please refer to the SET UP FLOW OF POWER SUPPLY.

PON1: This is an operation-starting bit for the booster circuit 2, 3. In case of PON1 = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the PON1= 1, please refer to the SET UP FLOW OF POWER SUPPLY.

AON: This is an operation-starting bit for the Amplifier. In case of AON = 0, the circuit is stopped and vice versa. For further information about timing for adjusting to the AON= 1, please refer to the SET UP FLOW OF POWER SUPPLY.

VCMR: If VCMR is LOW, VCOMH is adjusted by VCM5-0 Register and VCOMR pin is used to monitor the input voltage of the AMP which outputs the VCOMH voltage.
If VCMR is HIGH, VCM5-0 register is ignored and VCOMH voltage is adjusted by VCOMR voltage. V COMR voltage is externally supplied. The relationship between VCOMH and VCOMR is given as VCOMH=2.5xVCOMR.

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SUB_PANEL CONTROL(R15H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	FCV_EN				MPU_MODE	STN_EN	SUB_IM1	SUB_IM0

SUB_IM1-0: set the sub-panel interface

SUB_IM1	SUB_IM0	Interface
0	0	18bit
0	1	9bit
1	0	16bit
1	1	8bit

STN_EN: set the panel property.
STN_EN = “1”: STN panel.
STN_EN = “0”: TFT panel**.**

MPU_MODE: set the MPU interfaces
MPU_MODE = “1”: 68 mode
MPU_MODE = “0”: 80 mode

FCV_EN : data format conversion enable signal
FCV_EN = “1”: 16 bit data format conversion (not used)
FCV_EN = “0”: current 16bit data format

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VCM5-0: Set the VCOMH voltage. (Vref = 2.0V)

VCM 5	VCM 4	VCM 3	VCM 2	VCM 1	VCM 0	VCOMH Voltage	VCM 5	VCM 4	VCM 3	VCM 2	VCM 1	VCM 0	VCOMH Voltage
0	0	0	0	0	0	3.00V	1	0	0	0	0	0	4.01V
0	0	0	0	0	1	3.03V	1	0	0	0	0	1	4.05V
0	0	0	0	1	0	3.06V	1	0	0	0	1	0	4.08V
0	0	0	0	1	1	3.09V	1	0	0	0	1	1	4.11V
0	0	0	1	0	0	3.12V	1	0	0	1	0	0	4.14V
0	0	0	1	0	1	3.16V	1	0	0	1	0	1	4.17V
0	0	0	1	1	0	3.19V	1	0	0	1	1	0	4.21V
0	0	0	1	1	1	3.22V	1	0	0	1	1	1	4.24V
0	0	1	0	0	0	3.25V	1	0	1	0	0	0	4.27V
0	0	1	0	0	1	3.28V	1	0	1	0	0	1	4.30V
0	0	1	0	1	0	3.31V	1	0	1	0	1	0	4.33V
0	0	1	0	1	1	3.35V	1	0	1	0	1	1	4.36V
0	0	1	1	0	0	3.38V	1	0	1	1	0	0	4.40V
0	0	1	1	0	1	3.41V	1	0	1	1	0	1	4.43V
0	0	1	1	1	0	3.44V	1	0	1	1	1	0	4.46V
0	0	1	1	1	1	3.47V	1	0	1	1	1	1	4.49V
0	1	0	0	0	0	3.51V	1	1	0	0	0	0	4.52V
0	1	0	0	0	1	3.54V	1	1	0	0	0	1	4.56V
0	1	0	0	1	0	3.57V	1	1	0	0	1	0	4.59V
0	1	0	0	1	1	3.60V	1	1	0	0	1	1	4.62V
0	1	0	1	0	0	3.63V	1	1	0	1	0	0	4.65V
0	1	0	1	0	1	3.66V	1	1	0	1	0	1	4.68V
0	1	0	1	1	0	3.70V	1	1	0	1	1	0	4.71V
0	1	0	1	1	1	3.73V	1	1	0	1	1	1	4.75V
0	1	1	0	0	0	3.76V	1	1	1	0	0	0	4.78V
0	1	1	0	0	1	3.79V	1	1	1	0	0	1	4.81V
0	1	1	0	1	0	3.82V	1	1	1	0	1	0	4.84V
0	1	1	0	1	1	3.86V	1	1	1	0	1	1	4.87V
0	1	1	1	0	0	3.89V	1	1	1	1	0	0	4.91V
0	1	1	1	0	1	3.92V	1	1	1	1	0	1	4.94V
0	1	1	1	1	0	3.95V	1	1	1	1	1	0	4.97V
0	1	1	1	1	1	3.98V	1	1	1	1	1	1	5.00V

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VML5-0: Set the Amplitude of the VCOM voltage.
VCOML is automatically adjusted by setting the Amplitude of VCOM voltage.

(Vref = 2.0V)

VML 5	VML 4	VML 3	VML 2	VML 1	VML 0	Amplitude of VCOM	VML 5	VML 4	VML 3	VML 2	VML 1	VML 0	Amplitude of VCOM
0	0	0	0	0	0	3.592	1	0	0	0	0	0	4.815
0	0	0	0	0	1	3.631	1	0	0	0	0	1	4.854
0	0	0	0	1	0	3.669	1	0	0	0	1	0	4.892
0	0	0	0	1	1	3.707	1	0	0	0	1	1	4.930
0	0	0	1	0	0	3.745	1	0	0	1	0	0	4.968
0	0	0	1	0	1	3.783	1	0	0	1	0	1	5.006
0	0	0	1	1	0	3.822	1	0	0	1	1	0	5.045
0	0	0	1	1	1	3.860	1	0	0	1	1	1	5.083
0	0	1	0	0	0	3.898	1	0	1	0	0	0	5.121
0	0	1	0	0	1	3.936	1	0	1	0	0	1	5.159
0	0	1	0	1	0	3.975	1	0	1	0	1	0	5.197
0	0	1	0	1	1	4.013	1	0	1	0	1	1	5.236
0	0	1	1	0	0	4.051	1	0	1	1	0	0	5.274
0	0	1	1	0	1	4.089	1	0	1	1	0	1	5.312
0	0	1	1	1	0	4.127	1	0	1	1	1	0	5.350
0	0	1	1	1	1	4.166	1	0	1	1	1	1	5.389
0	1	0	0	0	0	4.204	1	1	0	0	0	0	5.427
0	1	0	0	0	1	4.242	1	1	0	0	0	1	5.465
0	1	0	0	1	0	4.280	1	1	0	0	1	0	5.503
0	1	0	0	1	1	4.318	1	1	0	0	1	1	5.541
0	1	0	1	0	0	4.357	1	1	0	1	0	0	5.580
0	1	0	1	0	1	4.395	1	1	0	1	0	1	5.618
0	1	0	1	1	0	4.433	1	1	0	1	1	0	5.656
0	1	0	1	1	1	4.471	1	1	0	1	1	1	5.694
0	1	1	0	0	0	4.510	1	1	1	0	0	0	5.732
0	1	1	0	0	1	4.548	1	1	1	0	0	1	5.771
0	1	1	0	1	0	4.586	1	1	1	0	1	0	5.809
0	1	1	0	1	1	4.624	1	1	1	0	1	1	5.847
0	1	1	1	0	0	4.662	1	1	1	1	0	0	5.885
0	1	1	1	0	1	4.701	1	1	1	1	0	1	5.924
0	1	1	1	1	0	4.739	1	1	1	1	1	0	5.962
0	1	1	1	1	1	4.777	1	1	1	1	1	1	6.000

NOTES: Set VCOML range from -2V to 0V (In the case of Vref=2.0V)

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RAM ADDRESS SET (R20H/R21H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

AD16–0: Initially set GRAM addresses to the address counter (AC). Once the GRAM data is written, the AC is automatically updated according to the I/D bit settings. This allows consecutive accesses without resetting address. Once the GRAM data is read, the AC is not automatically updated. GRAM address setting is not allowed in the standby mode. Ensure that the address is set within the specified window address
When RGB interface is in use (RM1-0=10), AD16-0 will be set at the falling edge of the VSYNC signal.
When the internal clock operation and VSYNC interface (RM=0X) are in use, AD16-0 will be set upon execution of an instruction.

AD16 to AD0	GRAM setting
“00000”H to “000EF”H	Bitmap data for G1
“00100”H to “001EF”H	Bitmap data for G2
“00200”H to “002EF”H	Bitmap data for G3
“00300”H to “003EF”H	Bitmap data for G4
: : :	: : :
“13C00”H to “13CEF”H	Bitmap data for G317
“13D00”H to “13DEF”H	Bitmap data for G318
“13E00”H to “13EEF”H	Bitmap data for G319
“13F00”H to “13FEF”H	Bitmap data for G320

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WRITE DATA TO GRAM (R22H)

R/W	RS	IB17	IB16	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	RAM write data (WD17-0): Pin assignment varies according to the interface method. (see the following figure for more information)																	
W	1	IB17	IB16	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
		When RGB-interface , WD : the latch of write gram port																	

WD17-0: Input data for GRAM can be expanded to 18 bits. The expansion format varies according to the interface method. The input data selects the grayscale level. After a write, the address is automatically updated according to I/D bit settings. The GRAM cannot be accessed in standby mode. When 16- or 8-bit interface is in use, the write data is expanded to 18 bits by writing the MSB of the <R><B> data to its LSB.

When written data to GRAM is used by RGB interface via the system interface, please make sure that writing data do not cause conflicts.

When the 18-bit RGB interface is in use, 18-bit data is written to RAM via PD17-0. This interface is available on the 262,144-colors. When the 16-bit RGB interface is in use, the MSB is written to its LSB. This interface is available on the 65,536-colors.

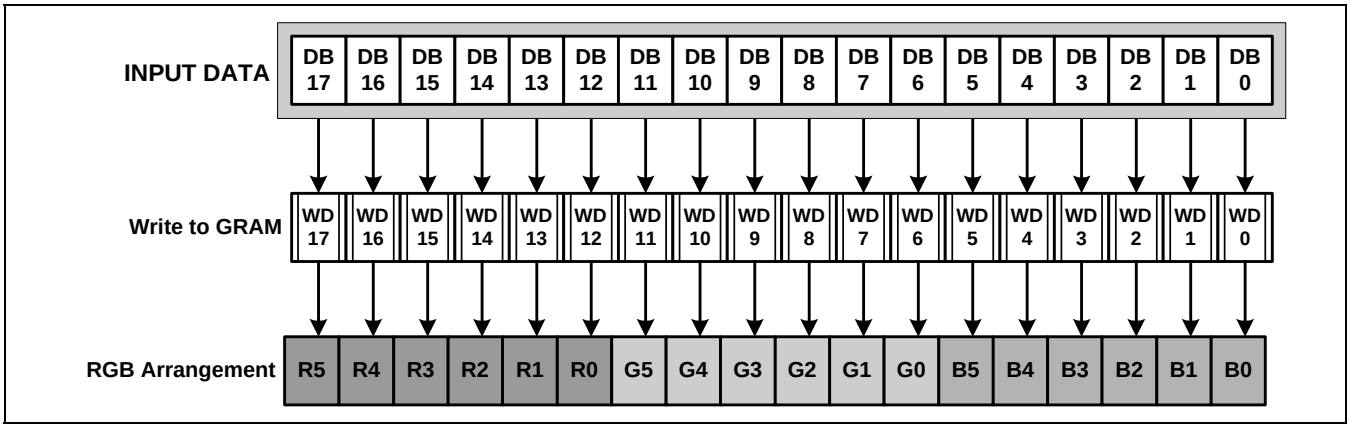

Figure 9. 18-bit System interface (260K-color)

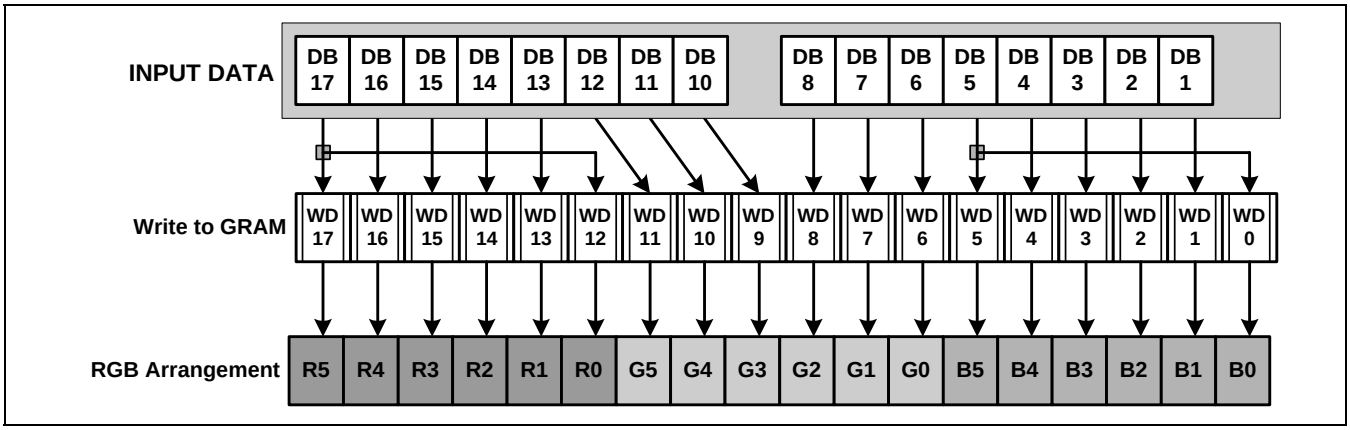

Figure 10. 16-bit System interface (65K-color)

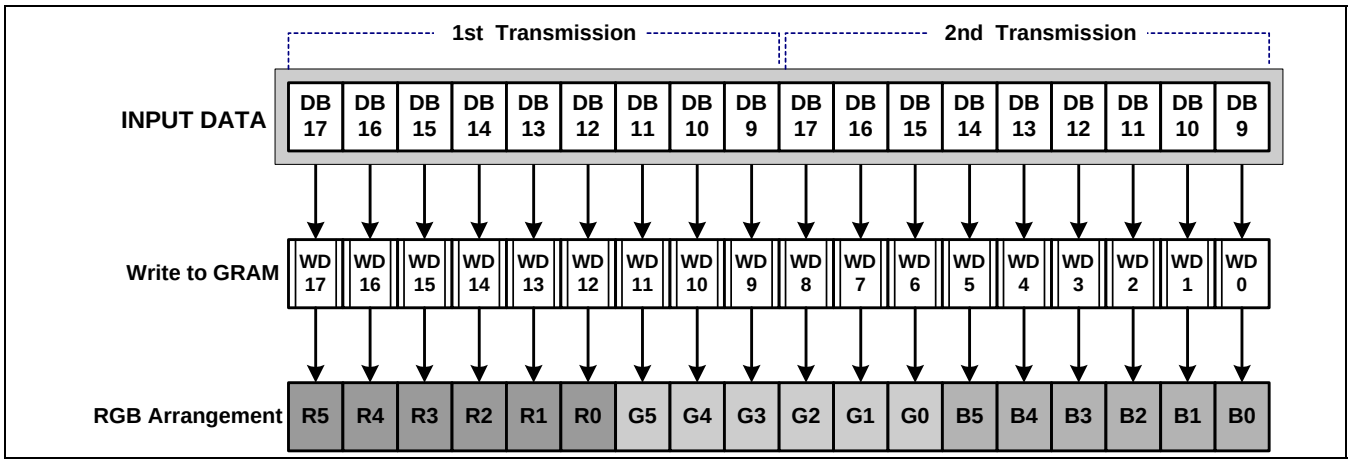

Figure 11. 9-bit System interface (260K-color)

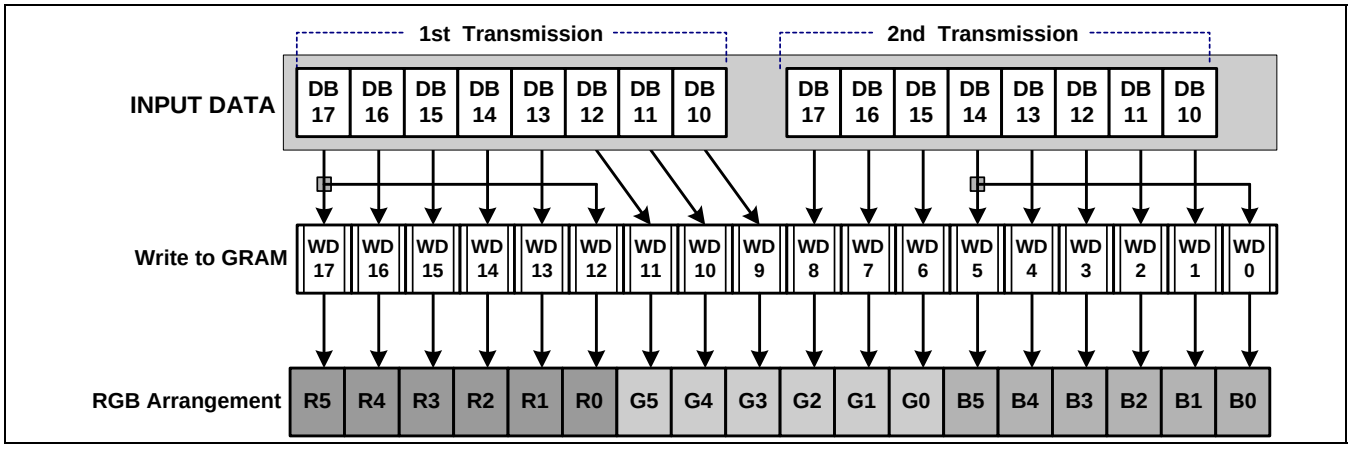

Figure 12. 8-bit System interface (65K-color) TRI=0, DFM=0

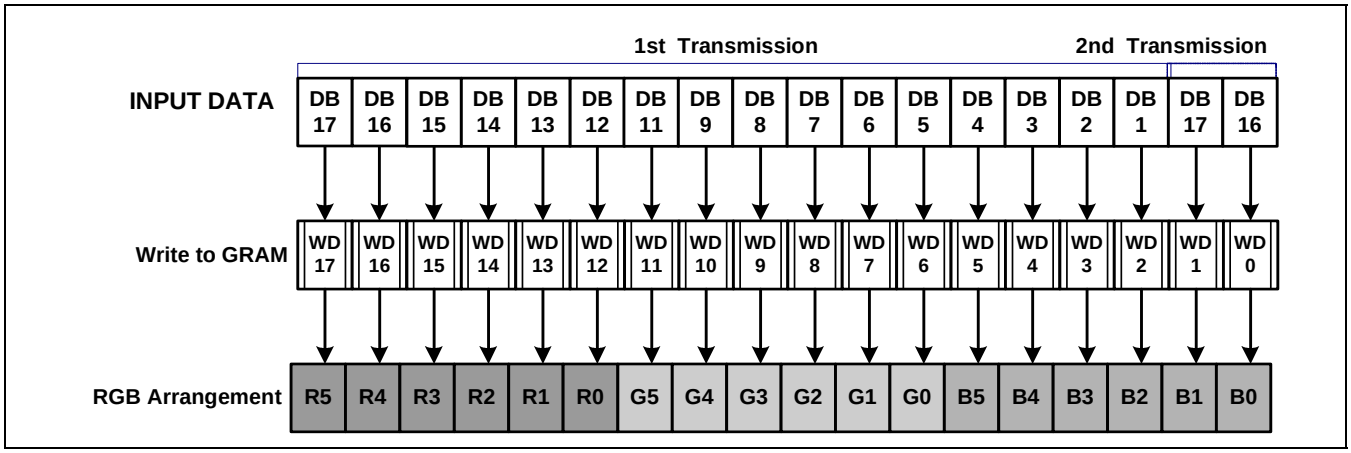

Figure 13. 16-bit System interface (260K-color) TRI=1, DFM=0

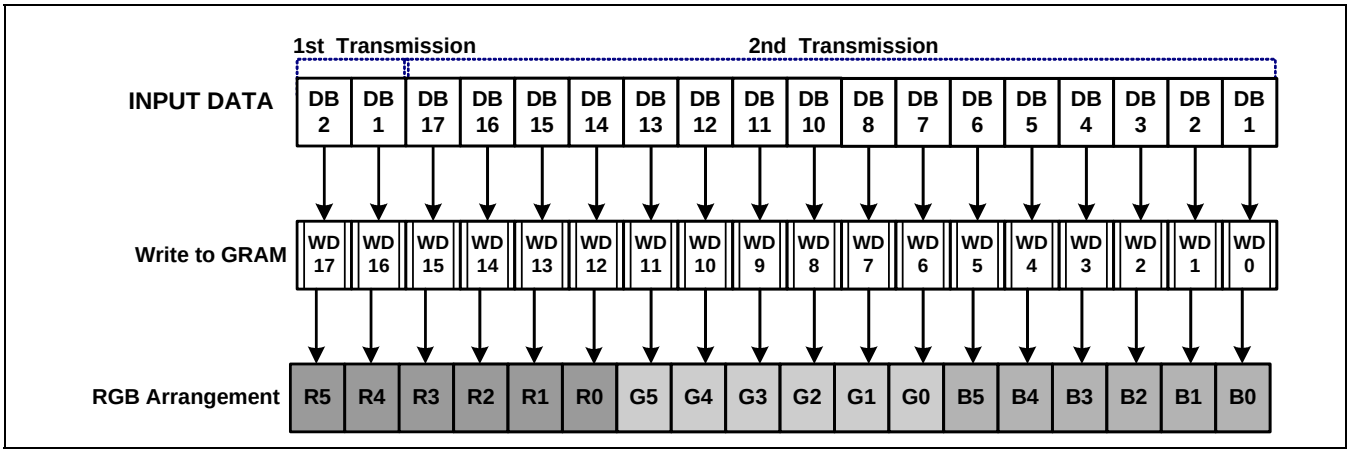

Figure 14. 16-bit System interface (65K-color) TRI=1, DFM=1

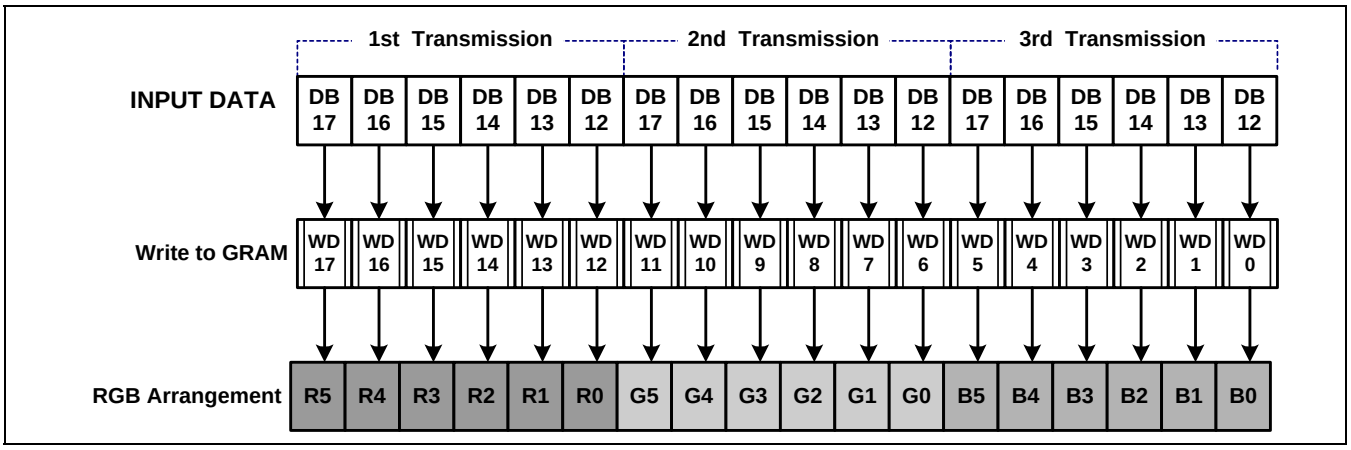

Figure 15. 8-bit System interface (260K-color) TRI=1, DFM=0

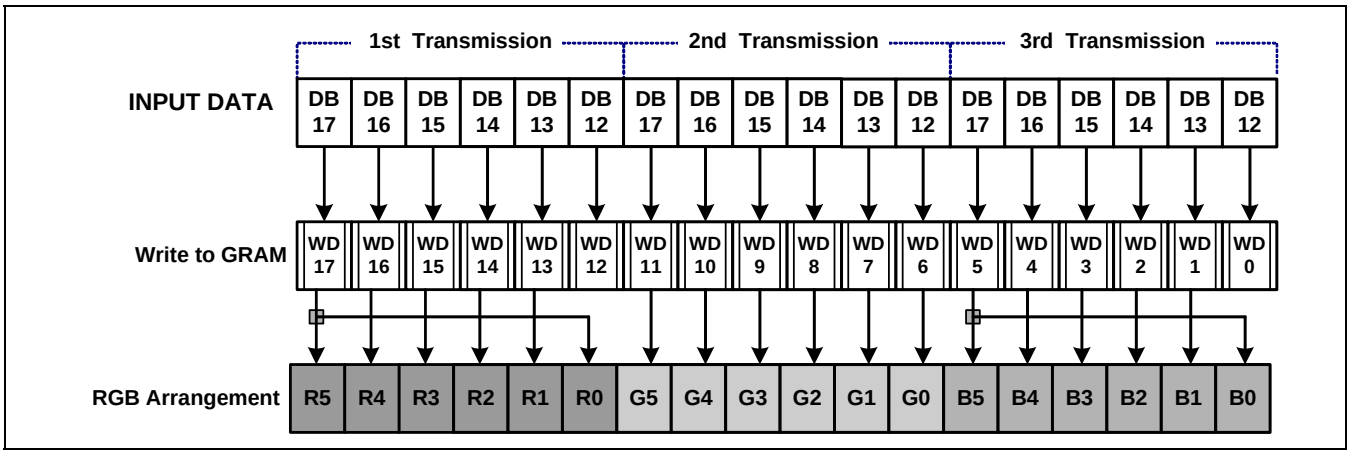

Figure 16. 8-bit System interface (65K-color) TRI=1, DFM=1

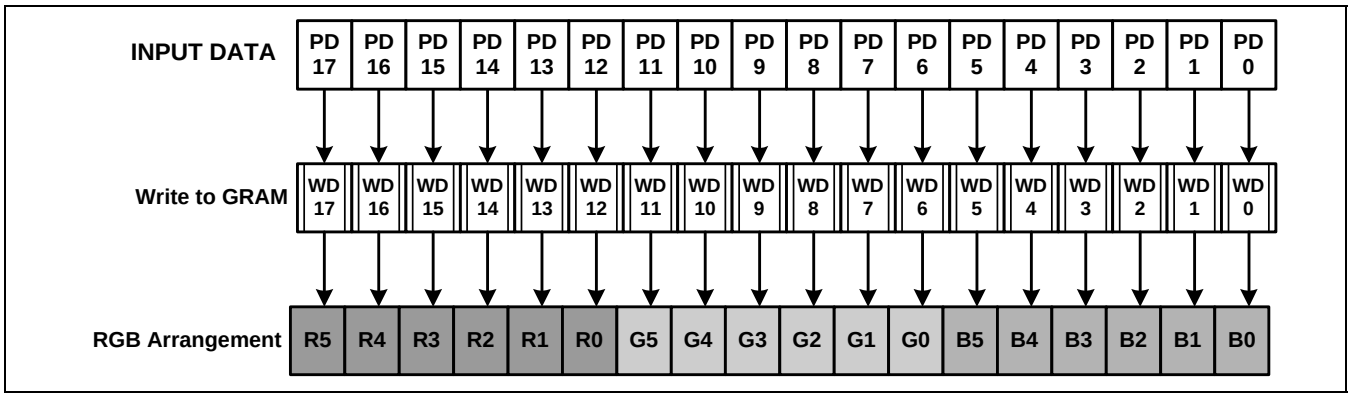

Figure 17. 18-bit RGB interface (260K-color)

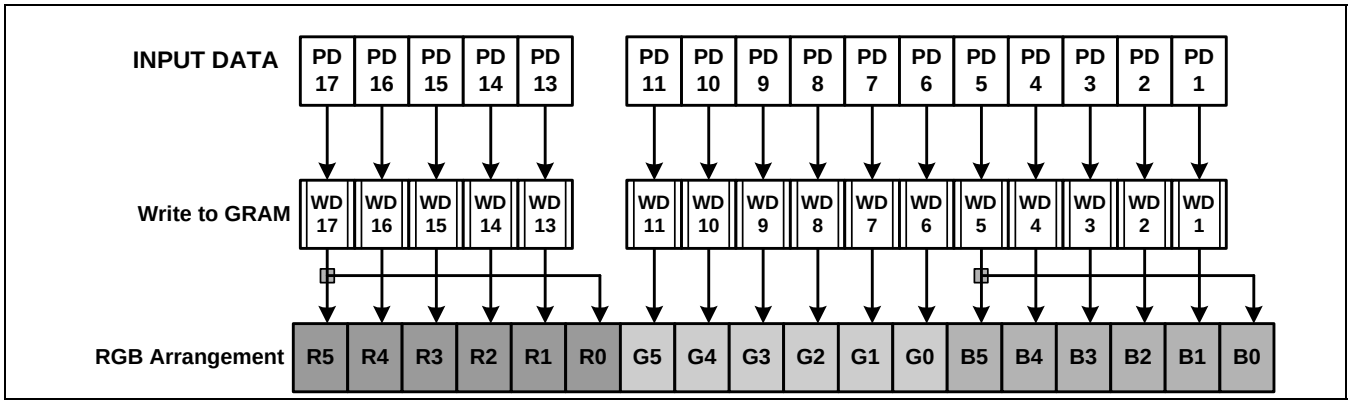

Figure 18. 16-bit RGB interface (65K-color)

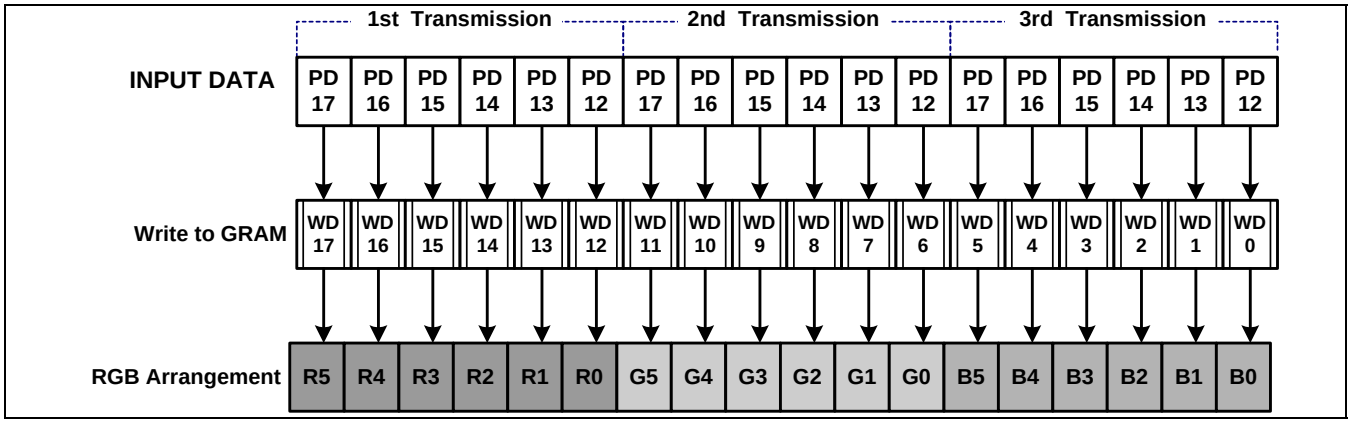

Figure 19. 6-bit RGB interface (260K-color)

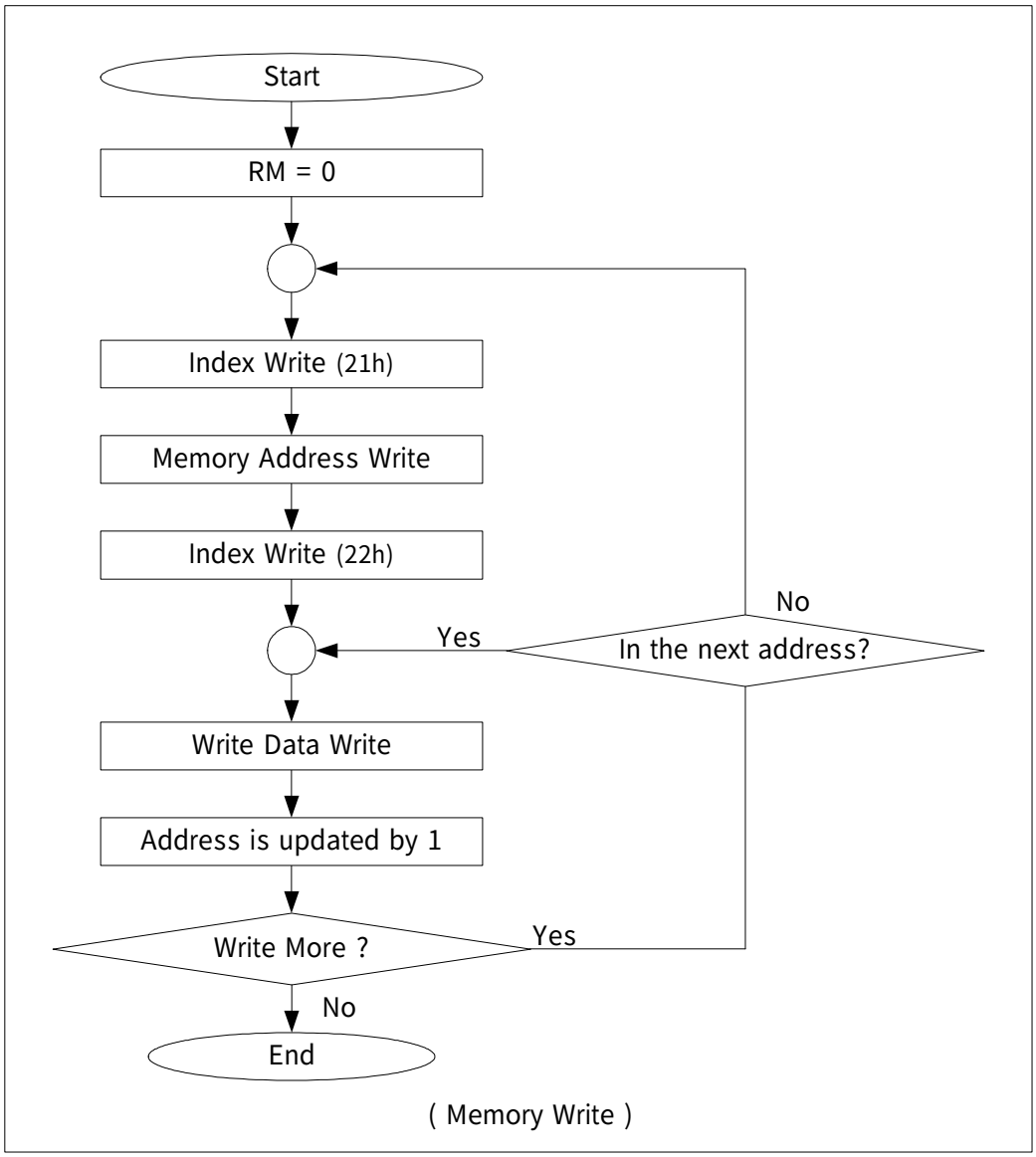

Figure 20. Memory write sequnce

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Table 28. GRAM Data and Grayscale Level

GRAM data	Grayscale Polarity		GRAM Data	Grayscale Polarity		GRAM Data	Grayscale Polarity		GRAM Data	Grayscale Polarity	
RGB	N	P	RGB	N	P	RGB	N	P	RGB	N	P
000000	V0	V63	010000	V16	V47	100000	V32	V31	110000	V48	V15
000001	V1	V62	010001	V17	V46	100001	V33	V30	110001	V49	V14
000010	V2	V61	010010	V18	V45	100010	V34	V29	110010	V50	V13
000011	V3	V60	010011	V19	V44	100011	V35	V28	110011	V51	V12
000100	V4	V59	010100	V20	V43	100100	V36	V27	110100	V52	V11
000101	V5	V58	010101	V21	V42	100101	V37	V26	110101	V53	V10
000110	V6	V57	010110	V22	V41	100110	V38	V25	110110	V54	V9
000111	V7	V56	010111	V23	V40	100111	V39	V24	110111	V55	V8
001000	V8	V55	011000	V24	V39	101000	V40	V23	111000	V56	V7
001001	V9	V54	011001	V25	V38	101001	V41	V22	111001	V57	V6
001010	V10	V53	011010	V26	V37	101010	V42	V21	111010	V58	V5
001011	V11	V52	011011	V27	V36	101011	V43	V20	111011	V59	V4
001100	V12	V51	011100	V28	V35	101100	V44	V19	111100	V60	V3
001101	V13	V50	011101	V29	V34	101101	V45	V18	111101	V61	V2
001100	V14	V49	011110	V30	V33	101100	V46	V17	111110	V62	V1
001101	V15	V48	011111	V31	V32	101101	V47	V16	111111	V63	V0

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RAM ACCESS via RGB INTERFACE & SYSTEM INTERFACE

All the data for display is written to the internal RAM in the S6D0139 when RGB interface is in use. In this method, data, including that in both the motion picture area and the screen update frame, can only be transferred via RGB interface. Data for display which is not in the motion picture area or the screen update frame can be written via the system interface.

RAM can be accessed via the system interface when RGB interface is in use. When data is written to RAM during RGB interface mode, the ENABLE bit should be low to stop data writing via RGB interface, because RAM writing is always performed in synchronization with the DOTCLK input when ENABLE is high. After this RAM access via the system interface, a waiting time is needed for a write/read bus cycle before the next RAM access starts via RGB interface. When a RAM write conflict occurs, data writing is not guaranteed.

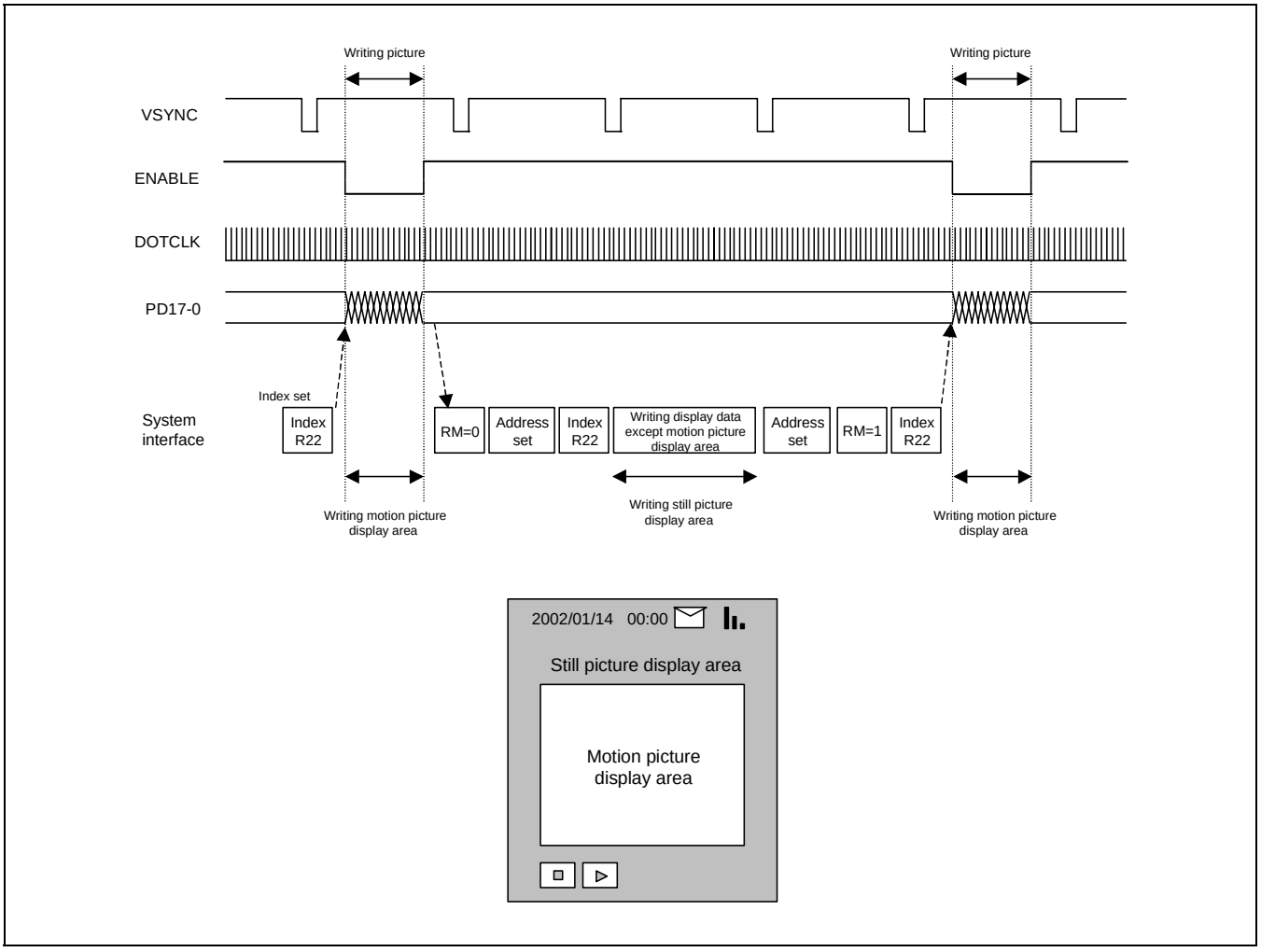

Figure 21. RAM access via RGB Interface & System Interface

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READ DATA FROM GRAM (R22H)

R/W	RS	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	1	RAM Read data (RD17-0): Pin assignment varies according to the interface method. (see the following figure for more information)																	

RD17–0: Read 18-bit data from the GRAM. When the data is read to the MCU, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (DB15–0) becomes invalid and the second-word read is normal.

In case of 16-/8-bit interface, the LSB of <R><B> color data will not be read.

This function is not available in RGB interface mode.

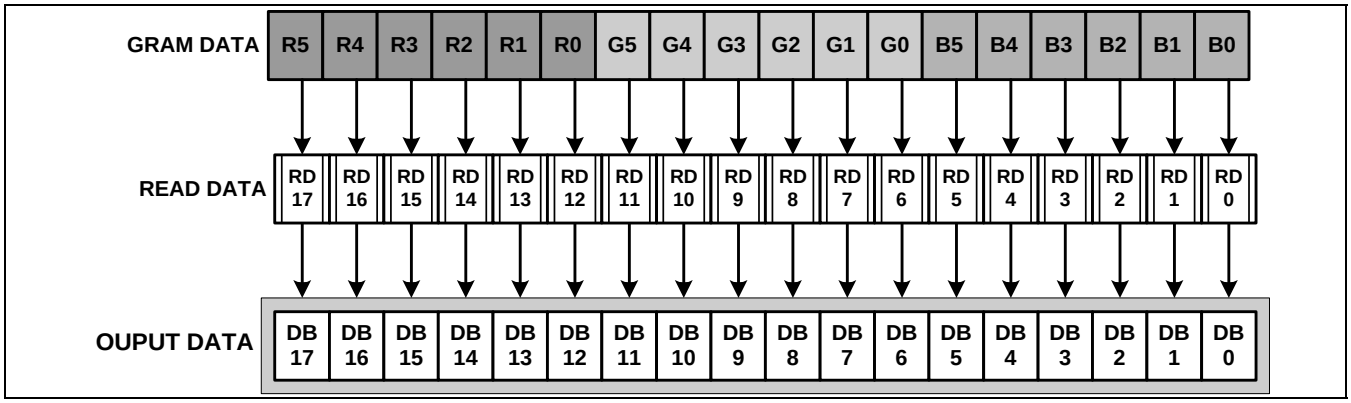

Figure 22. 18-bit System Interface for GRAM read

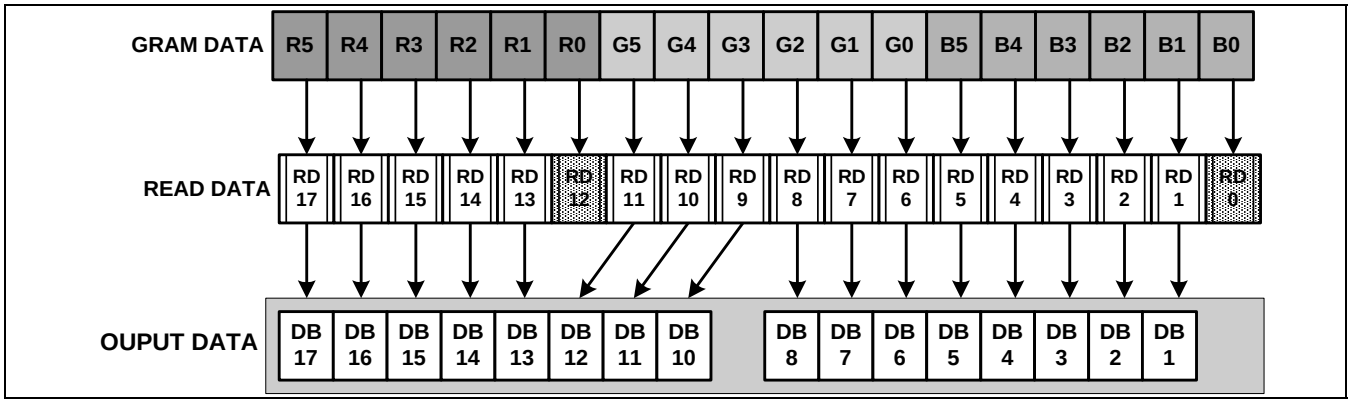

Figure 23. 16-bit System Interface for GRAM read

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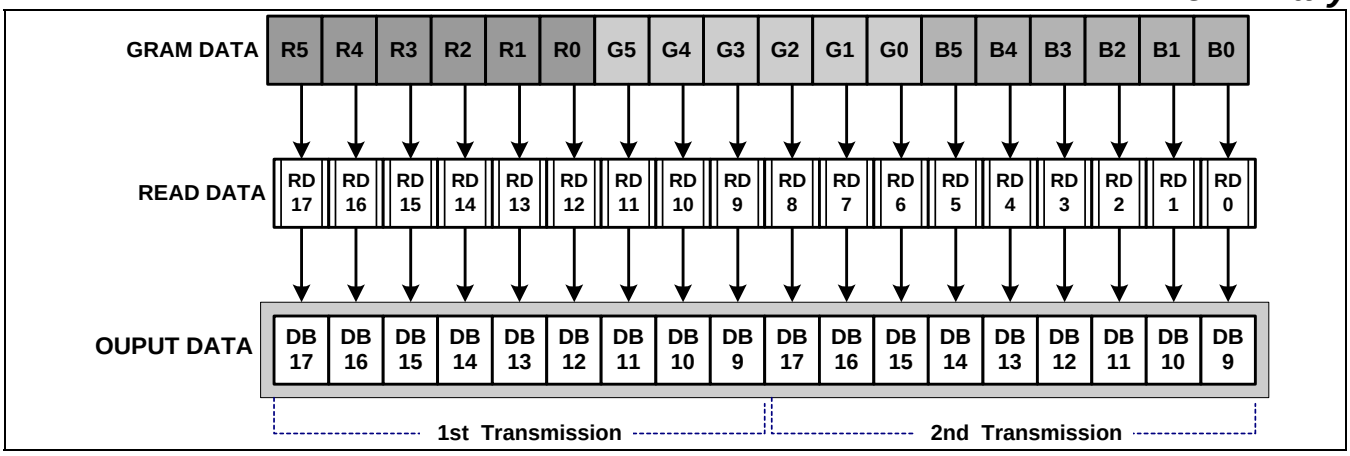

Figure 24. 9-bit System Interface for GRAM read

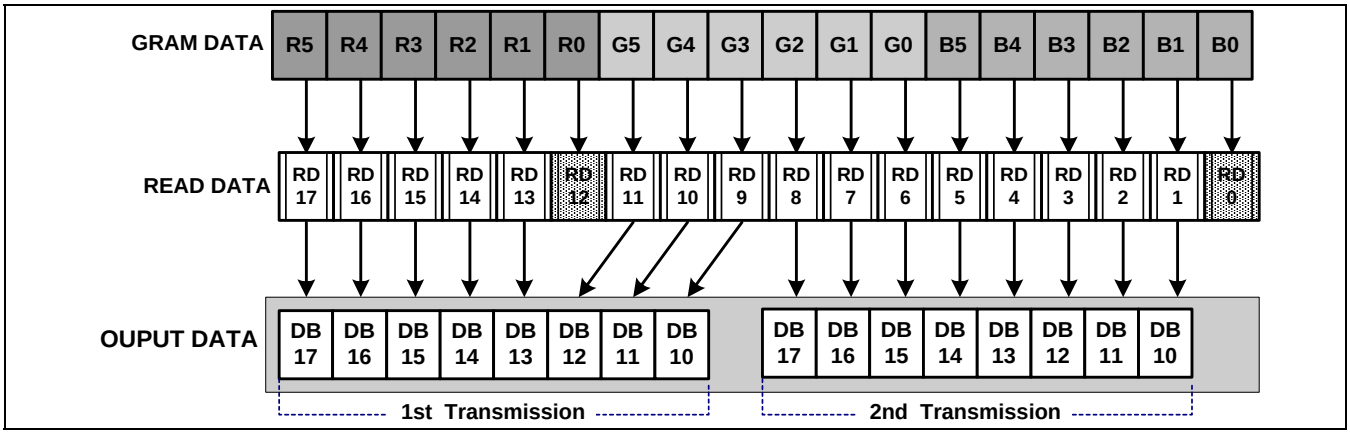

Figure 25. 8-bit System Interface for GRAM read

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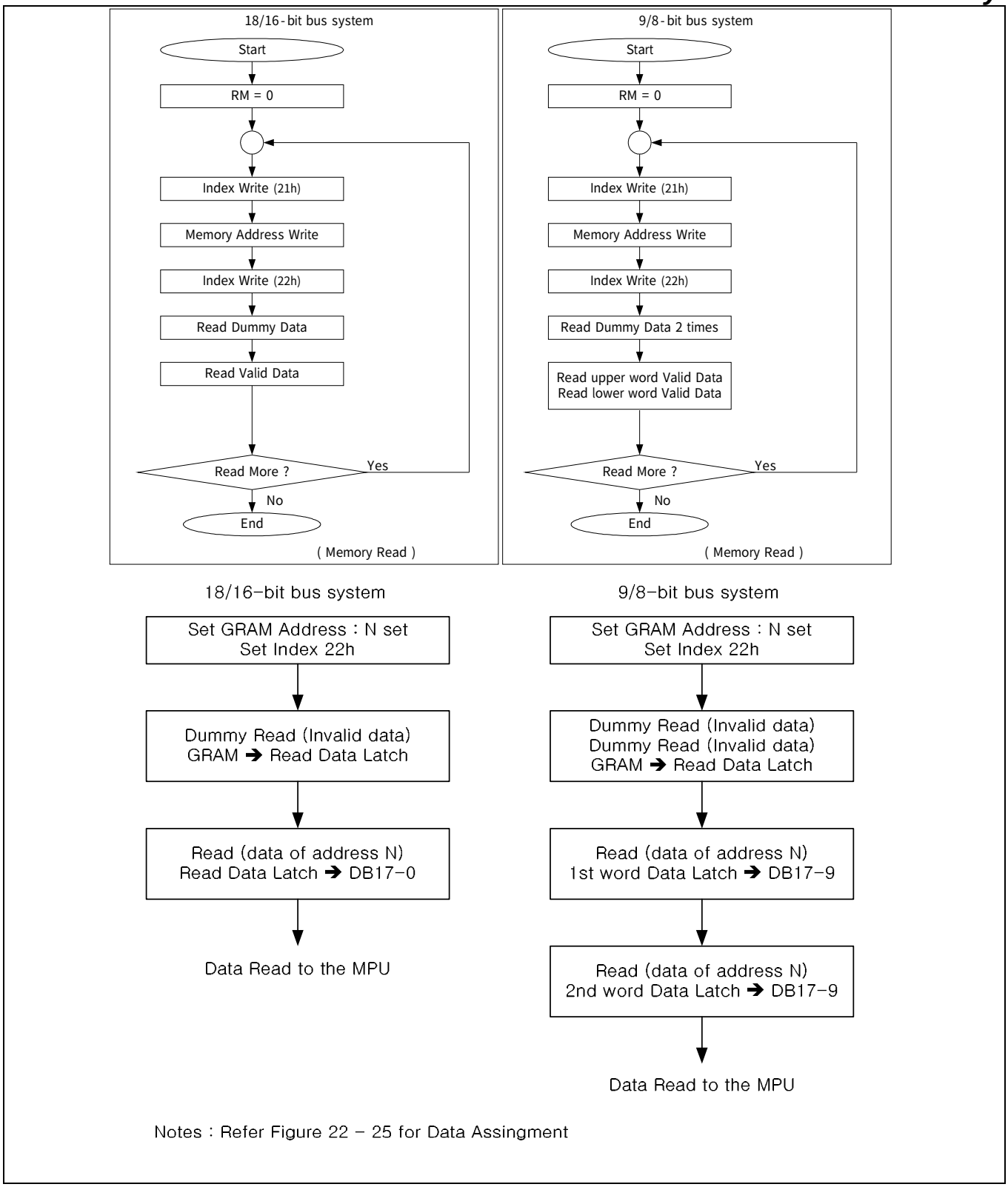

Figure 26. GRAM read sequence

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GAMMA CONTROL (R30H TO R39H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PKP12	PKP11	PKP10	RATIOP02	RATIOP01	RATIOP00	0	0	PKP02	PKP01	PKP00
W	1	0	0	0	0	0	PKP32	PKP31	PKP30	RATIOP12	RATIOP11	RATIOP10	0	0	PKP22	PKP21	PKP20
W	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
W	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
W	1	0	0	0	0	0	PKN12	PKN11	PKN10	RATION02	RATION01	RATION00	0	0	PKN02	PKN01	PKN00
W	1	0	0	0	0	0	PKN32	PKN31	PKN30	RATION12	RATION11	RATION10	0	0	PKN22	PKN21	PKN20
W	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40
W	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
W	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00
W	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00

PKP52–00: The gamma fine adjustment register for the positive polarity output

PRP12-00: The gradient adjustment register for the positive polarity output

PKN52-00: The gamma fine adjustment register for the negative polarity output

PRN12-00: The gradient adjustment register for the negative polarity output

VRP14-10: The amplitude adjustment register for the positive polarity output

VRN14-10: The amplitude adjustment register for the negative polarity output

VRP03-00: The reference adjustment register for the positive polarity output

VRN03-00: The reference adjustment register for the negative polarity output

RATIOP12-00: The ratio adjustment register for the positive polarity output.

RATION12-00: The ratio adjustment register for the negative polarity output.

For details, see the GAMMA ADJUSTMENT FUNCTION.

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GATE SCAN POSITION (R40H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	SCN5	SCN4	SCN3	SCN2	SCN1	SCN0

SCN5-0: Set the scanning starting position of the gate driver.

SCN5	SCN4	SCN3	SCN2	SCN1	SCN0	Scanning start position	
						GS=0	GS=1
0	0	0	0	0	0	G1	G320
0	0	0	0	0	1	G9	G312
0	0	0	0	1	0	G17	G304
:	:	:	:	:	:	:	:
1	0	0	1	0	0	G289	G32
1	0	0	1	0	1	G297	G24
1	0	0	1	1	0	G305	G16

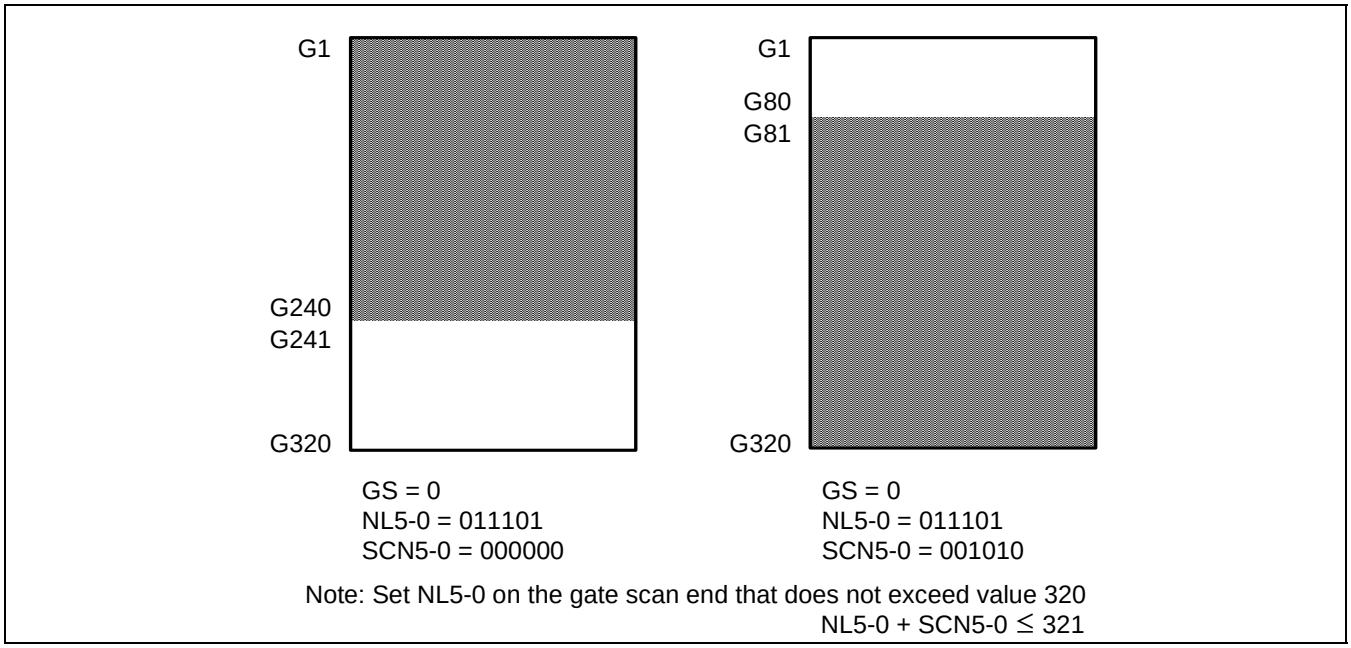

Figure 27. Relationship between NL and SCN set up value

Preliminary

VERTICAL SCROLL CONTROL (R41H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

VL8-0: Specify scroll length at the scroll display for vertical smooth scrolling. Any raster-row from the 1st to 320th can be scrolled according to the value of VL8-0. After 320th raster-row is displayed, the display restarts from the first raster-row. The scroll length (VL8-0) is valid when VLE1 = 1 or VLE2 = 1. The raster-row display is fixed when VLE2-1 = 00.

VL8	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scroll Length
0	0	0	0	0	0	0	0	0	0 raster-row
0	0	0	0	0	0	0	0	1	1 raster-row
0	0	0	0	0	0	0	1	0	2 raster-row
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
.	.	.	.	.	.	.	.	.	.
1	0	0	1	1	1	1	1	0	318 raster-row
1	0	0	1	1	1	1	1	1	319 raster-row

Note: Don't set any higher raster-row than 319 ("13F"H). Also, make sure that SS + VL < 512.

1st Screen Driving Position (R42h/R43h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10
W	1	0	0	0	0	0	0	0	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10

2nd Screen Driving Position (R44h/R45h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	SE28	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20
W	1	0	0	0	0	0	0	0	SS28	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

SS18–10: Specify the driving starting position for the first screen in a line unit. The LCD driving starts from the 'set value +1' gate driver.

SE18–10: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the 'set value + 1' gate driver. For instance, when SS18–10 = 07h and SE18–10 = 10h are set, the LCD driving is performed from G8 to G17, and non-display driving is performed for G1 to G7, G18, and others. Ensure that SS18–10 ≤ SE18–10 ≤ 13Fh. For details, see the SCREEN-DIVISION DRIVING FUNCTION section.

SS28–20: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the 'set value + 1' of the gate driver. The second screen is driven when SPT = 1.

SE28–20: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the 'set value + 1' of the gate driver. For instance, when SPT = 1, SS28–20 = 20h, and SE28–20 = 13Fh are set, the LCD driving is performed from G33 to G320. Ensure that SS18–10 ≤ SE18–10 ≤ SS28–20 ≤ SE28–20 ≤ 13Fh. For details, see the SCREEN-DIVISION DRIVING FUNCTION section.

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HORIZONTAL RAM ADDRESS POSITION (R46H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	HEA 7	HEA 6	HEA 5	HEA 4	HEA 3	HEA 2	HEA 1	HEA 0	HSA 7	HSA 6	HSA 5	HSA 4	HSA 3	HSA 2	HSA 1	HSA 0

VERTICAL RAM ADDRESS POSITION (R47H/R48H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	VEA 8	VEA 7	VEA 6	VEA 5	VEA 4	VEA 3	VEA 2	VEA 1	VEA 0
W	1	0	0	0	0	0	0	0	VSA 8	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0

HSA7-0/HEA7-0: Specify the horizontal start/end positions of a window for access in memory. Data can be written to the GRAM. The written data is from the address specified by HSA7-0 to the address specified by HEA 7-0. Note that an address must be set before RAM data are written. Ensure 00h ≤ HSA7-0 ≤ HEA7-0 ≤ EFh.

VSA8-0/VEA8-0: Specify the vertical start/end positions of a window for access in memory. Data can be written to the GRAM. The written data is from the address specified by VSA8-0 to the address specified by VEA8-0. Note that an address must be set before RAM data are written. Ensure 000h ≤ VSA8-0 ≤ VEA8-0 ≤ 13Fh.

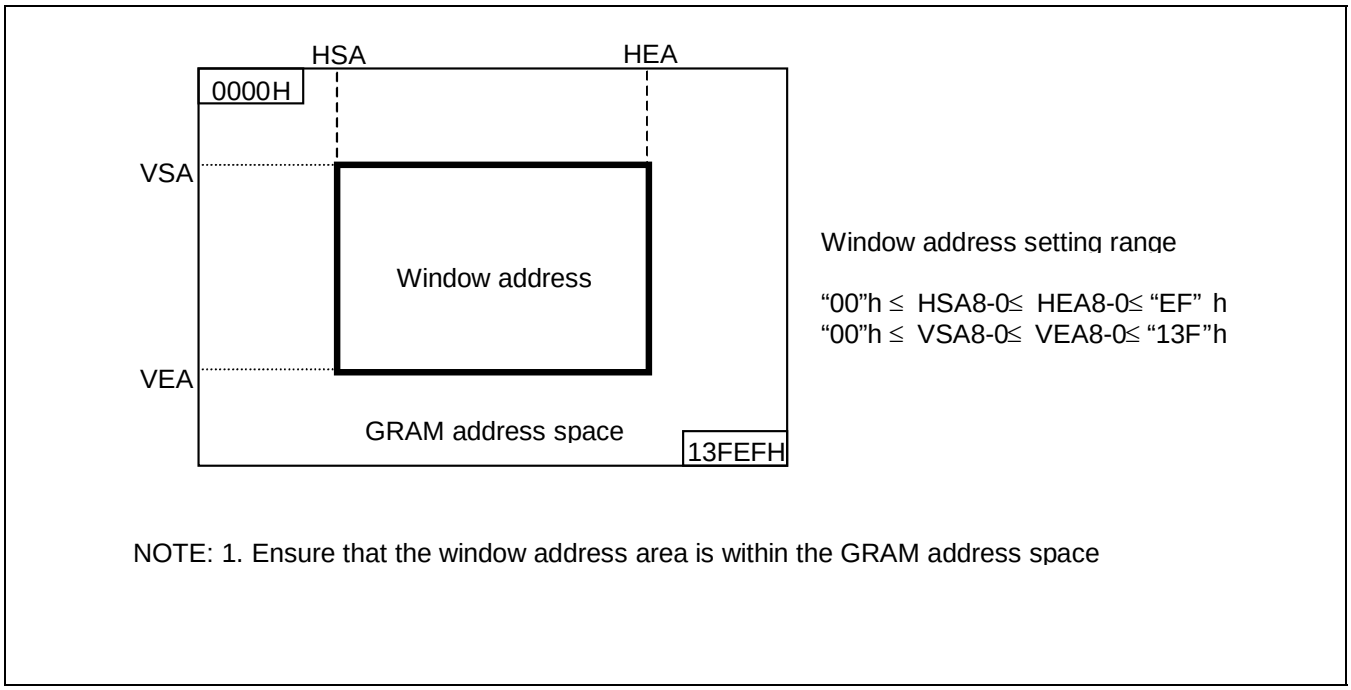

Figure 28. Window address setting range

Preliminary

CLIENT INITIATED WAKE-UP (R50H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VWAKE_EN

VWAKE_EN : When VWAKE_EN is 1, client initiated wake-up is enabled. But parameter data IB[15:1] must be "0000h", otherwise, client initiated wake-up is disabled.

MDDI LINK WAKE-UP START POSITION (R51H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	WKL8	WKL7	WKL6	WKL5	WKL4	WKL3	WKL2	WKL1	WKL0	0	WKF3	WKF2	WKF1	WKF0	0	0

WKF3-0 : When client initiated wake-up is used at MDDI, the frame position that data is updated is set by the value of WKF 3-0. The range of WKF is from '0000' to '1111'.
If WKF is '0000', data is updated at the first frame, and if "1111" data update starts after 16th frame.

WKF8-0 : When client initiated wakeup is used at MDDI, data is updated at the line the value of WKL7-0 in the frame that is set by WKF3-0. The range of WKL is from '000h' to '1FFh'.
If WKL is '000h', data is updated at the first line, and if WKL is '1FFh', data update starts at the 256th line.

Setting of WFK and WKL is needed for client-initiated link wake-up.
For example, WKF is "0010" and WKL is "0001", data is updated at second line of third frame.

SUB PANEL CONTROL(R60H / R61H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	SUB_SEL							
W	1	0	0	0	0	0	0	0	0	SUB_WR							

SUB_SEL : SUB_SEL is the index of main/sub panel selection. Initial value of SUB_SEL is '7Ah'.
In MDDI mode, If written register address is '7Ah' (initial state: SUB_SEL is '7Ah') and register data is '0001h', then main panel is selected, and if that is "0000h", then sub panel is selected.
Using SUB_SEL register, Main / Sub panel selection index change is possible.

SUB_WR : SUB_WR is the index of sub panel data write. Initial value of SUB_WR is '22h'.
When MDDI host transfer GRAM data to sub panel driver IC via video stream packet, SUB_WR (initially 22h), index for GRAM access is automatically transferred before GRAM data transfer.
When sub panel driver IC uses other address, 22h address have to be changed. Then user can change SUB_WR value from 22h to other value.

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MIE FUNCTION (R73H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	MIE_MODE[1]	MIE_MODE[1]	SEL_TABLE[1]	SEL_TABLE[0]	MIE_S_M	0	0	0	0	0	0	0	MIE_GAMMA[3]	MIE_GAMMA[2]	MIE_GAMMA[1]	MIE_GAMMA[0]

MIE_MODE1-0 : Specify the operating modes of MIE. The mode of MIE is updated before the transition of the next image frame to the value of MIE_MODE1-0.

MIE_MODE1-0	MIE mode	MIE work	MIE Output
00	Off	Off	Original Image
01	Halt	Off	Enhanced Image (last gamma value is applied)
10	Test	-	-
11	Normal	On	Enhanced Image

SEL_TABLE1-0: It specifies the selected image enhancement methods among 3 MIE methods. One image enhancement method has 9 gamma tables, one of which is selected by the gamma value calculated during the current frame transition. The image enhancement method of MIE is updated before the transition to the next frame image to the value of SEL_TABLE1-0.

SEL_TABLE1-0	MIE effect
00	Normal enhancement
01	Luminance emphasized enhancement
10	Contrast emphasized enhancement
11	Setting disabled

- MIE_S_M: If MIE_S_M is 1, it means that the input is a still image. Moreover, if MIE_S_M is 0, it means that the input is a motion image. When the input is a motion image, MIE slowly changes the gamma value over the next frames to avoid flickering. When the input is a still image, however, MIE changes the gamma value on the next frame. To make an enhanced still image, write same image in two frames. For any back-to-back frames, the latter image is enhanced by the gamma value that is calculated in the former frame.

- MIE_GAMMA3-0: It indicates the gamma value of MIE. MCU reads this gamma value by register read operation.

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GPIO CONTROL (R75H/R76H/R77H/R78H/R79H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	GPIO9	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0
W	1	0	0	0	0	0	0	GPIO_ CON9	GPIO_ CON8	GPIO_ CON7	GPIO_ CON6	GPIO_ CON5	GPIO_ CON4	GPIO_ CON3	GPIO_ CON2	GPIO_ CON1	GPIO_ CON0
W	1	0	0	0	0	0	0	GPCLR9	GPCLR8	GPCLR7	GPCLR6	GPCLR5	GPCLR4	GPCLR3	GPCLR2	GPCLR1	GPCLR0
W	1	0	0	0	0	0	0	GPIO_ EN9	GPIO_ EN8	GPIO_ EN7	GPIO_ EN6	GPIO_ EN5	GPIO_ EN4	GPIO_ EN3	GPIO_ EN2	GPIO_ EN1	GPIO_ EN0
W	1	0	0	0	0	0	0	GPPOL9	GPPOL8	GPPOL7	GPPOL6	GPPOL5	GPPOL4	GPPOL3	GPPOL2	GPPOL1	GPPOL0

GPIO: GPIO value. When GPIO is input mode, GPIO value is set to the register.
GPIO_CON: Control of GPIO, When GPIO_CON is “0”, then GPIO is input mode, and when “1”, then GPIO is output mode
GPCLR: After client is wakeup, GPIO
GPIO_EN: When GPIO is set input, if GPIO_EN is “1”, it acts as enable internal interrupt.
GPPOL: If the bit is set to “1”, GPIO interrupt happens at rising edge of GPIN, If set to “0”, it happens at falling edge.

For more information about these registers, refer to GPIO CONTROL section

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MTP CONTROL (R90H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	MTP_ LOAD	MTP_ WRB	MTP_ SELB	MTP_ INI

MTP_LOAD: If MTP_LOAD is set high (more 80ns), then MTP data latch from MTP cells to MTP port. Default is Low.

MTP_WRB: MTP Program Enable signal, Low active, it is only usable in STB or SLP mode. Default is high. R91h (Test Key command) should be set '8C'h before this command.

MTP_SELB: MTP value(MTP VCOMH) or Instruction value(R14H VCOMH) selection, If MTP_SELB =0, VCOMH of MTP Data is selected, else MTP_SELB = 1, the value of Instruction Register VCOMH(R14h) is selected.

MTP_INI: MTP initial(Erase) mode set
If MTP_INI = 1, MTP data are initialized to all zero.
R91h (Test Key command) should be set '8C'h before this command.

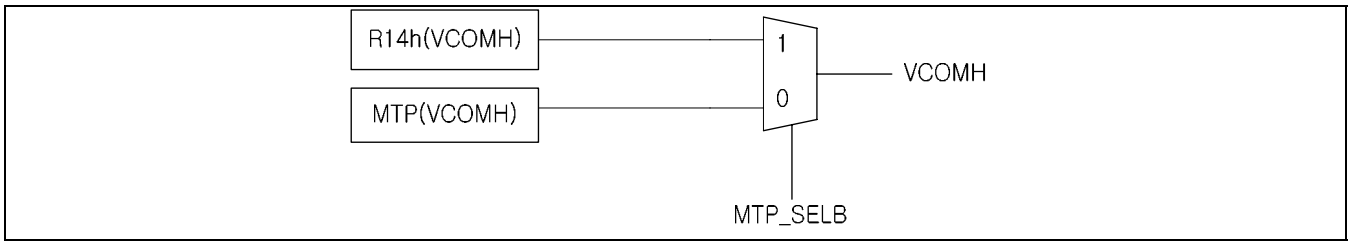

Figure 29. Relation between R14h and MTP

MTP VCOMH READ(R91H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	D6	D5	D4	D3	D2	D1	D0

This command reads the VCOM MTP Read bits.

Read 7bit data from MTP cells. D6 is protection bit, when MTP is programming , MSB should be high.
If MSB set to high, it cannot be write-protective , If you want to re-write, first Initialize MTP, then MTP D6 set to low

Bit	Descriptions
D6	Protection
D5	VCM[5]
D4	VCM[4]
D3	VCM[3]
D2	VCM[2]
D1	VCM[1]
D0	VCM[0]

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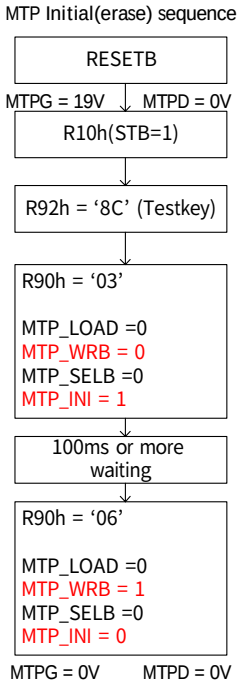
MTP TEST KEY COMMAND(R92H)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	1	0	0	0	1	1	0	0

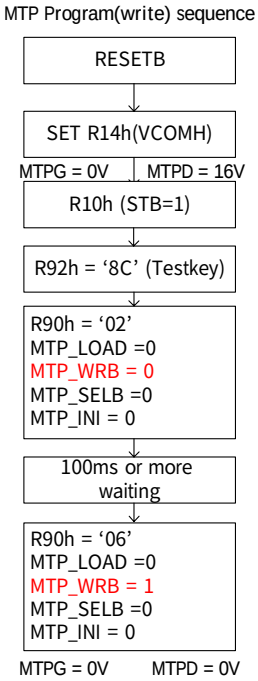
This command is a key of some operations (ex. MTP_INI, MTP_WRB)
If it is not matched with '8C', then some MTP command doesn't operate.



<MTP initialization Sequence>

1. Reset enable.
2. Power enable. MTP_G(=19V), MTP_D(=0V).
3. R92h command '8C'h parameter setting: Test key command is set.
4. R90h command set '0001'. (MTP initial & write on)
5. Hold the signal over 100ms
6. R90h command set '0100' (MTP initial & write off)
7. Remove the power MTP_G, MTP_D

Note: Initialization sequence is not related with D6 bit (protection bit), If user set R92h to '8Ch' , and when MTP_INI is low , then Initialization sequence is operated.



<MTP Program Sequence>

1. Reset enable.
2. Set values, which we wish to program, to VCOMH(R14h) register.
3. Power enable, MTP_G(=0V), MTP_D(=16V)
4. If protection bit is set, first of all, initialization should be proceeded
5. If protection bit is not set, then write process is enable.
6. R92h command '8C'h parameter setting: Test key command is set.
7. R90h command set '0000'. (MTP write on)
8. Hold the signal over 100ms
9. R90h command set '0100'. (MTP write off)
10. Remove the power, MTP_G, MTP_D.

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RESET FUNCTION

The S6D0139 is internally initialized by RESET input. The reset input must be held for at least 1 ms after the power is stable. Do not access the GRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

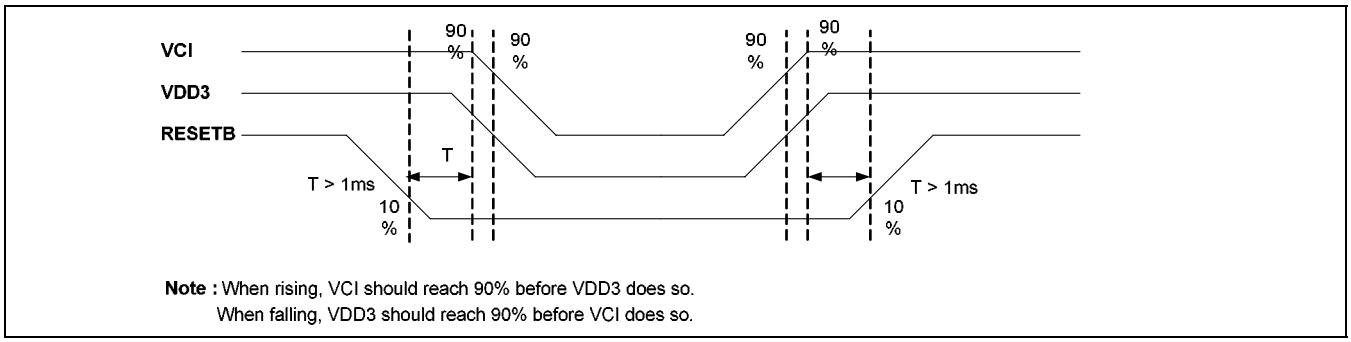

Figure 30. Input conditions for RESET

Instruction Set Initialization

1. Start oscillation executed (OSC = 1)
2. Driver output control (NL5–0 = 100111, SS = 0, GS = 0, EPL=0, VSPL=0, HSPL=0, DPL=0)
3. LCD driving AC control (FLD1-0 = 01, B/C = 0, EOR = 0)
4. Entry mode set (TRI = 0, DFM = 0, I/D1-0 = 11: Increment by 1: Horizontal move, BGR=0)
5. Display control 1 (PT1-0 = 00, VLE2–1 = 00: No vertical scroll, SPT = 0, GON = 0, CL = 0: 260K-color mode, REV = 0, D1–0 = 00: Display off)
6. Display control 2 (FP3-0 = 1000, BP3-0 = 1000)
7. Frame cycle control (NO1-0 = 00, SDT1-0 = 00, ECS1-0 = 00: no charge sharing, DIV1-0 = 00: 1-divided clock, RTN3-0 = 0000: 16 clock cycle in 1H period)
8. External display interface (RIM1-0=00:18-bit RGB interface, DM1-0=00: operated by internal clock, RM=0: system interface)
9. Power control 1 (SAP2-0 = 000, BT2-0 = 000, DC2–0 = 011, SLP = 0, STB = 0: Standby mode off)
10. Power control 2 (GVD5-0 = 000000, VC2-0 = 000)
11. Power control 3 (PON = 0, PON1 = 0, AON = 0)
12. Power control 4 (VCMR = 0, VCM5-0 = 000000, VML5-0 = 000000)
13. RAM address set (AD16–0 = 00000h)
14. Gamma control
    (PKP02–00 = 000, PKP12–10 = 000, PKP22–20 = 000, PKP32–30 = 000,
    PK42–40 = 000, PKP52–50 = 000, PRP02–00 = 000, PRP12–10 = 000)
    (PKN02–00 = 000, PKN12–10 = 000, PKN22–20 = 000, PKN32–30 = 000,
    PKN42–40 = 000, PKN52–50 = 000, PRN02–00 = 000, PRN12–10 = 000)
    VRP14–00 = 00000, VRP03–00 = 0000, VRN14–00 = 00000, VRN03–00 = 0000)
15. Gate scanning starting position (SCN5-0 = 000000)
16. Vertical scroll (VL8–0 = 00000000)
17. 1st screen division (SE18-10 = 100111111, SS18-10 = 00000000)
18. 2nd screen division (SE28-20 = 100111111, SS27-20 = 00000000)
19. Horizontal RAM address position (HEA7-0 = 11101111, HSA7-0 = 00000000)
20. Vertical RAM address position (VEA8-0 = 100111111, VSA8-0 = 00000000)

GRAM Data Initialization

GRAM is not automatically initialized by reset input but must be initialized by software while display is off (D1-0 = 00).

Output Pin Initialization

1. LCD driver output pins (Source output) : Output VSS level
   (Gate output) : Output VGL level
2. Oscillator output pin (OSC2): Outputs oscillation sign

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POWER SUPPLY CIRCUIT

The following figure shows a configuration of the voltage generation circuit for S6D0139. The step-up circuits consist of step-up circuits 1 to 3. Step-up circuit1 doubles the voltage supplied to VCI1 for AVDD level. Step-up circuit2 makes 2, 2.5 or 3times AVDD level for VGH level, and make -1.5, -2 or -3 times AVDD level for VGL level. Step-up circuit3 reverses the VCI1 level with reference to VSS or VBS and generates the VCL level. These step-up circuits generate power supplies AVDD, GVDD, VGH, VGL, VCL, and VCOM. Reference voltages GVDD, VCOM, and VGL for the grayscale voltage are amplified from the voltage adjustment circuit. Connect VCOM to the TFT panel.

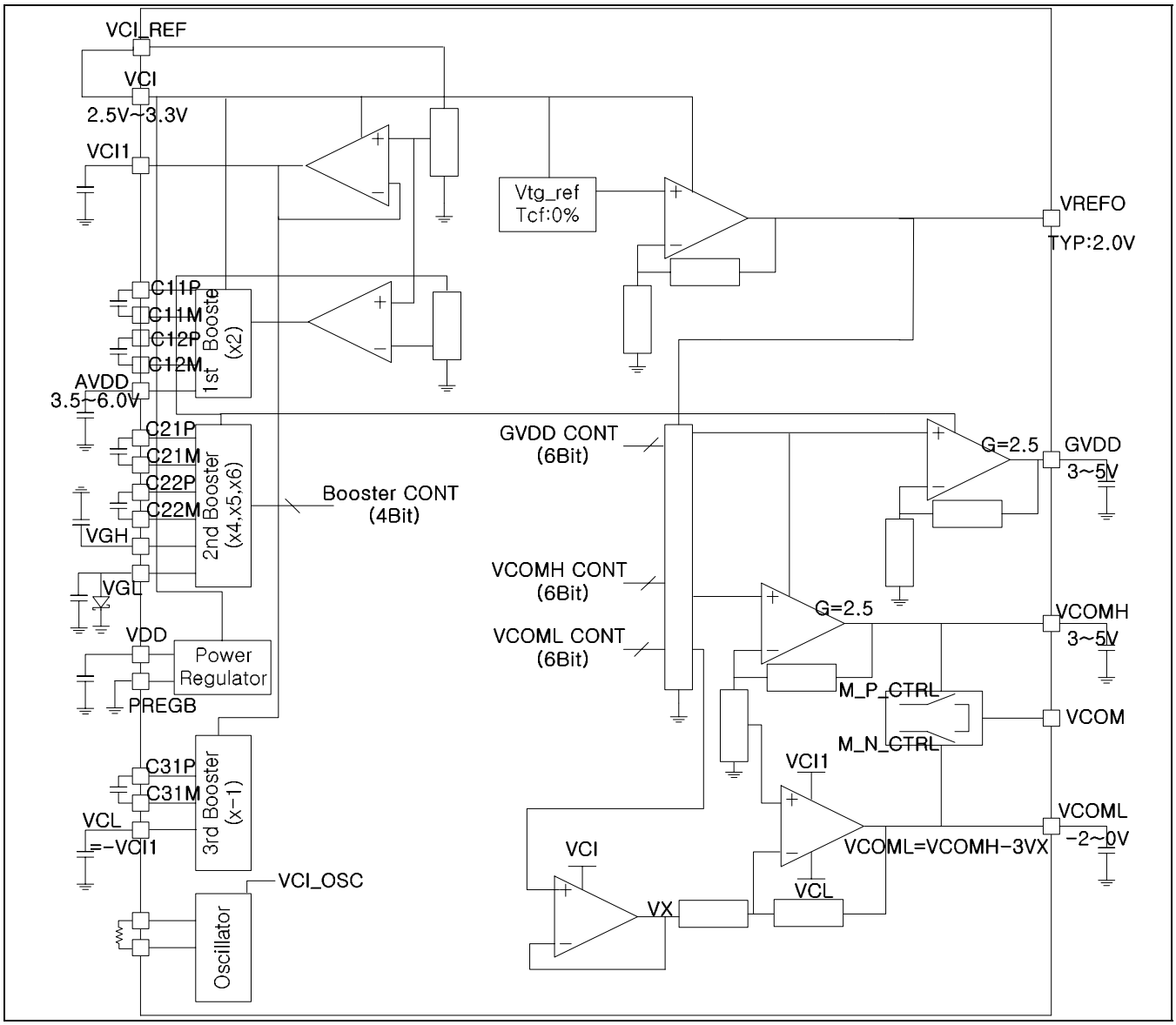


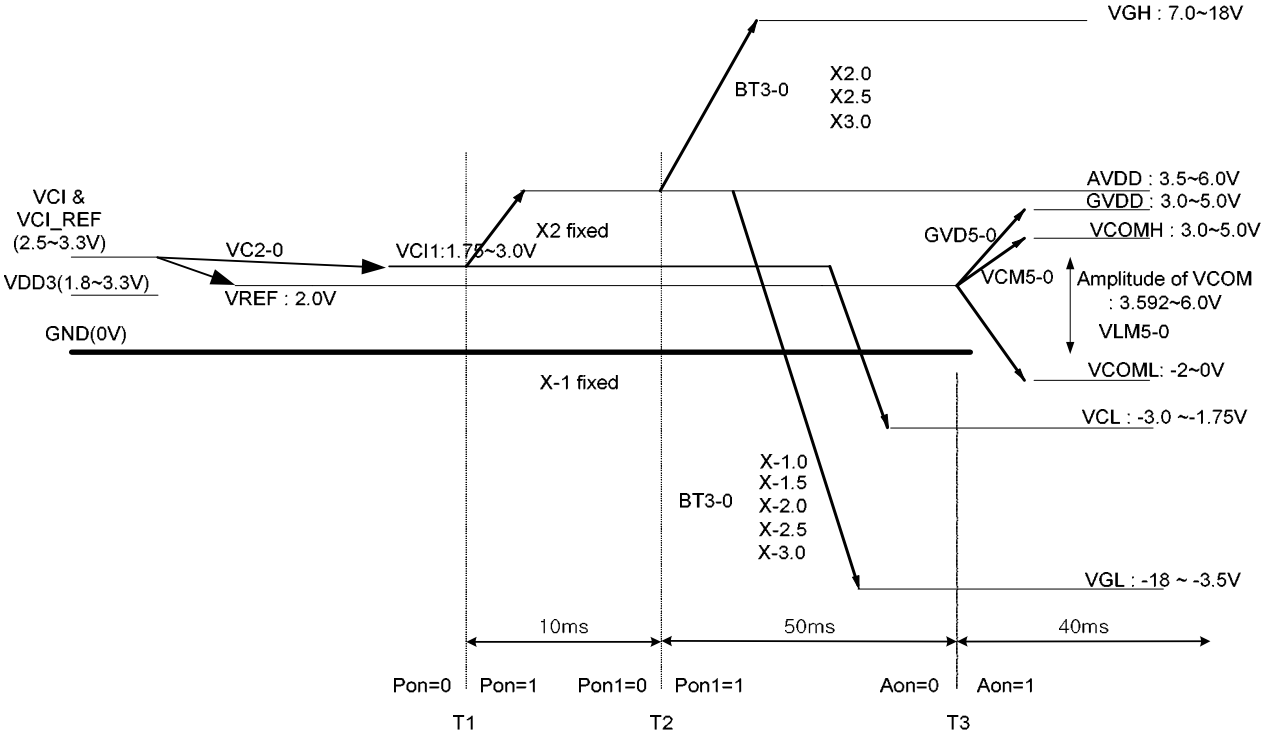
Figure 31. Configuration of the Internal Power-Supply Circuit

Notes:

Use the 1uF capacitor.

PATTERN DIAGRAMS FOR VOLTAGE SETTING

The following figure shows a pattern diagram for the voltage setting and an example of waveforms.



Note:

Adjust the conditions of AVDD-GVDD>0.5V with loads because they are different , depending on the display load to be driven.

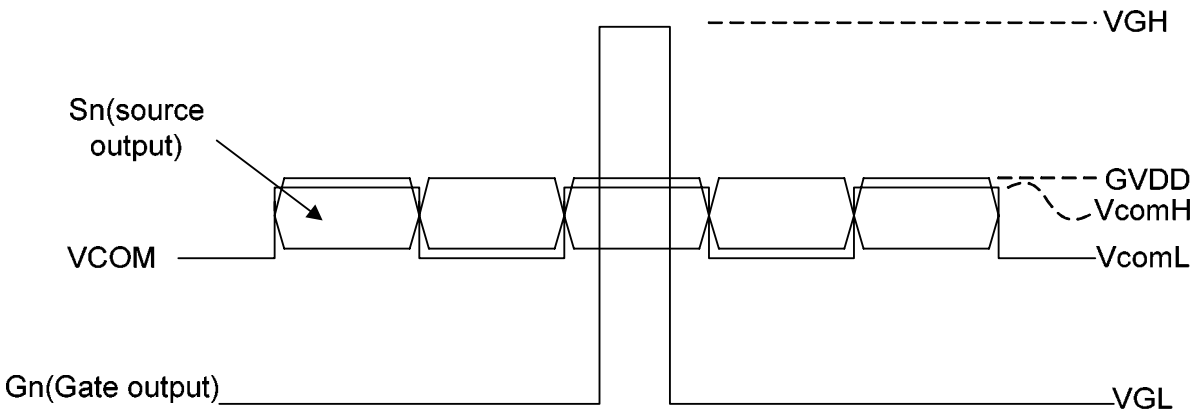


Figure 32. Pattern diagram and an example of waveforms

Preliminary

SET UP FLOW OF POWER SUPPLY

Apply the power in a sequence as shown in the following figure. The stable time of the oscillation circuit, step-up circuit, and operational amplifier depends on the external resistor or capacitance.

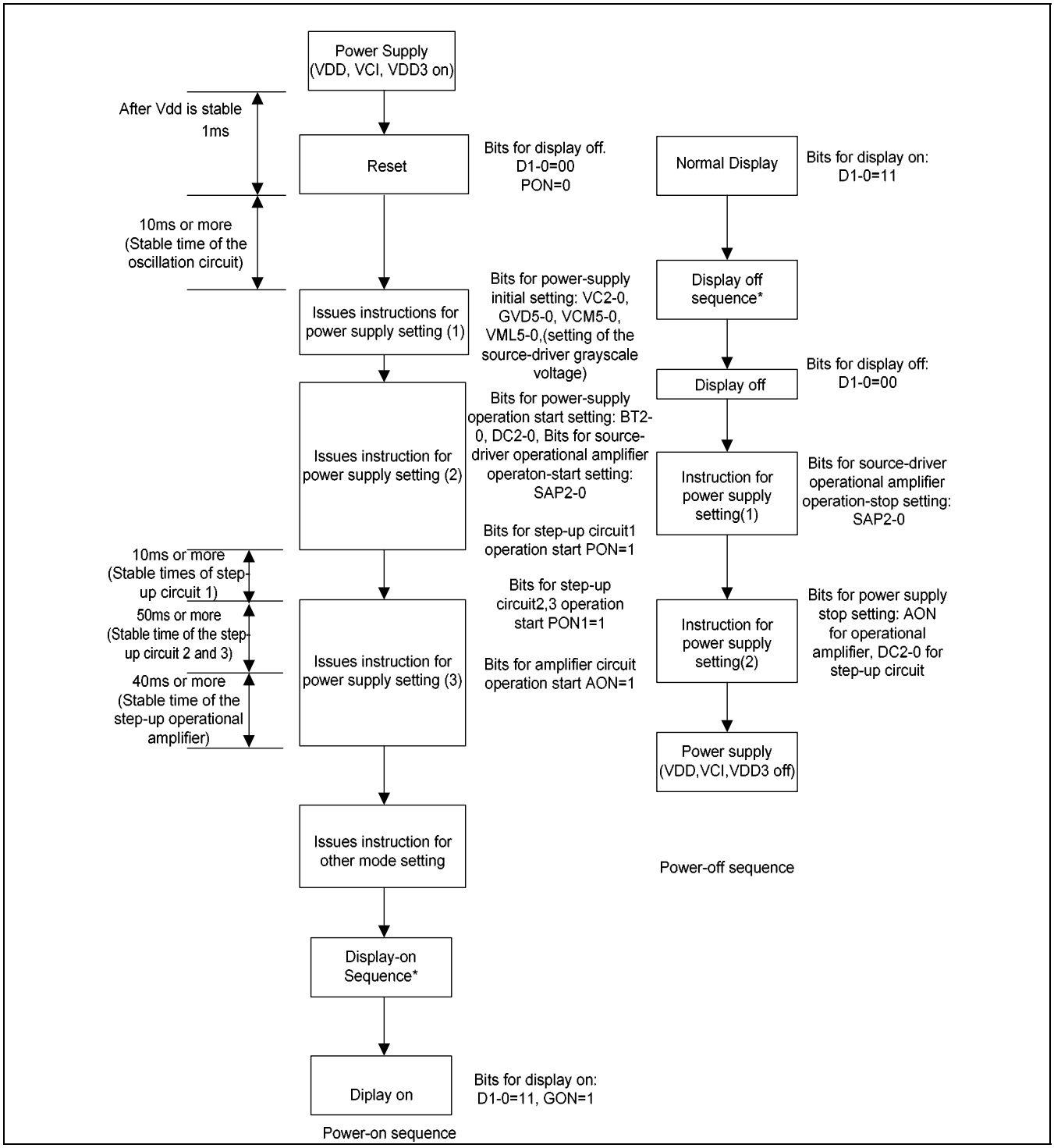
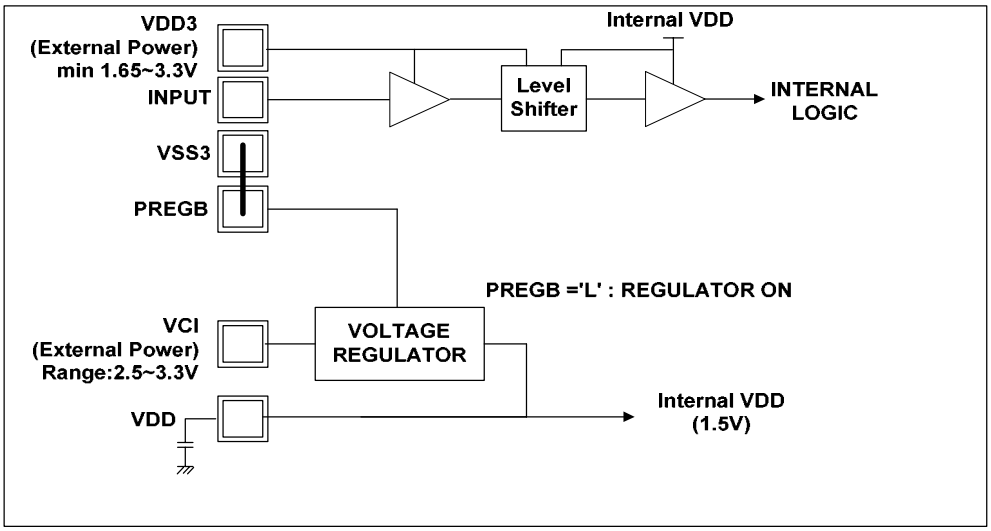


Figure 33. Set up Flow of Power Supply

Preliminary

VOLTAGE REGULATION FUNCTION

The S6D0139 have internal voltage regulator. Voltage regulation function is controlled by PREGB pin.
If PREGB= “H”, voltage regulation is stopped. PREGB= “L” enables internal voltage regulation function.
By use of this function, internal logic circuit damage can be prohibited. Furthermore, power consumption can also be reduced by this function. Detailed function description and application setup is described in the following diagram.



(a) Voltage regulation function enabled

Figure 34. Voltage regulation function

Preliminary

INTERFACE SPECIFICATION

The S6D0139 incorporates a system interface, which is used to set instructions, and an external display interface, which is used to display motion pictures. Selecting these interfaces to match the screen data (motion picture or still picture) enables efficient transfer of data for display.

The external display interface includes RGB and VSYNC interface. This allows flicker-free screen update.
When RGB interface is selected, the synchronization signals (VSYNC, HSYNC, and DOTCLK) are available for use in operating the display. The data for display (PD17-0) is written according to the values of the data enable signal (ENABLE) in synchronization with the VSYNC, HSYNC, and DOTCLK signals. In addition, using the window address function enables rewriting only to the internal RAM area to display motion pictures. Using this function also enables simultaneously display of the motion picture area and the RAM data that was written.

The internal display operation is synchronized with the frame synchronization signal (VSYNC) in VSYNC interface mode. When writing to the internal RAM is done within the required time after the falling edge of VSYNC, motion pictures can be displayed via the conventional interface. There are some limitations on the timing and methods of writing to RAM. See the section on the external display interface.

The S6D0139 has four operation modes for each display state. These settings are specified by control instructions for external display interface. Transitions between modes should follow the transition flow.

Table 31. Display Operation Mode and RAM Access Selection

Operation Mode	RAM Access Selection (RM)	Display Operation Mode (DM1-0)
Internal Clock Operation (Displaying still picture)	System interface (RM=0)	Internal clock operation (DM1-0=00)
RGB interface (Displaying motion picture)	RGB interface (RM=1)	RGB interface (DM1-0=01)
VSYNC interface (Displaying motion Pictures)	System interface (RM=0)	VSYNC interface (DM1-0=10)
MDDI interface (Displaying motion Pictures)	System interface (RM=0)	MDDI interface (DM1-0=00,10)

NOTES: 1) Instruction registers can only be set via system interface.
2) RGB interface and VSYNC interface cannot be used at the same time.
3) RGB interface mode cannot be set during operations.
4) For mode transitions, see the section on the external display interface.

Preliminary

SYSTEM INTERFACE

S6D0139 is enabled to set instruction and access to RAM by selecting IM3/2/1/0 pin in the system interface mode.

Table 29. IM Bits and System Interface

IM3	IM2	IM1	IM0	System Interface	DB Pin
0	0	0	0	68-system 16-bit interface	DB17 to10, 8 to1
0	0	0	1	68-system 8-bit interface	DB17 to10
0	0	1	0	80-system 16-bit interface	DB17 to10, 8 to1
0	0	1	1	80-system 8-bit interface	DB17 to10
0	1	0	*	Serial peripheral interface (SPI)	DB1 to 0
0	1	1	*	Setting disabled	-
1	0	0	0	68-system 18-bit interface	DB17 to 0
1	0	0	1	68-system 9-bit interface	DB17 to 9
1	0	1	0	80-system 18-bit interface	DB17 to 0
1	0	1	1	80-system 9-bit interface	DB17 to 9
1	1	0	*	MDDI interface	-

68/80-SYSTEM 18-BIT BUS INTERFACE

When you set the IM3/2/1/0 (interface mode) to the VDD3/VSS/VSS/VSS level, the S6D0139 allows 68-system 18-bit parallel data transfer. When you set the IM3/2/1/0 to the VDD3/VSS/VDD3/VSS level, the S6D0139 allows 80-system 18-bit parallel data transfer.

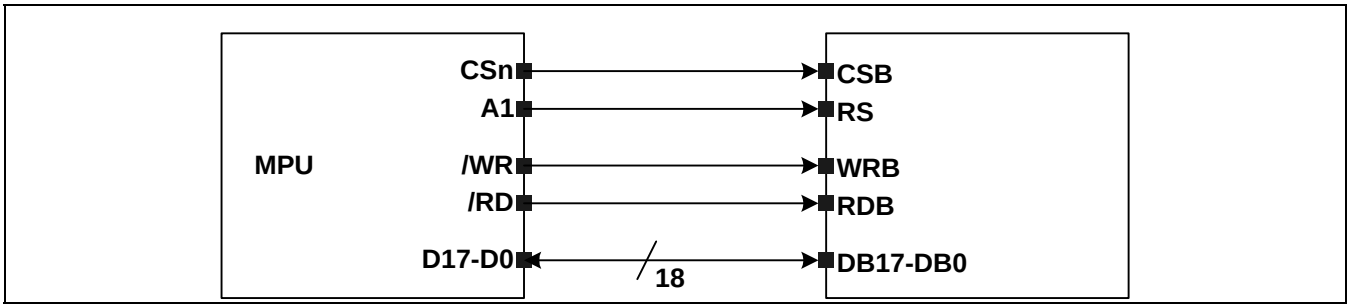


Figure 35. Interface with the 18-bit Microcomputer

68/80-SYSTEM 18-bit interface data FORMAT

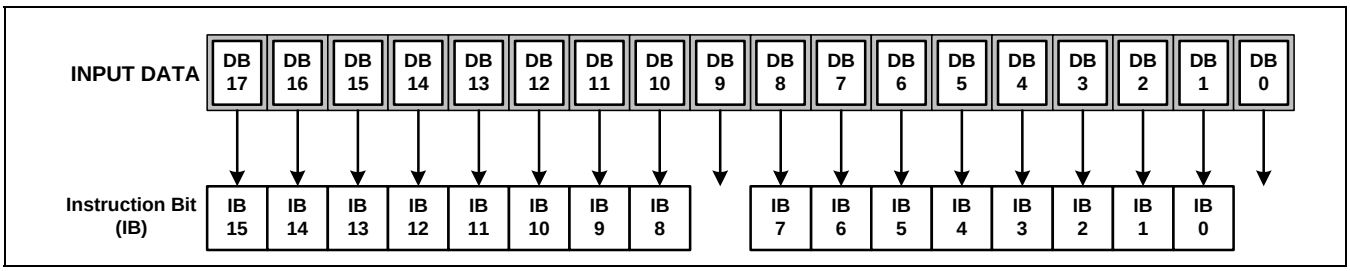


Figure 36. Instruction format for 18-bit Interface

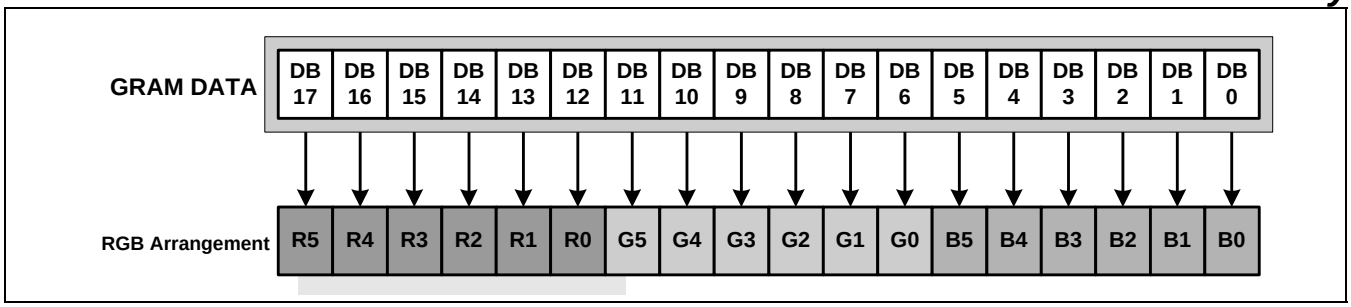


Figure 37. RAM Data Write format for 18-bit Interface

68/80-SYSTEM 16-BIT BUS INTERFACE

When you set the IM3/2/1/0 (interface mode) to the VSS/VSS/VSS/VSS level, the S6D0139 allows 68-system 16-bit parallel data transfer. When you set the IM3/2/1/0 to the VSS/VSS/VDD3/VSS level, the S6D0139 allows 80-system 16-bit parallel data transfer.

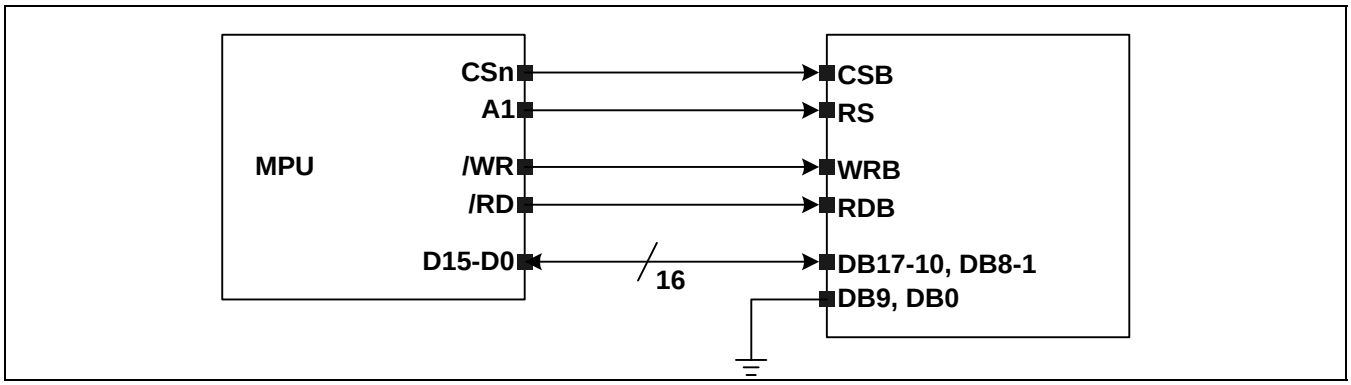


Figure 38. Interface with the 16-bit Microcomputer

68/80-SYSTEM 16-bit interface data FORMAT

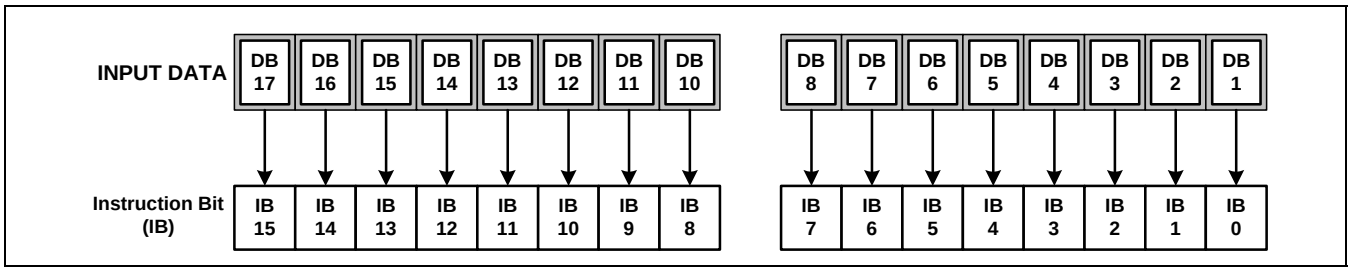


Figure 39. Instruction format for 16-bit Interface

Preliminary

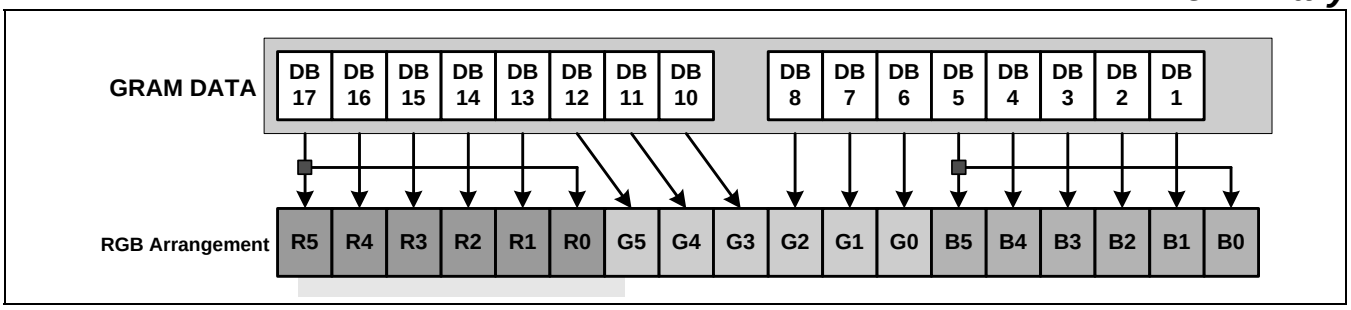


Figure 40. RAM Data Write format for 16-bit Interface

Preliminary

68/80-SYSTEM 9-BIT BUS INTERFACE

When you set the IM3/2/1/0 (interface mode) to the VDD3/VSS/VSS/VDD3 level, the S6D0139 allows 68-system 9-bit parallel data transfer using pins DB17–DB9. When the IM3/2/1/0 is set to the VDD3/VSS/VDD3/VDD3 level, the S6D0139 allows 80-system 9-bit parallel data transfer. The 16-bit instructions and RAM data are divided into nine upper/lower bits and the transfer starts from the upper nine bits. Fix unused pins DB8–DB0 to the VDD 3 or VSS level. Note that the upper bytes must also be written when the index register is written.

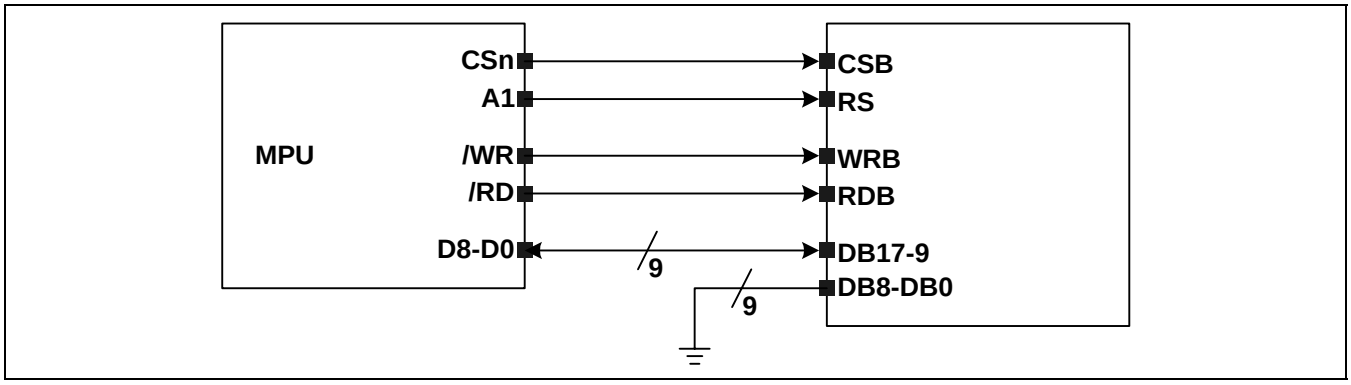


Figure 41. Interface to 9-bit Microcomputer

68/80-SYSTEM 9-bit interface data FORMAT

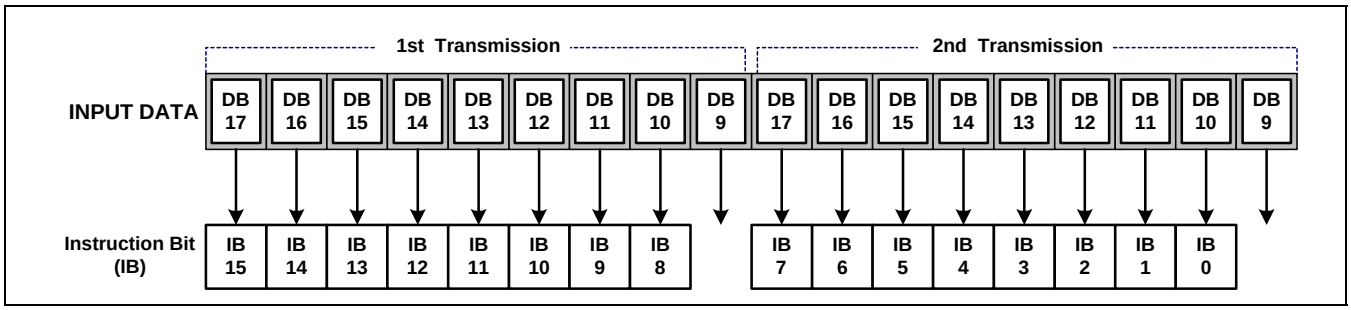


Figure 42. Instruction format for 9-bit Interface

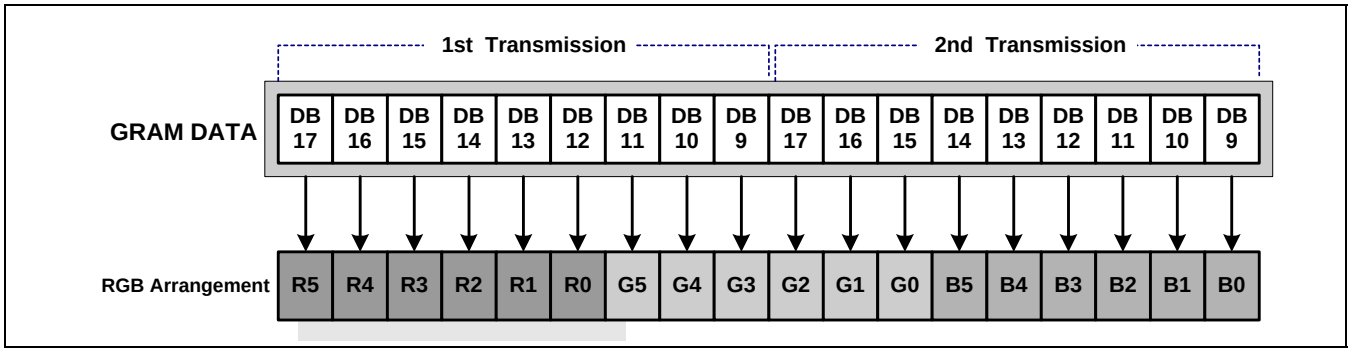


Figure 43. RAM Data Write format for 9-bit Interface

Preliminary

68/80-SYSTEM 8-BIT BUS INTERFACE

When you set the IM3/2/1/0 (interface mode) to the VSS/VSS/VSS/VDD3 level, the S6D0139 allows 68-system 8-bit parallel data transfer. When you set the IM3/2/1/0 to the VSS/VSS/VDD3/VDD3 level, the S6D0139 allows 80-system 8-bit parallel data transfer. The 16-bit instructions and RAM data are divided into eight upper/lower bits and the transfer starts from the upper eight bits. Fix unused pins DB9–DB0 to the VDD3 or VSS level. Note that the upper bytes must also be written when the index register is written.

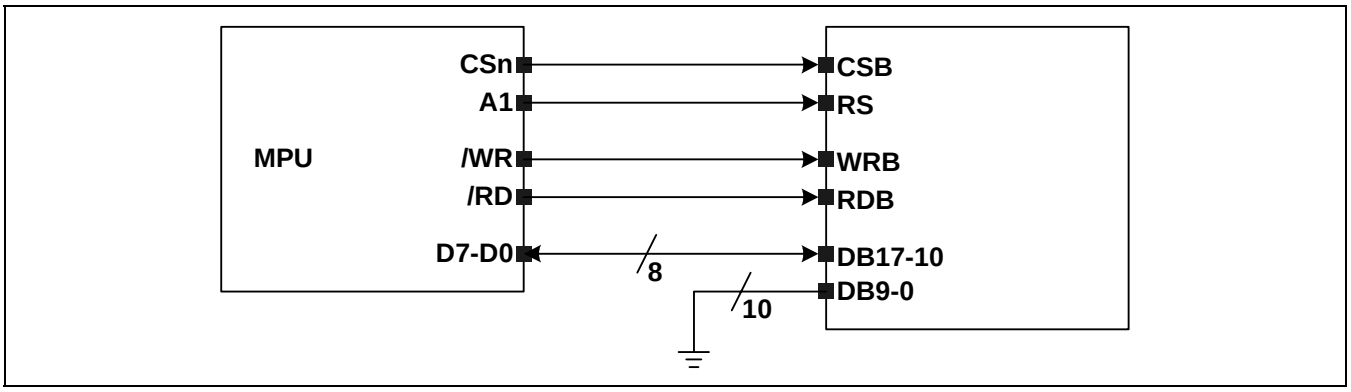


Figure 44. Interface with the 8-bit Microcomputer

68/80-SYSTEM 8-bit interface data FORMAT

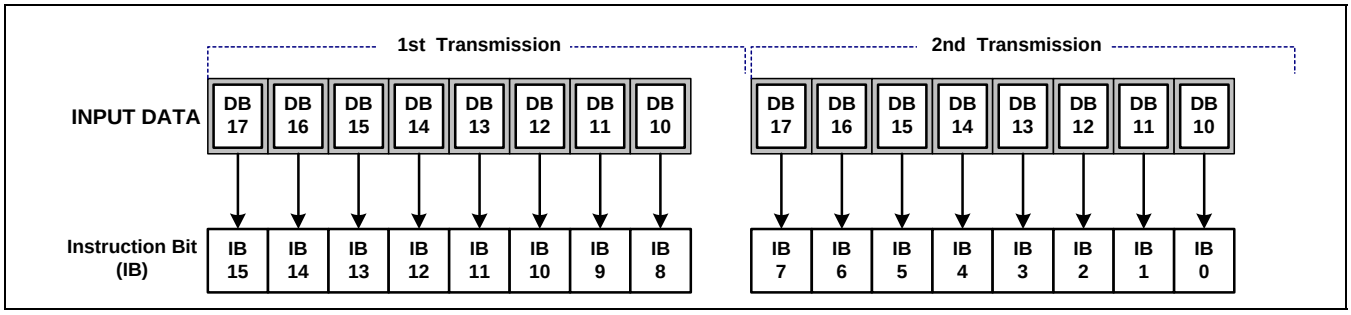


Figure 45. Instruction format for 8-bit Interface

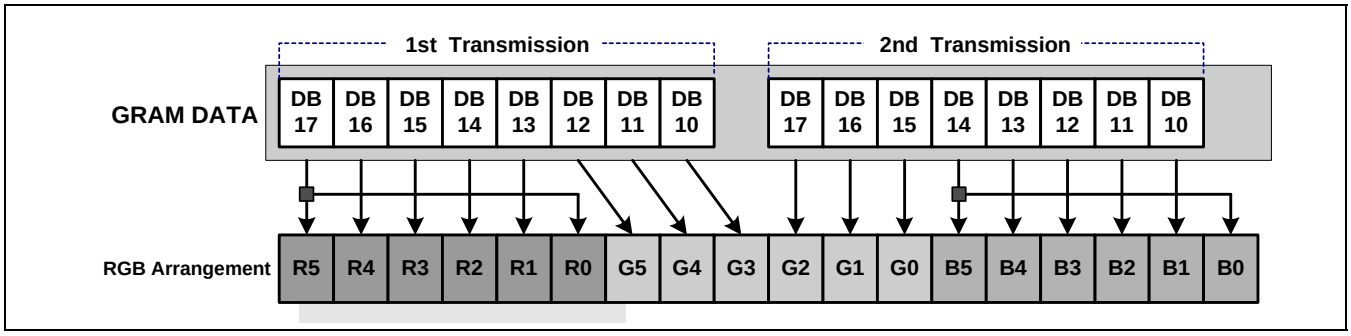


Figure 46. RAM Data Write format for 8-bit Interface

Preliminary

SERIAL DATA TRANSFER

When you set the IM3 pin to the VSS level, the S6D0139 allows serial peripheral interface (SPI) transfer, using the chip select line (CS*), serial transfer clock line (SCL), serial input data (SDI), and serial output data (SDO). For a serial interface, the IM0/ID pin function uses an ID pin. If the chip is set up for serial interface, the DB17-2 pins are not used and the pins must be fixed at VDD3 or VSS. The S6D0139 initiates serial data transfer by transferring the start byte at the falling edge of CSB input. It ends serial data transfer at the rising edge of CSB input. The S6D0139 is selected when the 6-bit chip address in the start byte matches the 6-bit device identification code that is assigned to the S6D0139. When selected, the S6D0139 receives the subsequent data string. The ID pin can determine the LSB of the identification code. The five upper bits must be 01110. Two different chip addresses must be assigned to a single S6D0139 because the seventh bit of the start byte is used as a register select bit (RS): When RS = 0, data can be written to the index register or status can be read, and when RS = 1, an instruction can be issued or data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit). The data is received when the R/W bit is 0, and is transmitted when the R/W bit is 1.

After receiving the start byte, the S6D0139 receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. All S6D0139 instructions are 16 bits. Two bytes are received with the MSB first (DB17 to 0), and the instructions are internally executed. After the start byte has been received, the next bytes are fetched of which, the first byte is fetched as the upper eight bits of the instruction and the second byte is fetched as the lower eight bits of the instruction. Four bytes of RAM read data after the start byte are invalid. The S6D0139 starts to read correct RAM data from the fifth byte.

Table 30. Start Byte Format

Transfer bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

NOTE: ID bit is selected by the IM0/ID pin.

Table 31. RS and R/W Bit Function

RS	RW	Function
0	0	Set index register
0	1	Read status
1	0	Writes instruction or RAM data
1	1	Reads instruction or RAM data

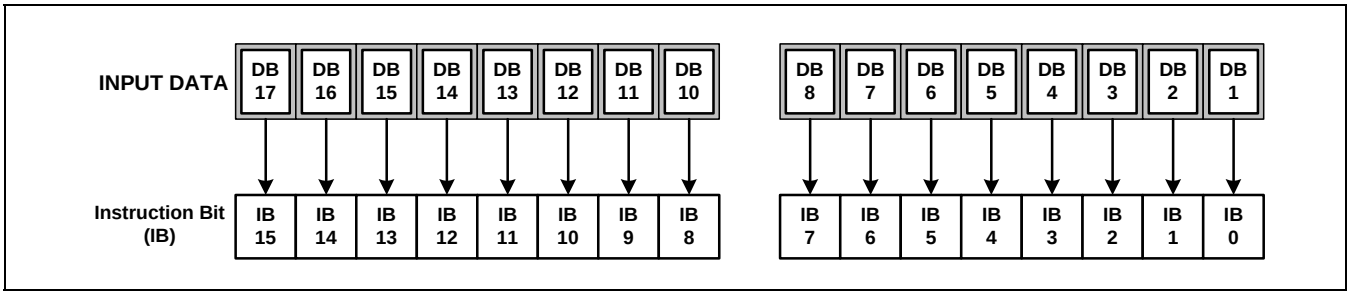


Figure 47. Instruction format for Serial Data Transfer

Preliminary

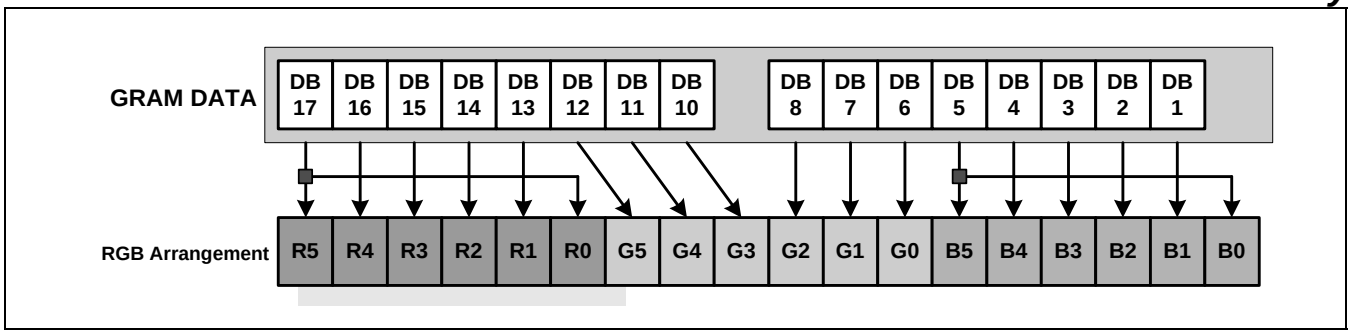


Figure 48. RAM Data Write format for Serial Data Transfer

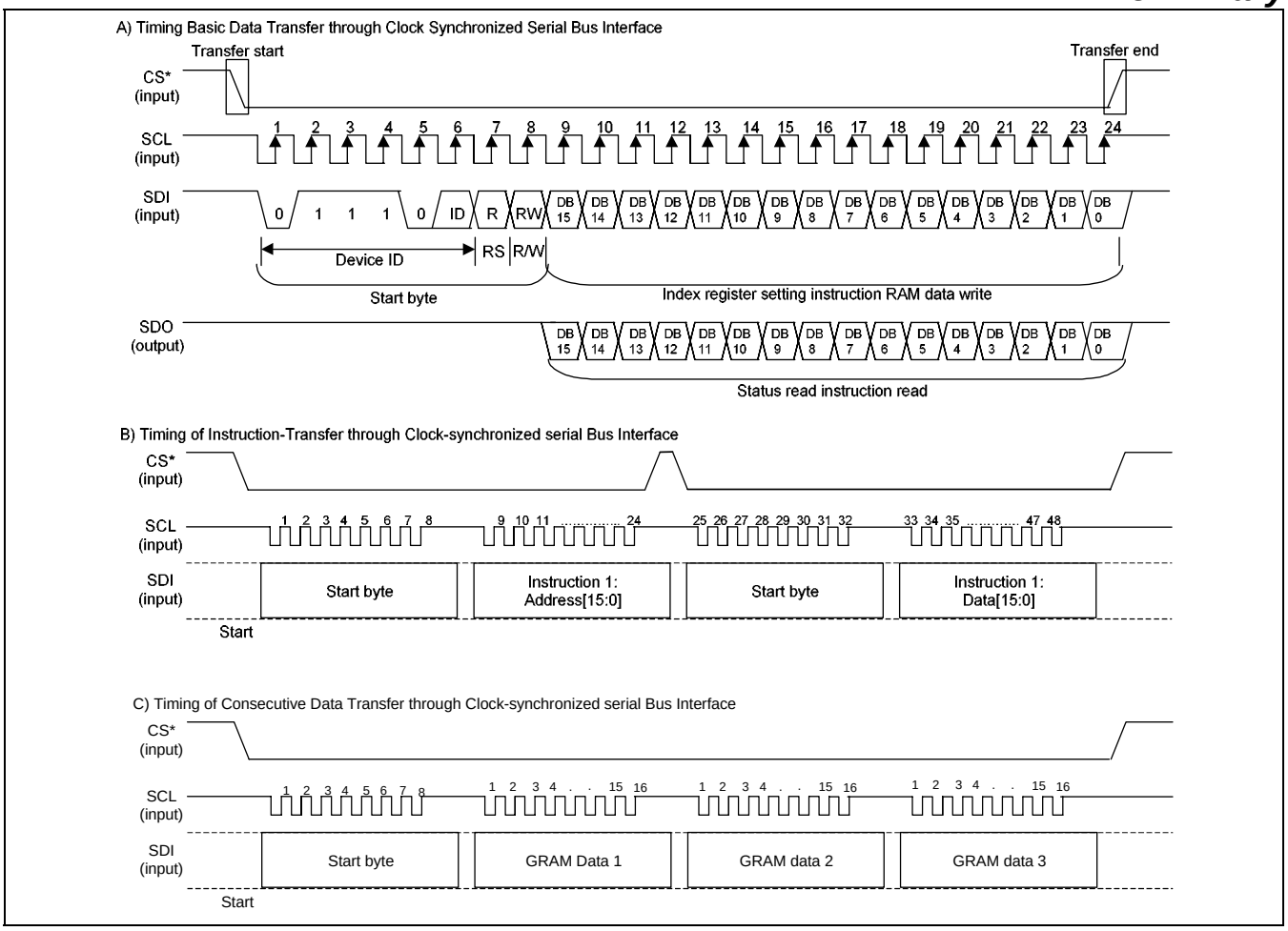
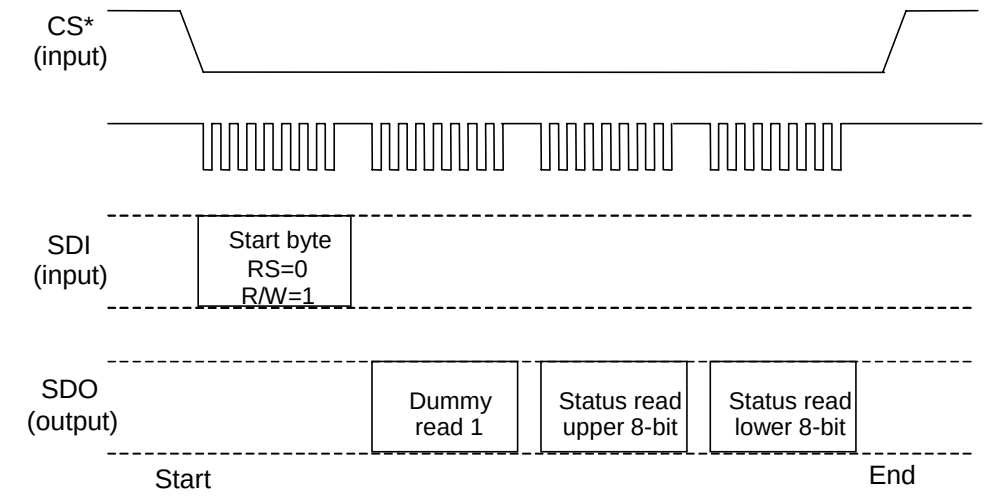


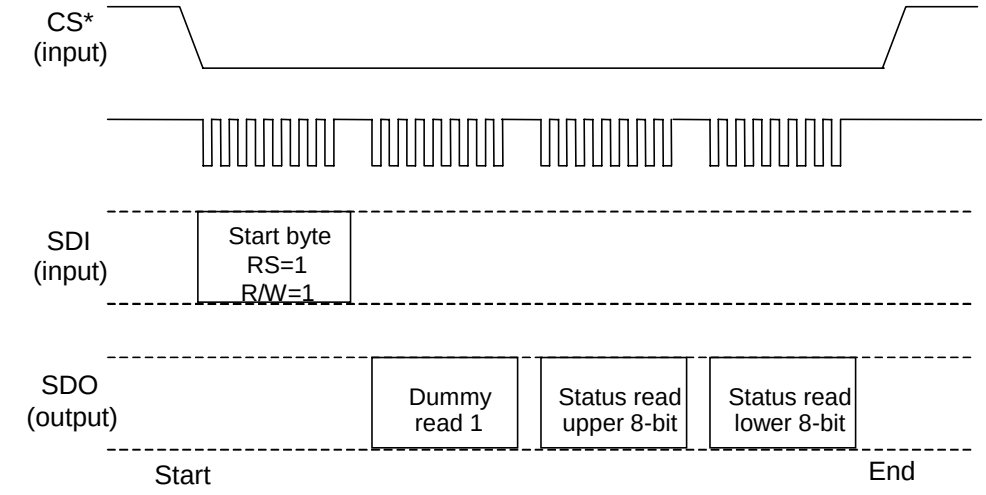
Figure 49. Procedure for transfer on clock synchronized serial bus interface

D) Status Read



NOTE: 2-byte of the RAM read after the start byte is invalid.
The S6D0139 starts to read the correct RAM data from the third data.

E) Instruction Read



NOTE: 2-byte of the RAM read after the start byte is invalid.
The S6D0139 starts to read the correct RAM data from the third data.

Figure 50. Procedure for transfer on clock synchronized serial bus interface (continued)

Preliminary

VSYNC INTERFACE

The S6D0139 incorporates VSYNC interface, which enables motion pictures to be displayed with only the conventional system interface and the frame synchronization signal (VSYNC). This interface requires minimal changes from the conventional system to display motion pictures.

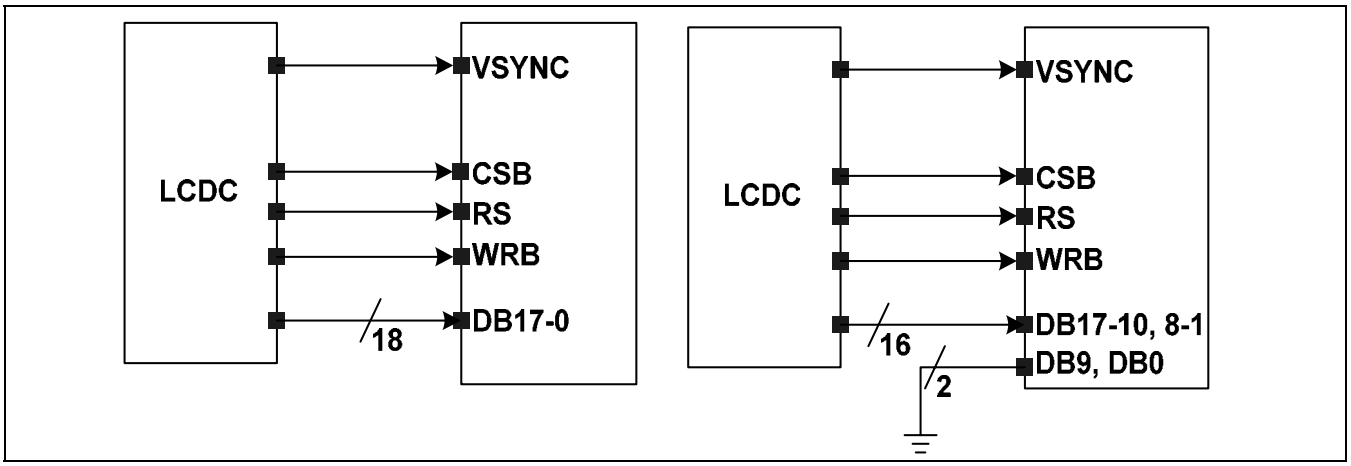


Figure 51. VSYNC Interface 18bit / 16bit

When DM1-0=”10” and RM=”0”, VSYNC interface is available. In this interface the internal display operation is synchronized with VSYNC. Data for display is written to RAM via the system interface with higher speed than for internal display operation. This method enables flicker-free display of motion pictures with the conventional interface.

Display operation can be achieved by using the internal clock generated by the internal oscillator and the VSYNC input. Since, all the data for display is written to RAM, only the data to be rewritten is transferred. This method reduces the amount of data transferred during motion picture display operation.

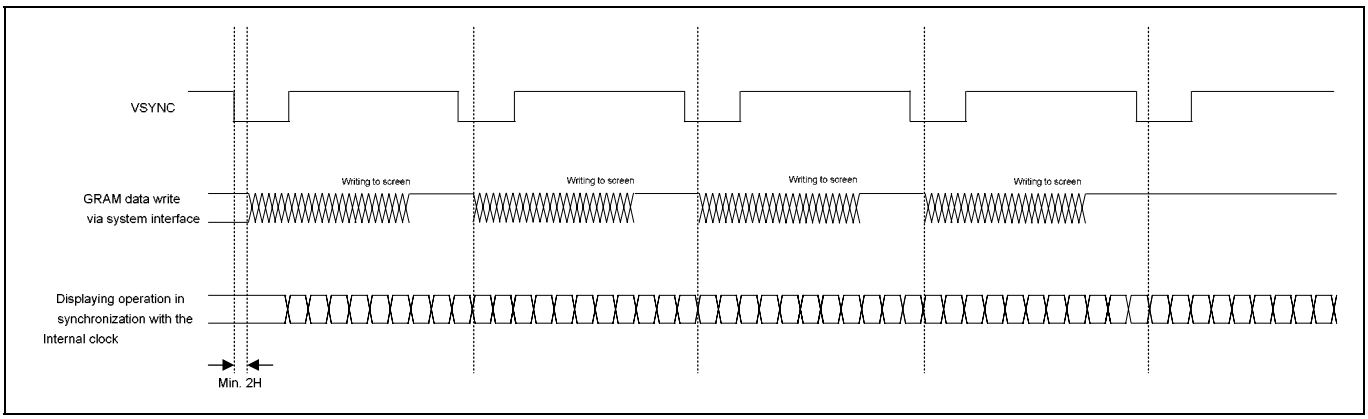


Figure 52. Motion Picture Data Transfer via VSYNC Interface

VSYNC interface requires taking the minimum speed for RAM writing via the system interface and the frequency of the internal clock into consideration. RAM writing should be performed with higher speed than the result obtained from the calculation shown below. The internal memory writing address counter is reset by VSYNC. So, ensure

interval time between VSYNC falling and GRAM data writing. The minimum interval time is 2 raster rows, and hence the data writing should start only after that duration.

Internal clock frequency (fosc) [Hz] = Frame freq. × (Display raster-row (NL) + Front porch (FP) + Back porch (BP)) × 16-Clock × Fluctuation

Minimum speed for RAM writing [Hz] > 240 × Display raster-row (NL) / {((Back porch (BP) + Display raster-row (NL) – Margin) × 16 Clock) / fosc}

NOTE: When RAM writing does not start immediately after the falling edge of VSYNC, the time between the falling edge of VSYNC and the RAM writing start timing must also be considered.

An example is shown below.

Example

Display size	240RGB × 320 raster-rows
Display line number	320 raster-row (NL=100111)
Back/Front porch	14 lines/2 lines (BP=1110/FP=0010)
Frame Frequency	60Hz

Internal clock frequency (fosc) [Hz]= 60 Hz × (320 + 2 + 14) lines× 16 clock × 1.1 / 0.9 = 394 kHz

NOTES: 1. Calculating the internal clock frequency requires considering the fluctuation. In the above case a 10% fluctuation within the VSYNC period is assumed.

2. The fluctuation includes LSI production variation and air temperature fluctuation. Other fluctuations, including those for the external resistors and the supplied power, are not included in this example. Please keep in mind that a margin for these factors is also needed.

Minimum speed for RAM writing [Hz] > 240 × 320 / {((14 + 320 – 2) lines × 16 clock) / 394kHz} = 5.7 MHz

NOTES: 3. In this case RAM writing starts immediately after the falling edge of VSYNC.

4. The margin for display raster-row should be two raster-rows or more at the completion of RAM writing for one frame.

Therefore, when RAM writing starts immediately after the falling edge of VSYNC is performed at 5.7 MHz or more, the data for display can be rewritten before display operation has started. This means that flicker-free display operation is achieved.

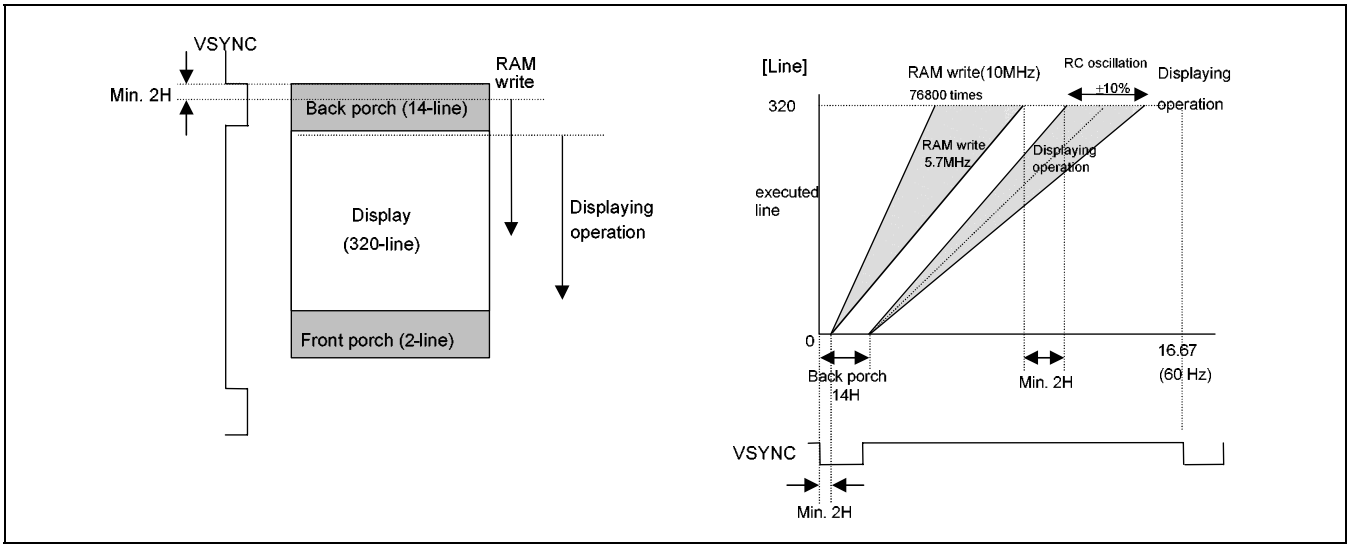


Figure 53. Operation for VSYNC Interface

Preliminary

Usage on VSYNC interface

1. The Example above is a calculated value. Please keep in mind that a margin for these factors is also needed. Because production variation of the internal oscillator requires consideration.
2. The Example above is a calculated value of rewriting the whole screen. A limitation of the motion picture area generates a margin for the RAM write speed.

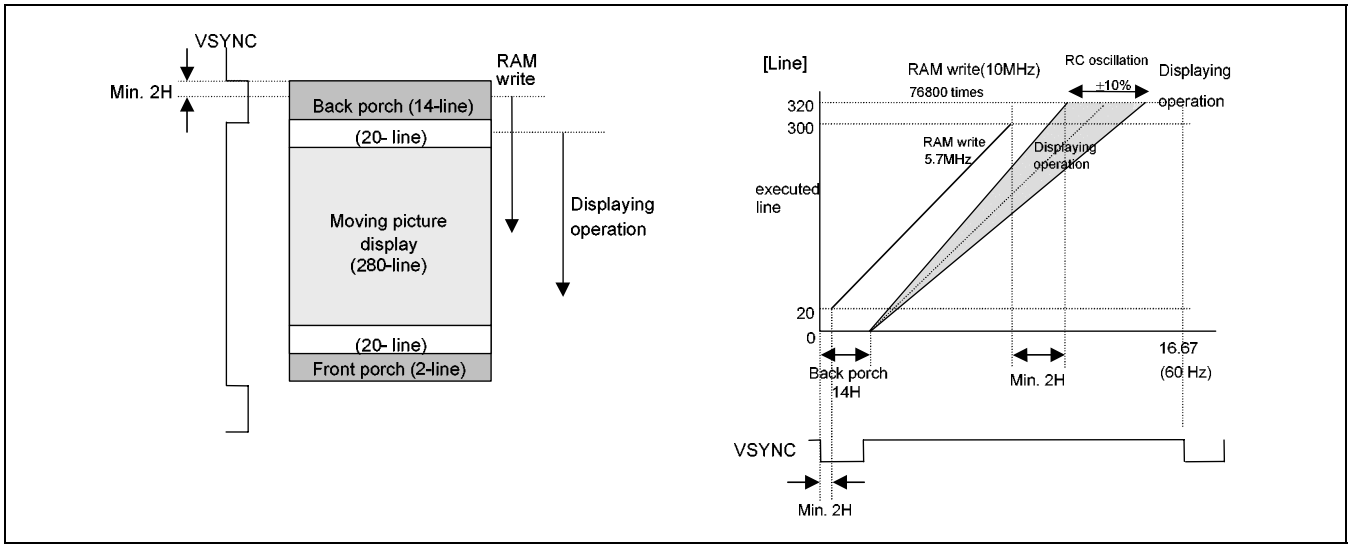


Figure 54. Limitation of Motion picture Area

3. During the period between the completion of displaying one frame data and the next VSYNC signal, the display will remain for a front porch period.
4. Transition between the internal operating clock mode (DM1-0=”00”) and VSYNC interface mode will be valid after the completion of the screen, which is displayed when the instruction is set.

Preliminary

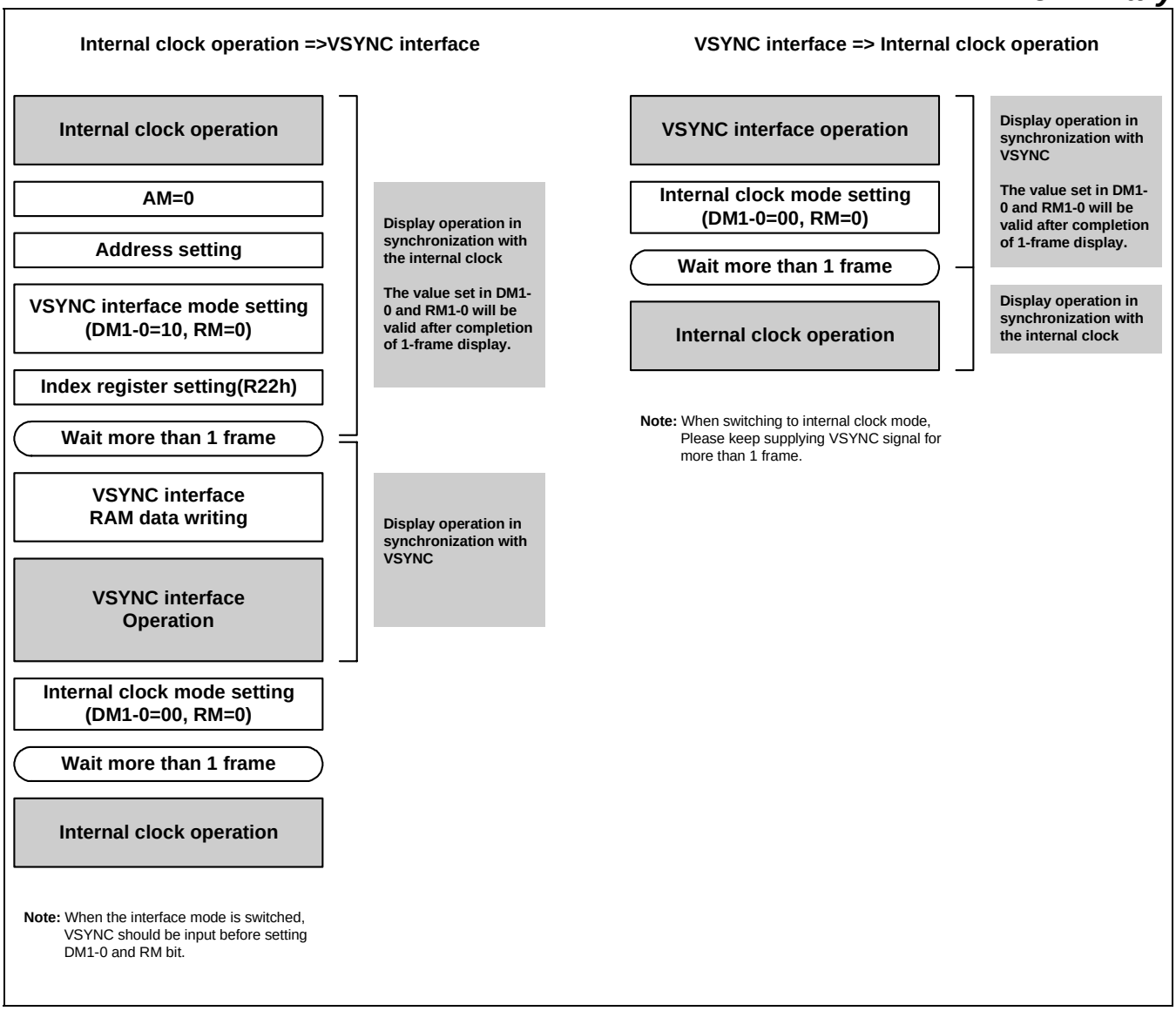


Figure 55. Transition between the Internal Operating Clock Mode and VSYNC Interface Mode

5. Partial display, vertical scroll, and interlaced driving functions are not available on VSYNC interface mode.
6. The flow of above method performs the VSYNC interface mode.

Preliminary

EXTERNAL DISPLAY INTERFACE

The following interfaces are available as external display interface. It is determined by the bit setting of DM1-0.

Table 32. DM Bits

DM1	DM0	Display Operation Mode
0	0	Internal clock operation / MDDI
0	1	RGB interface
1	0	VSYNC interface / MDDI
1	1	-

RGB INTERFACE

The RGB interface is performed in synchronization with VSYNC, HSYNC, and DOTCLK. Combining the function of the high-speed write mode and the window address enables transfer only the screen to be updated and reduce the power consumption.

Table 33. RIM Bits

RIM1	RIM0	RGB Interface	PD Pin
0	0	18-bit RGB interface	PD17 to 0
0	1	16-bit RGB interface	PD17 to13, 11 to 1
1	0	6-bit RGB interface	PD17 to12
1	1	Setting disabled	

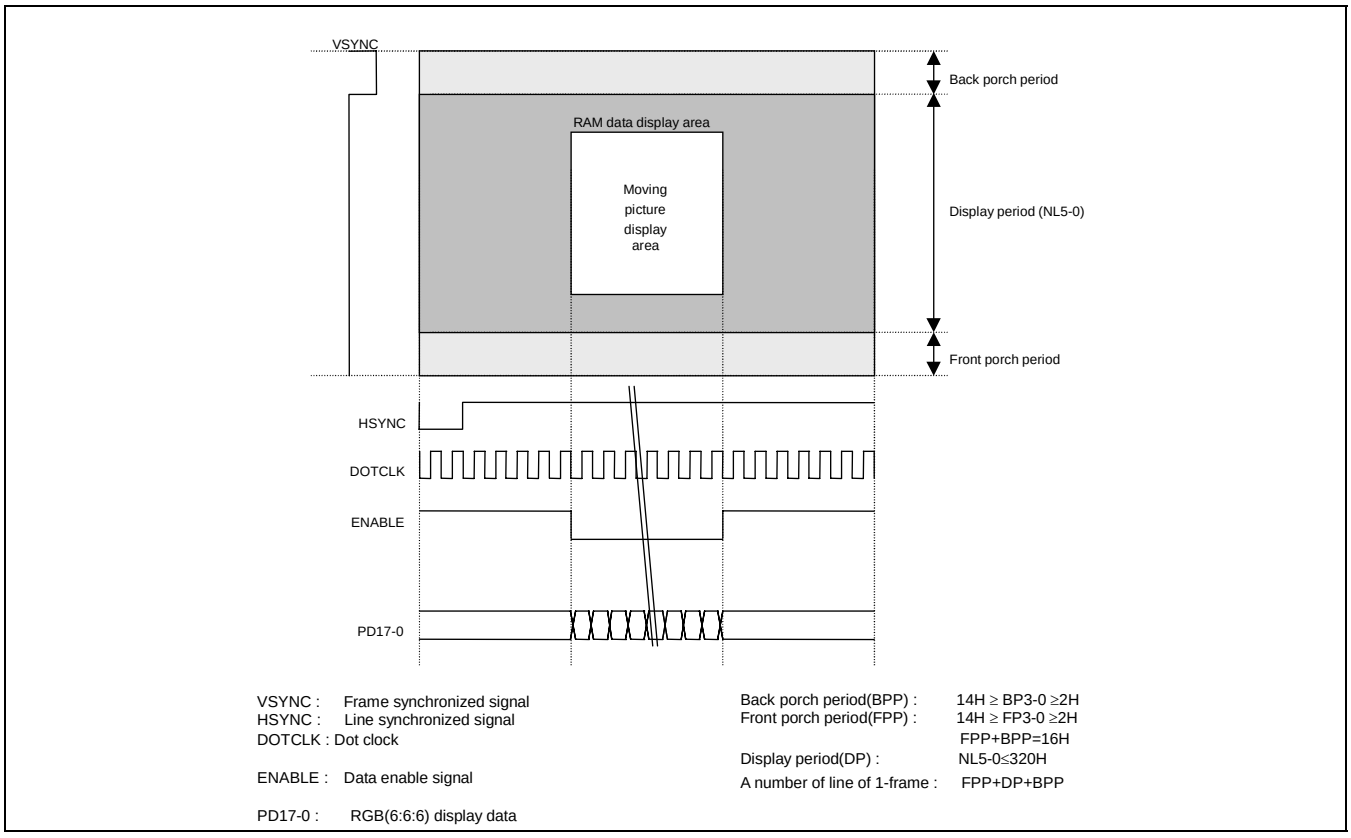


Figure 56. RGB Interface

Preliminary

ENABLE SIGNALS

The relationship between EPL and ENABLE signal is shown below. When ENABLE is not active, the address is not update. When ENABLE is active, the address is updated.

Table 34. Relationship between EPL and ENABLE

EPL	ENABLE	RAM WRITE	RAM ADDRESS
0	0	Valid	Updated
0	1	Invalid	Hold
1	0	Invalid	Hold
1	1	Valid	Update

Preliminary

RGB INTERFACE TIMING

Time chart for RGB interface is shown below.

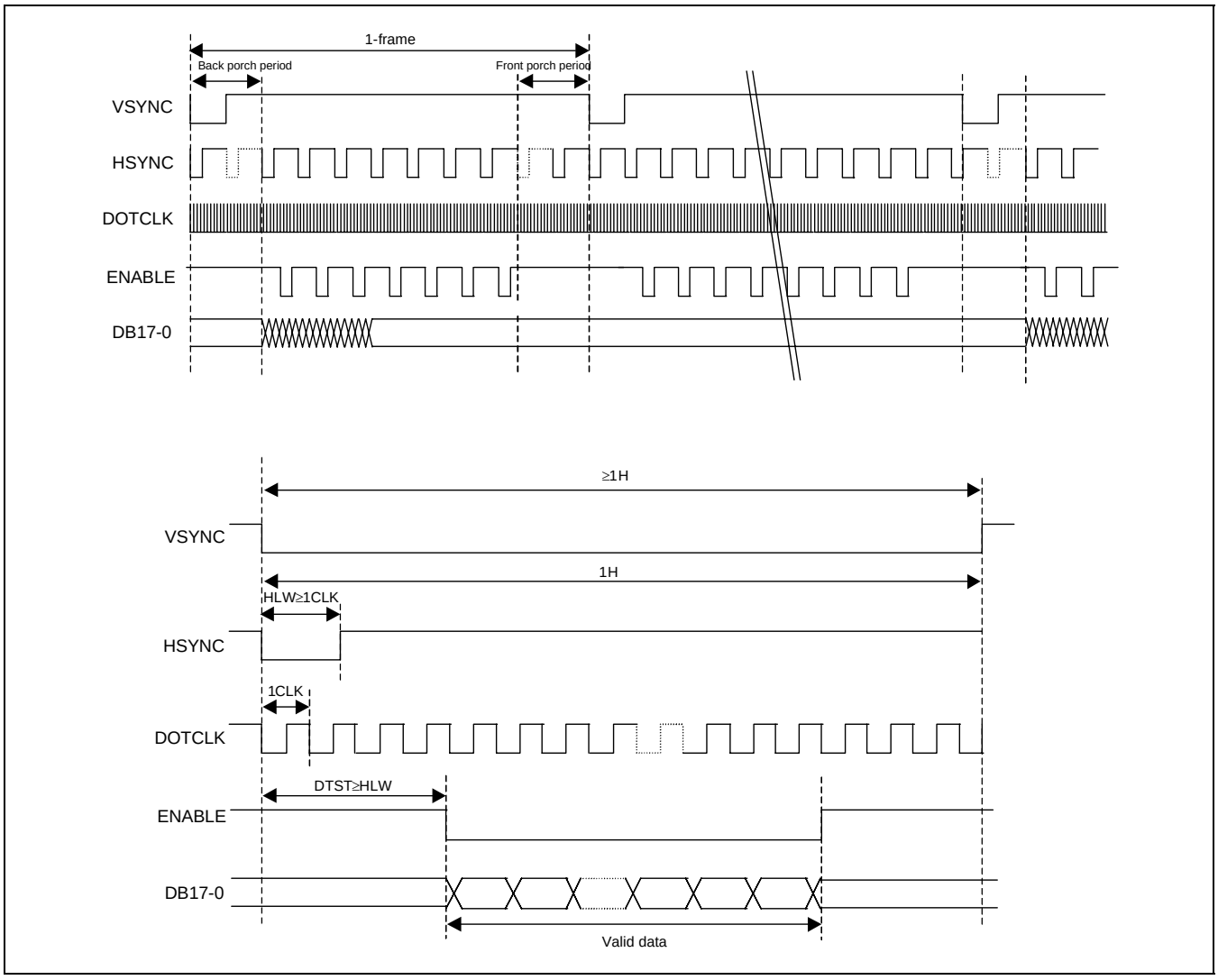


Figure 57. 16-/18-bit RGB Interface Timing (In case of EPL = 0, DPL = 0, VSPL = 0, HSPL = 0)

VLW: The period in which VSYNC is “Low” level
HLW: The period in which HSYNC is “Low” level
DTST: Set up time of data transfer

Preliminary

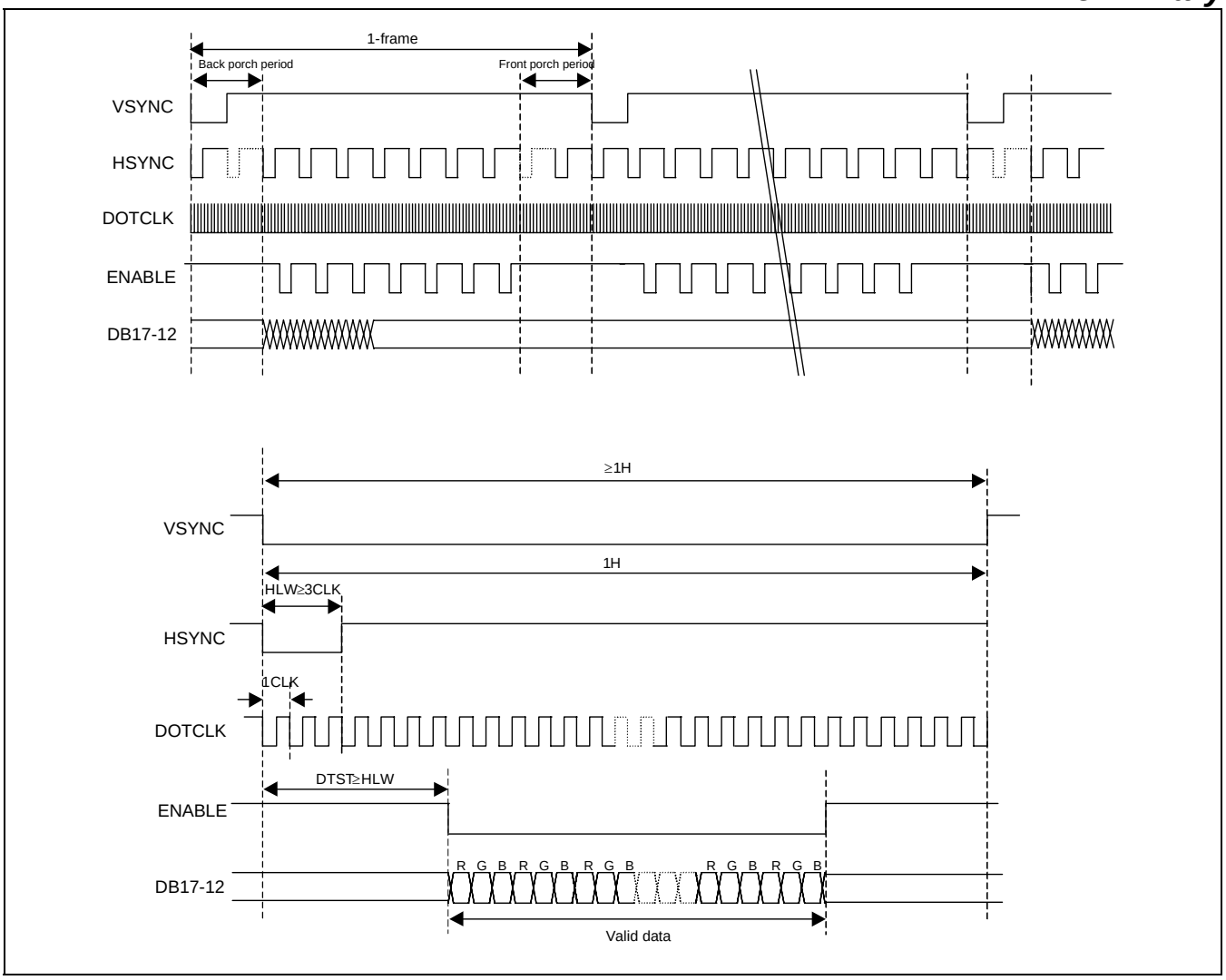


Figure 58. 6-bit RGB Interface Timing (In case of EPL = 0, DPL = 0, VSPL = 0, HSPL = 0)

VLW: The period in which VSYNC is “Low” level
HLW: The period in which HSYNC is “Low” level
DTST: Set up time of data transfer

NOTES: 1. Three clocks are regarded as one clock for transfer when data is transferred in 6-bit interface.
2. VSYNC, HSYNC, ENABLE, DOTCLK and PD17-2 should be transferred in units of three clocks.

Preliminary

MOTION PICTURE DISPLAY

The S6D0139 incorporates RGB interface to display motion pictures and RAM to store data for display.
For displaying motion pictures, the S6D0139 has the following features.
- Motion picture area can only be transferred by the window address function.
- Motion picture area to be rewritten can only be transferred.
- Reducing the amount of data transferred reduces the power consumption to the whole system.
- Still picture area, such as an icon, can be updated while displaying motion pictures combining with the system interface.

RAM ACCESS VIA RGB INTERFACE AND SYSTEM INTERFACE

RAM can be accessed via the system interface when RGB interface is in use. When data is written to RAM during RGB interface mode, the ENABLE bit should be low to stop data writing via RGB interface, because RAM writing is always performed in synchronization with the DOTCLK input when ENABLE is high. After this RAM access via the system interface, a waiting time is needed for a write/read bus cycle before the next RAM access starts via RGB interface. When a RAM write conflict occurs, data writing is not guaranteed.
Example of display motion picture via RGB-I/F and updating still picture via the system interface are shown below.

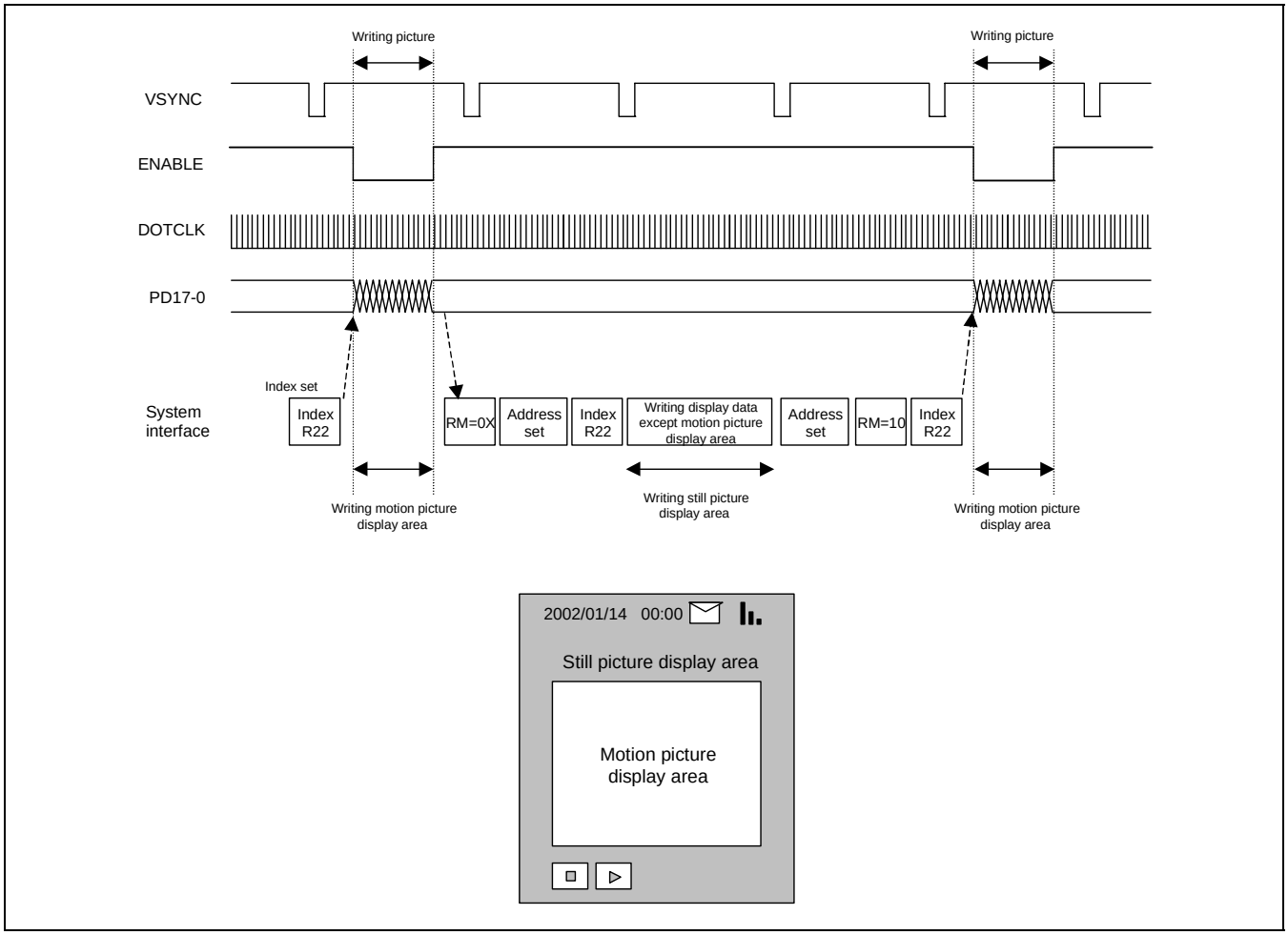


Figure 59. Example of Updating Still Picture Area during Displaying Motion Picture (In case of EPL = 0, VSPL = 0)

Preliminary

6-BIT RGB INTERFACE

6-bit RGB interface can be used by setting RIM1-0 pins to “00”. Display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Data for display is transferred to the internal RAM via 6-bit RGB data bus (PD17 to 12), the data valid signal (VLD), and the data enable signal (ENABLE). Unused pins must be fixed to the VDD3 or GND level.

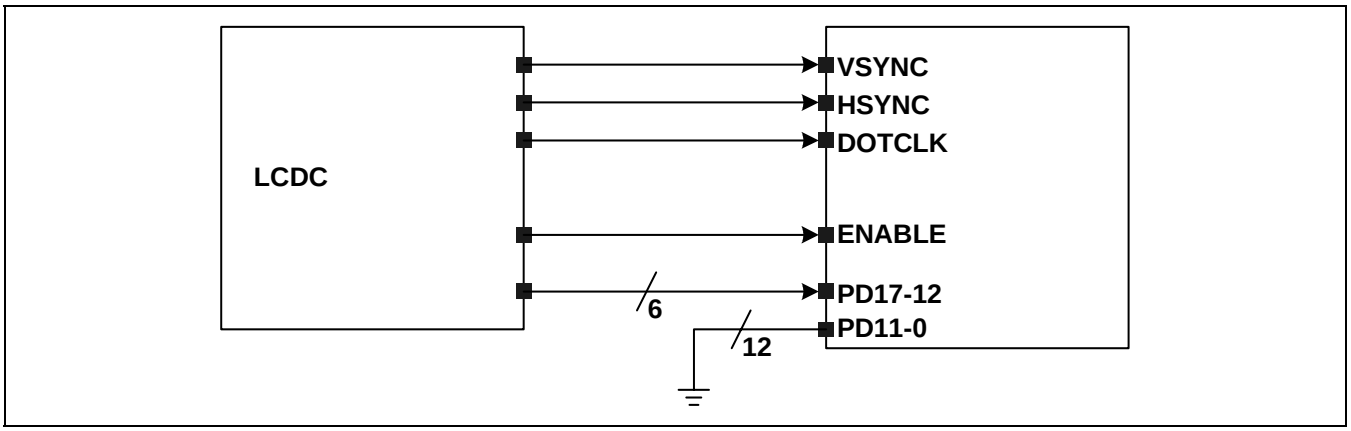


Figure 60. 6-bit RGB Interface

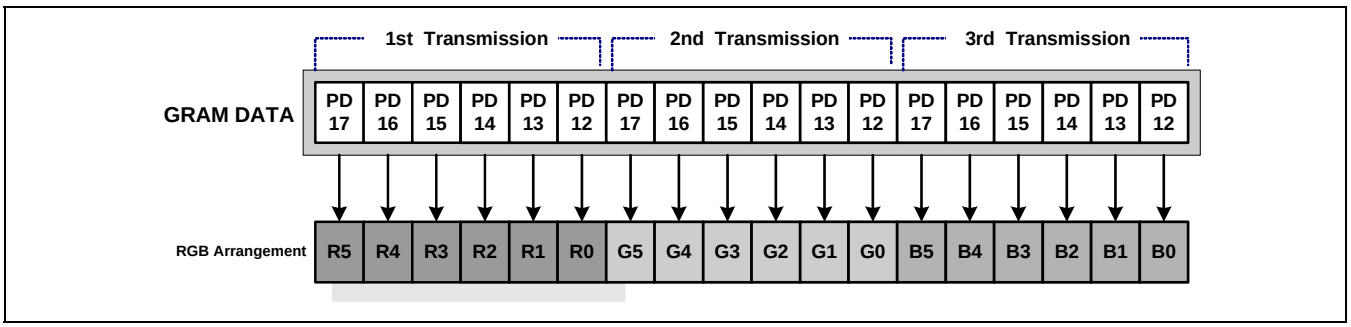


Figure 61. GRAM Write Data format for 6-bit RGB Interface Mode

NOTE: Transfer synchronization function for an 6-bit bus interface. The S6D0139 has the transfer counter to count 1st, 2nd and 3rd data transfer in the 6-bit bus interface. The transfer counter is reset on the falling edge of VSYNC and enters the 1st data transmission state. Transfer mismatch can be corrected, and after that the transfer restarts correctly. In this method, when data such as displaying motion pictures is consecutively transferred, the effect of transfer mismatch is reduced and normal operation is recovered.

NOTE: The internal display is operated in units of three DOTCLK. When the DOTCLK is not input in units of pixels, clock mismatch occurs and the frame, which is operated, and the next frame is not displayed correctly.

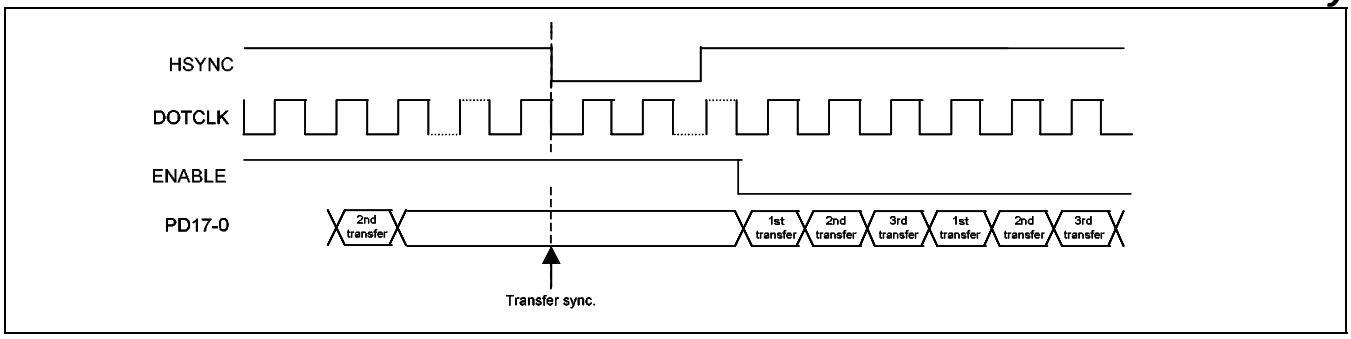


Figure 62. Transfer Synchronization Function in 6-bit RGB Interface Mode

16-BIT RGB INTERFACE

The 16-bit RGB interface can be used by setting RIM1-0 pins to 01. Display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Data for display is transferred to the internal RAM via 6-bit RGB data bus (PD17-13 and 11-1). Instruction should be set via the system interface.

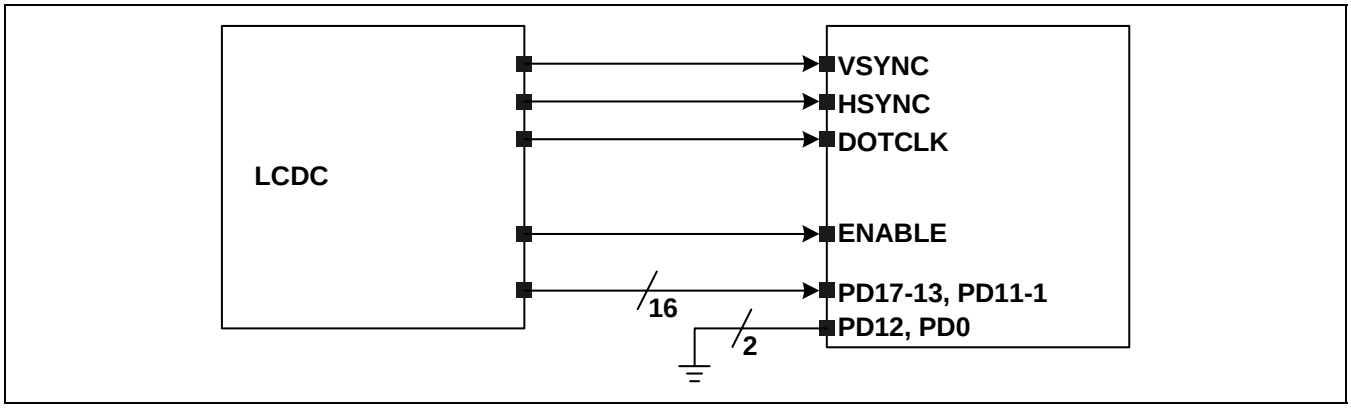


Figure 63. 16-bit RGB Interface to System

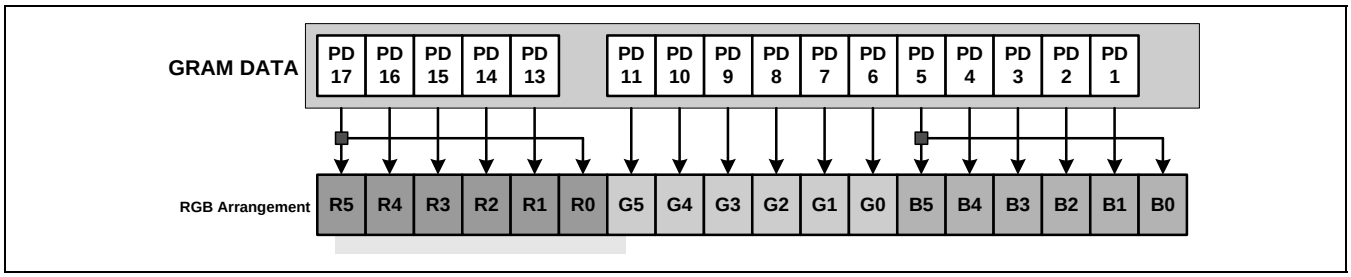


Figure 64. GRAM Write Data in the 16-bit RGB Interface Mode

Preliminary

18-BIT RGB INTERFACE

The 18-bit RGB interface can be used by setting MIF1-0 pins to 01. Display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Data for display is transferred to the internal RAM via 6-bit RGB data bus (PD17-0).

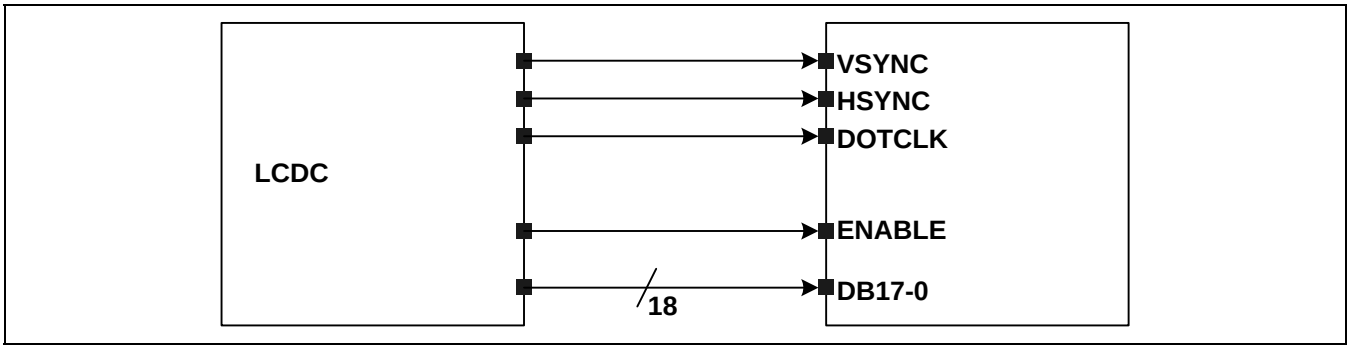


Figure 65. 18-bit RGB Interface to System

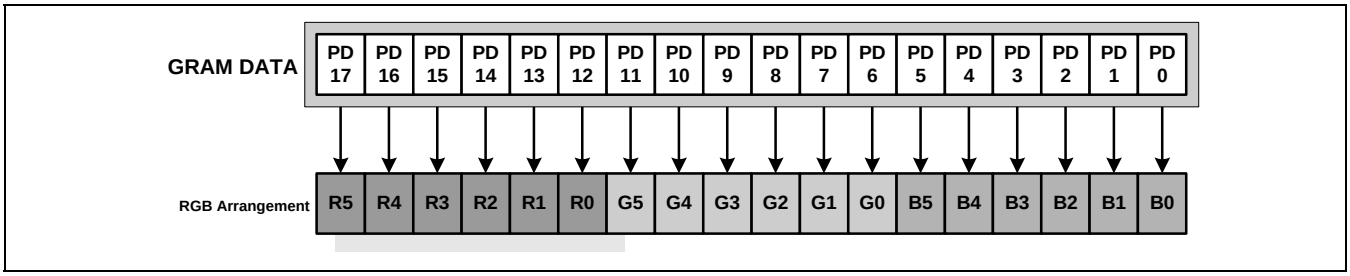


Figure 66. GRAM Write Data format for 18-bit RGB Interface Mode

Preliminary

USAGE ON EXTERNAL DISPLAY INTERFACE

1. When external display interface is in use, the following functions are not available.

Table 35. External Display Interface and Internal Display Operation

Function	External Display Interface	Internal Display Operation
Partial Display	Cannot be used	Can be used
Scroll Function	Cannot be used	Can be used
Interlaced Driving	Cannot be used	Can be used

2. VSYNC, HSYNC, and DOTCLK signals should be supplied during display operation via RGB interface.

3. Please make sure that when setting bits of NO1-0, SDT1-0, and ECS2-0 in RGB interface, the clock on which operations are based changes from the internal operating clock to DOTCLK.

4. RGB data are transferred for three clock cycles in 6-bit RGB interface. Data transferred, therefore, should be transferred in units of RGB.

5. Interface signals, VSYNC, HSYNC, DOTCLK, ENABLE and PD17-0 should be set in units of RGB (pixels) to match RGB transfer.

6. Transitions between internal operation mode and external display interface should follow the mode transition sequence shown below.

7. During the period between the completion of displaying one frame data and the next VSYNC signal, the display will remain for a front porch period.

8. An address set is done on the falling edge of VSYNC every frame in RGB interface.

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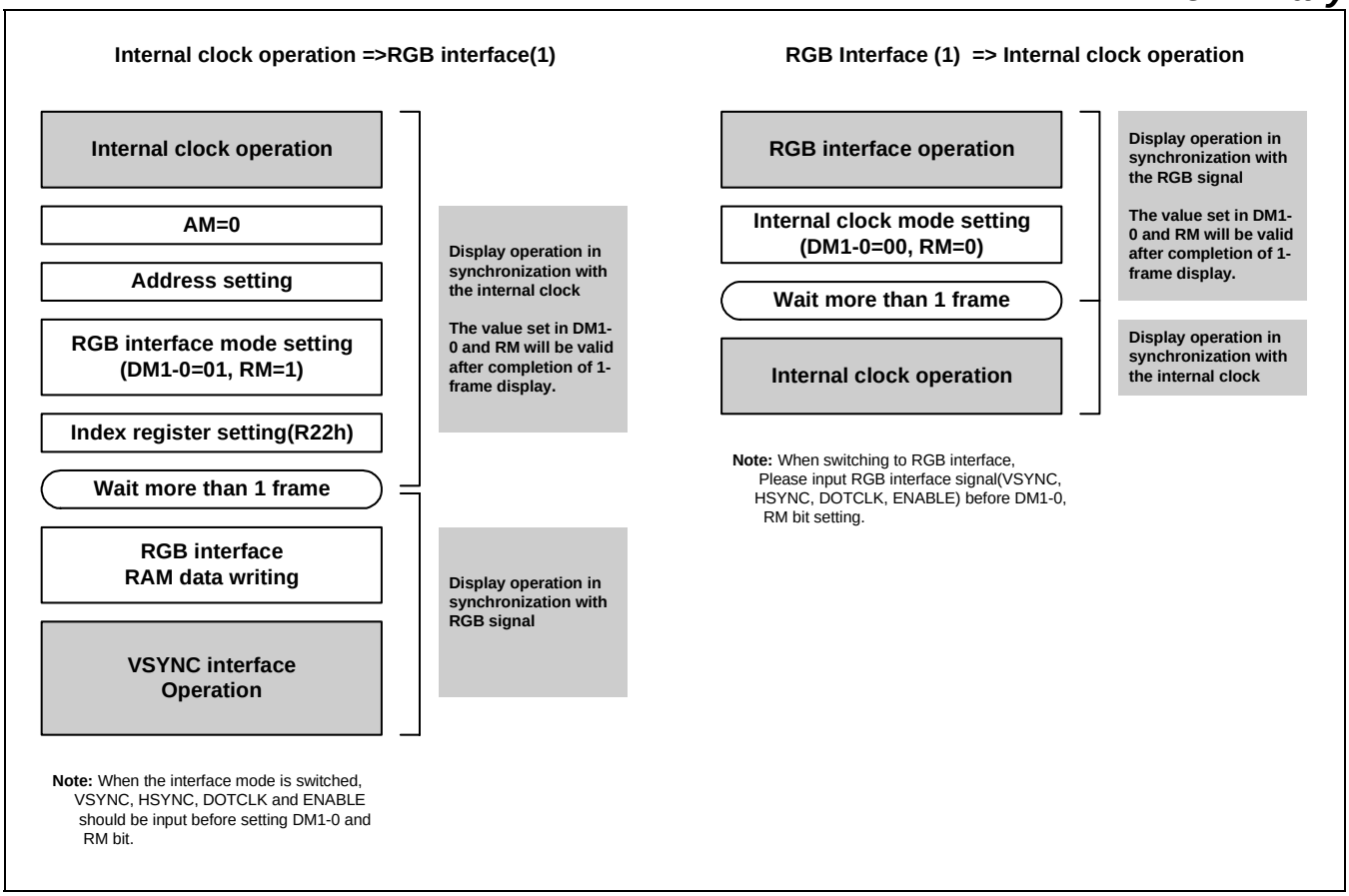

Figure 67. Transition between the Internal Operating Clock Mode and RGB Interface Mode

Preliminary

MDDI (MOBILE DISPLAY DIGITAL INTERFACE)

INTRODUCTION OF MDDI

The S6D0139 supports MDDI. The MDDI is a differential & serial interface with high speed. Both command and image data transfer can be achieved with MDDI.
MDDI host & client are linked with Data and STB line. Through Data line, command or image data is transferred from MDDI host to MDDI client, and vice versa. Data is transferred by packet unit.
Through STB line, strobe signal is transferred. When the link is in "FORWARD direction", data is transferred from host to client; in "REVERSE direction", client transfer reverse data to MDDI host.

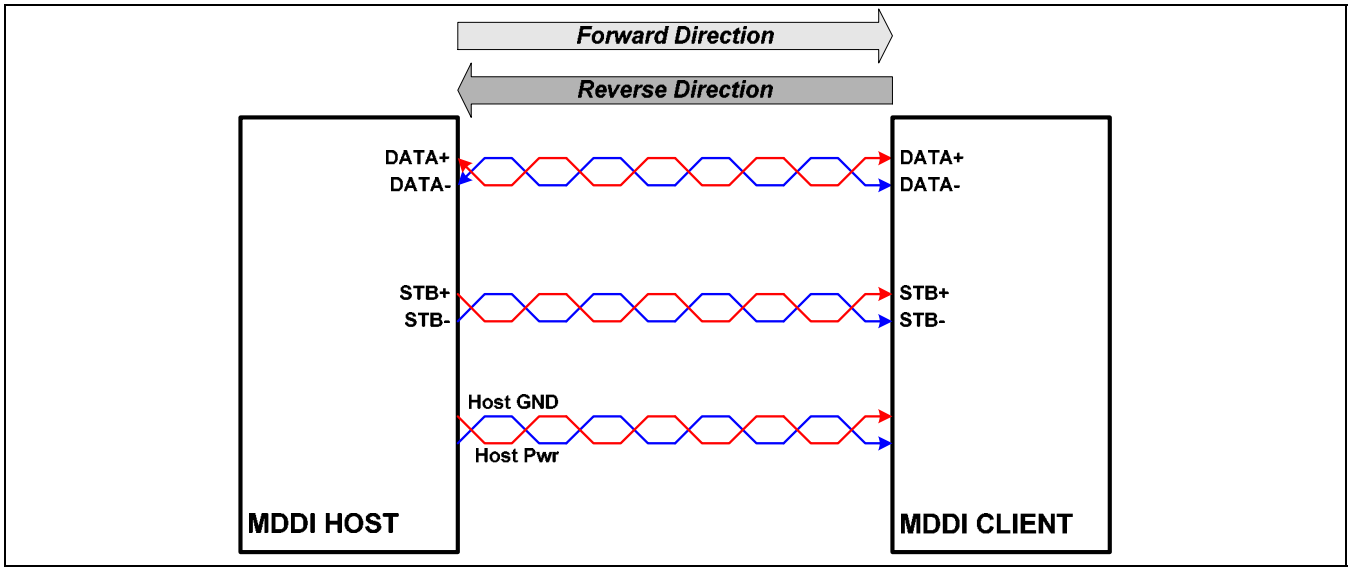

Figure 68. Physical connection of MDDI host and client

DATA-STB ENCODING

Data is encoded using a DATA-STB method. DATA is carried over a bi-directional differential cable, while STB is carried over a unidirectional differential cable driven only by the host. Figure below illustrates how the data sequence "1110001011" is transmitted using DATA-STB encoding.

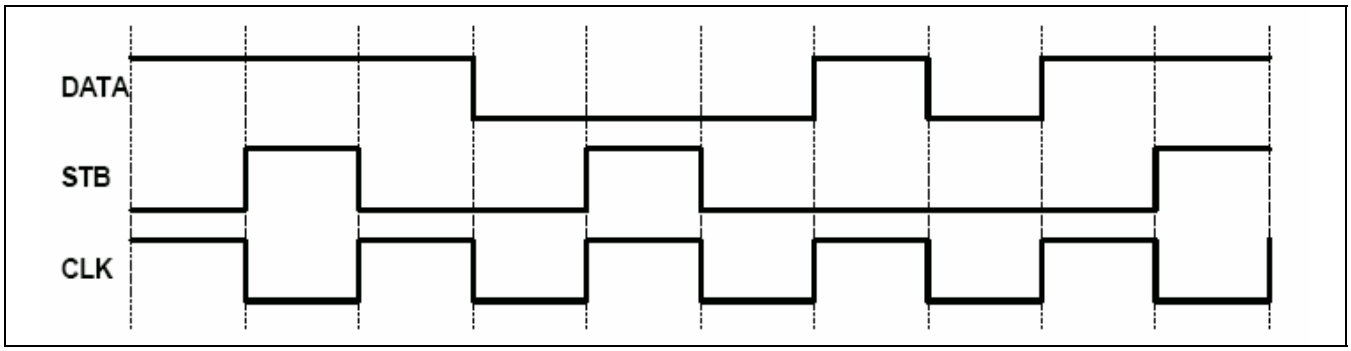

Figure 69. Data-STB encoding

The Following figure shows a sample circuit to generate DATA and STB from input data, and then recover the input data from DATA and STB.

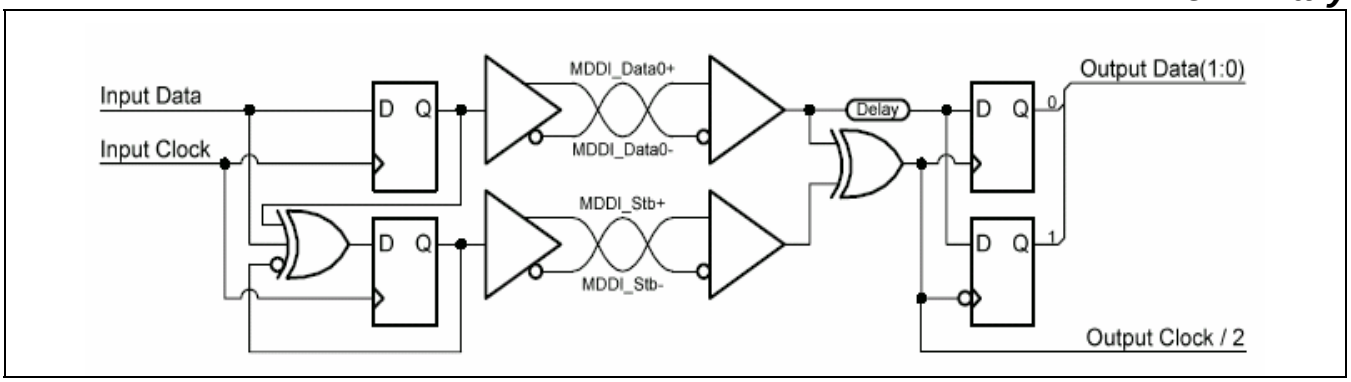

Figure 70. Data / STB Generation & Recovery circuit

MDDI DATA / STB

The Data (MDP/MDN) and STB(MSP/MSN) signals are always operated in a differential mode to maximize noise immunity. Each differential pair is parallel-terminated with the characteristic impedance of the cable. All parallel-terminations are in the client device. Figure below illustrates the configuration of the drivers, receivers, and terminations. The driver of each signal pair has a differential current output. While receiving MDDI packets the MDDI_DATA and MDDI_STB pairs use a conventional differential receiver with a differential voltage threshold of zero volts. In the hibernation state the driver outputs are disabled and the parallel termination resistors pull the differential voltage on each signal pair to zero volts. During hibernation a special receiver on the MDDI_DATA pairs has an offset input differential voltage threshold of positive 125 mV, which causes the hibernation line receiver to interpret the un-driven signal pair as logic-zero level.

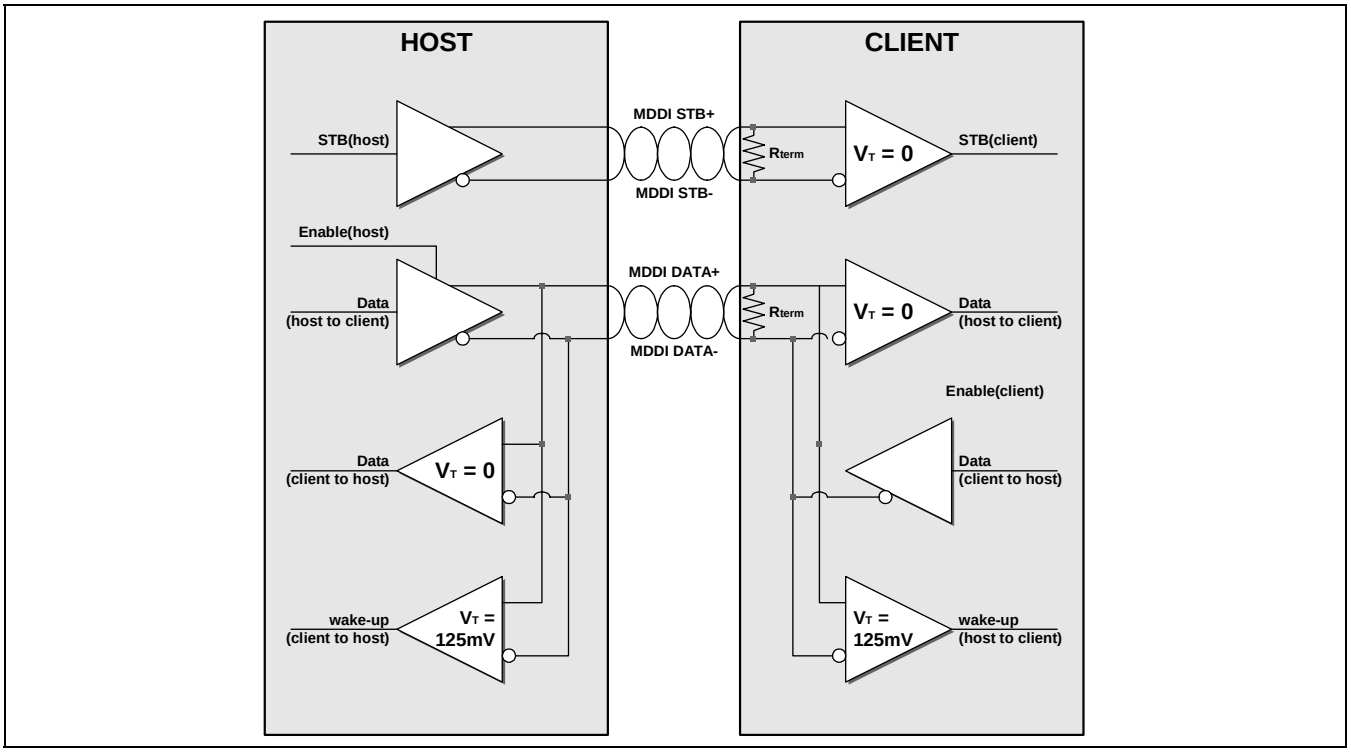

Figure 71. Differential connection between host and client

Preliminary

MDDI PACKET

MDDI transfer data by packet format. MDDI host can make many packets and transfer them.
In S6D0139, several packets format is supported. Most packets are transferred from MDDI host to client (forward direction); but reverse encapsulation packet is transferred from MDDI client to host (reverse direction).
A number of packets, started by sub-frame header packet, construct 1 sub frame.

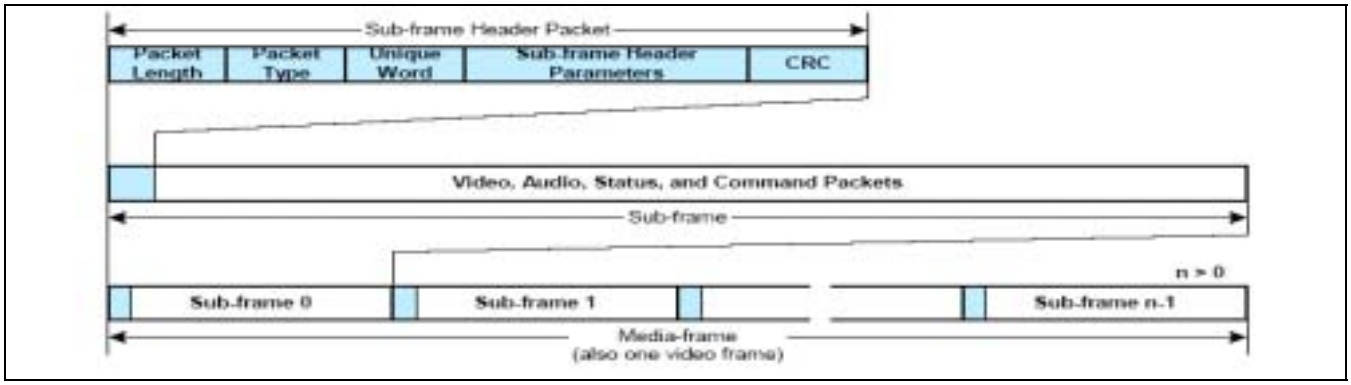

Figure 72. MDDI packet structure

Refer to MDDI packet structure, sub-frame header packet is placed in front of a sub-frame, and some sub-frame construct media-frame together.
The following table describes 9 types of packet which is supported in S6D0139.

PACKET	FUNCTION	DIRECTION
Sub-frame header packet	Header of each sub frame	Forward
Register access packet	Register setting	Forward
Video stream packet	Video data transfer	Forward
Filler packet	Fill empty packet space	Forward
Reverse link encapsulation packet	Reverse data packet	Reverse
Round-trip delay measurement packet	Host->client->host delay check	Forward/Reverse
Client capability packet	Capability of client check	Reverse
Clinet request and status packet	Information about client status	Reverse
Link shutdown packet	End of frame	Forward

Sub-frame header packet

packet length	packet type = 3bffh	unique word = 005ah	reserved1	sub-frame length	protocol version	sub-frame conut	media frame count	CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	2 bytes	4 bytes	2 bytes

packet length : packet length not including packet length block
packet type : packet type (sub-frame header packet is 3bffh)
unique word : Identify "This packet is sub-frame header packet"
reserved1 : not used (set zero)
sub-frame length : specifies number of bytes per sub-frame
protocol version : set all zero
sub-frame count : specifies number of sub-frame header packet
mddi frame count : specifies number of media frames
CRC : error check

Figure 73. Sub-frame header packet structure

Register access packet

packet length	packet type = 146	bClient ID	Read/Write Info	Register Address	Paramter CRC	Register Data List	Register Data CRC
2 bytes	2 bytes	2 bytes	2 bytes	4 bytes	2 bytes	4 bytes	2 bytes

packet length : packet length not including packet length block
packet type : packet type(Register Access packet is 146(decimal))
bClient ID : set to all zero
Read/Write Info : to write register value, bits[15:14] = "00"
to read register value, bits[15:14] = "11"
bits[13:0] is all zero
Register Address : Register address is set written here.
Parameter CRC : To error check from packet length to register address
Register Data List : Paramter data is written here.
CRC : To error check register data list.

Figure 74. Register access packet structure

Video Stream packet

packet length	packet type=16	bClientID	video data format descriptor	pixel data attributes	X left edge	Y top edge	X right edge	Y bottom edge	X start	Y start
2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes	2 bytes

pixel count	parameter CRC	pixel data	pixel data CRC
2 bytes	2 bytes	packet length – 26 bytes	2 bytes

packet length : packet length not including packatet length block
packet type : packet type(video stream packet is 16)
bClientID : reserved, set all 0
video data format descriptor : bits[15:13] = 010 : raw RGB format(fixed value)
bits[12] = 1 : Only packed type is available(fixed value)
bits[11:0] = 0110_0110_0110 : 18 bit pixel
bits[11:0] = 0101_0110_0101 : 16 bit pixel
pixel data attributes : bits[1:0] = 11 : displayed both eyes(fixed value)
bits[5] = 1 : X left edge .. Y start edge is not defined.(fixed value)
other bits are all zero.
X left edge : Not used in S6D0139, set all zero.
Y top edge : Not used in S6D0139, set all zero.
X right edge : Not used in S6D0139, set all zero.
Y bottom edge : Not used in S6D0139, set all zero.
X start : Not used in S6d0139, set all zero.
Y start : Not used in S6d0139, set all zero.
Pixel count : Write number of pixel.
Paramter CRC : To error check from packet length to pixel count.
pixel data : pixel data info. number of pixel data must not be over 65509.
pixel data CRC : To pixel data error check.

Figure 75. Video stream packet structure

Filler packet

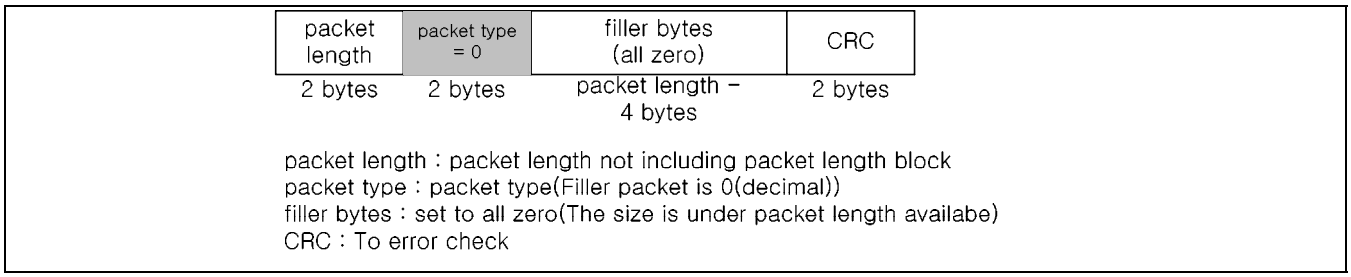

Figure 76. Filler packet structure

Link shutdown packet

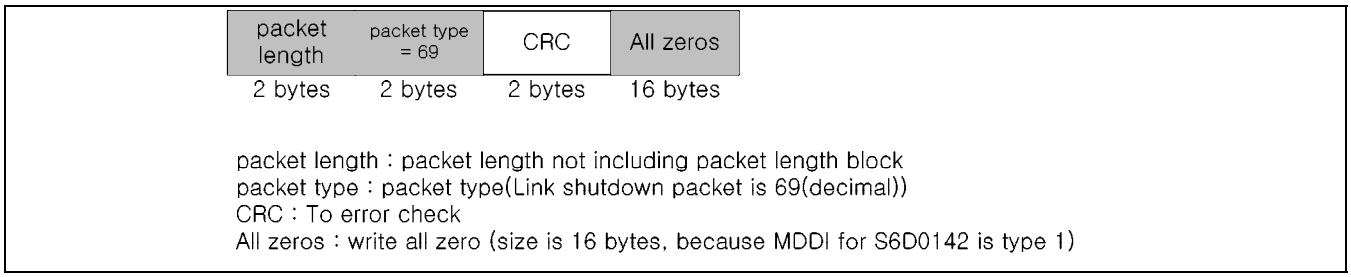

Figure 77. Link shutdown packet structure

: fixed value

For More information about MDDI packet, please refer to VESA MDDI spec.

Preliminary

TEARING-LESS DISPLAY

In S6D0139, the matching between data write timing and written data display timing is important. If timing is mismatched, tearing effect can occur.
To avoid display tearing effect, two possible ways are suggested.
First case is that data write is slower than speed of displaying written data. In this case, data write speed is not critical, but current consumption in interface will be increased because data transfer time is long. Data write time is selected widely (?) in this case.
Other case is that data write is faster than speed of displaying written data. In this case, data update speed is very high so that transfer time is short. So current consumption in interface can be minimized, but it requires fast data transfer. The most important thing is to avoid data scan conflicts with data update.
The following figures describe some examples to avoid display tearing phenomenon.

1. Display speed is faster than data write.

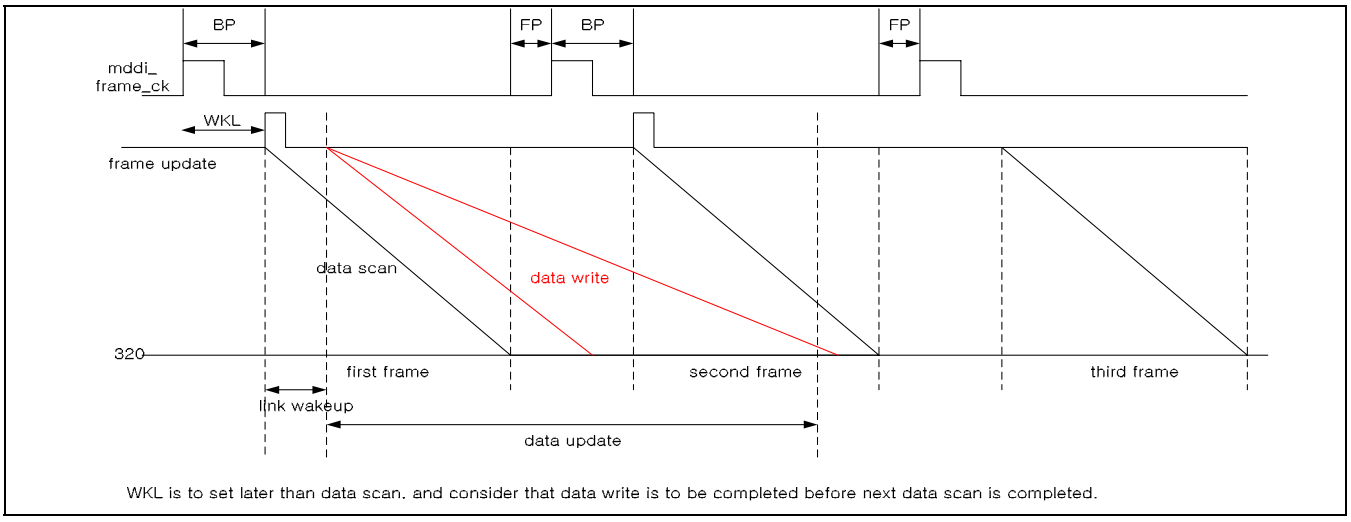

Figure 78. Tearing-less display: display speed is faster than data write

2. Display speed is slower than data write.

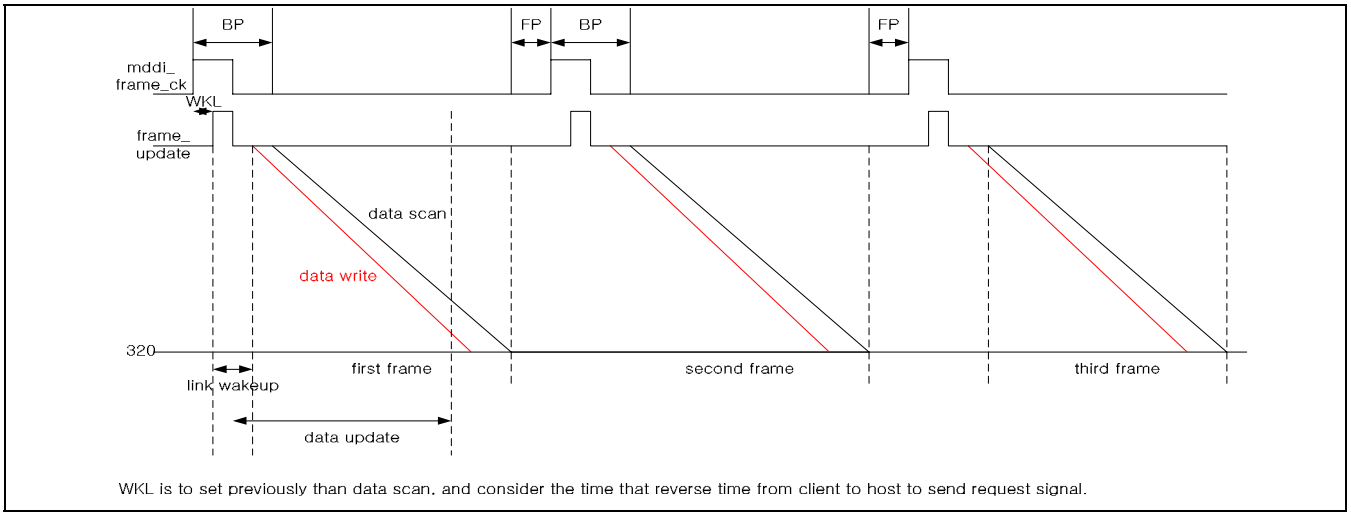

Figure 79. Tearing-less display: data write speed is faster than display

Preliminary

HIBERNATION / WAKE-UP

S6D0139 support hibernation mode for reducing interface power consumption.
The MDDI link can enter the hibernation state quickly and wake up from hibernation quickly. This allows the system to force the MDDI link into hibernation frequently to reduce power consumption.

In hibernation mode, hi-speed transceivers and receivers are disabled and low-speed & low-power receivers are enabled to detect wake-up sequence.

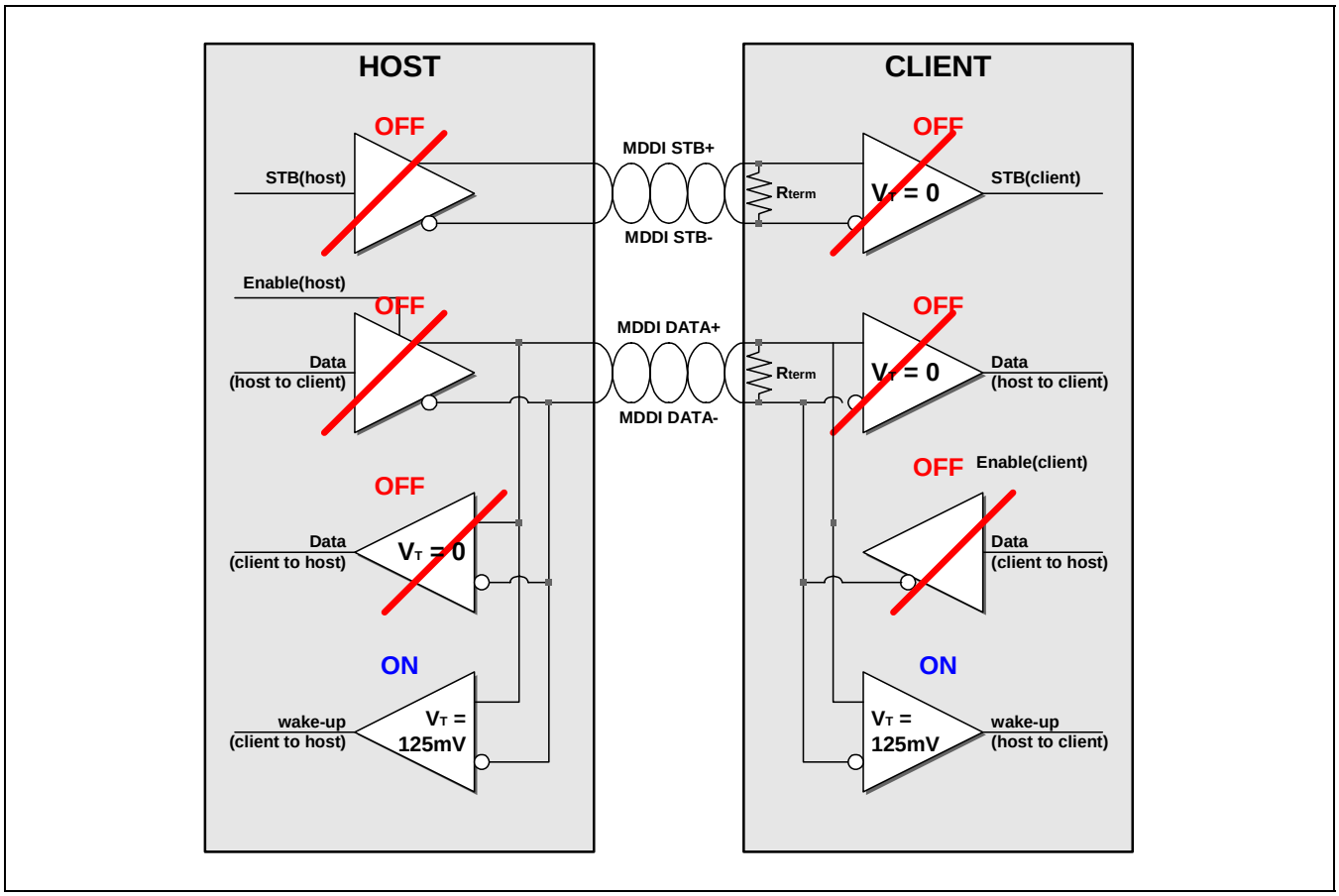

Figure 80. MDDI Transceiver / Receiver state in hibernation

When the link wakes up from hibernation the host and client exchange a sequence of pulses. These pulses can be detect using low-speed, low-power receivers that consume only a fraction of the current of the differential receivers required to receive the signals at the maximum link operating speed.

Both the client and the host can wake up the link, so 2-types of wake-up are supported in S6D0139: Host-initiated link wakeup and Client-initiated link wakeup.

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MDDI LINK WAKE-UP PROCEDURE

Host-initiated Link Wake-up Procedure

The simple case of a host-initiated wake-up is described below without contention from the client trying to wake up at the same time. The following sequence of events is illustrated in the following figure.

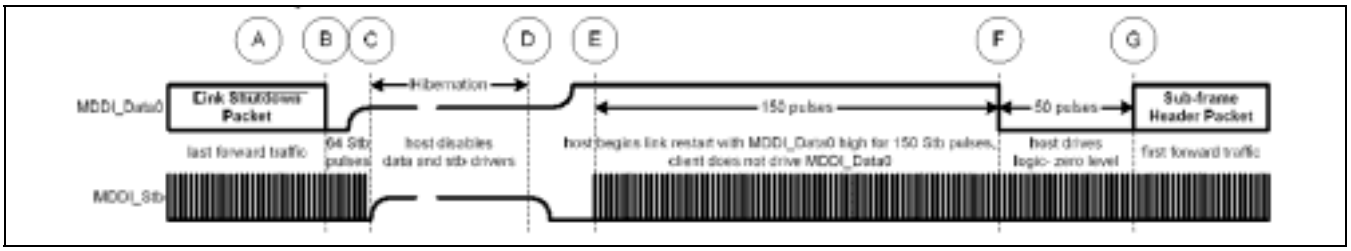

Figure 81. Host-initiated link wakeup sequence

The Detailed descriptions for labeled events are as follows:

A. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.

B. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device.
Also during this interval the host initially sets MDDI_Data0 to a logic-zero level, and then disables the MDDI_Data0 output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC.
It may be desirable for the client to place its high-speed receivers for MDDI_Data0 and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point C.

C. The host enters the low-power hibernation state by disabling the MDDI_Data0 and MDDI_Stb drivers and by placing the host controller into a low-power hibernation state.
It is also allowable for MDDI_Stb to be driven to logic-zero level or to continue toggling during hibernation.
The client is also in the low-power hibernation state.

D. After a while, the host begins the link restart sequence by enabling the MDDI_Data0 and MDDI_Stb driver outputs. The host drives MDDI_Data0 to a logic-one level and MDDI_Stb to logic-zero level for at least the time it takes for the drivers to fully enable their outputs.
The host shall wait at least 200 nsec after MDDI_Data0 reaches a valid logic-one level and MDDI_Stb reaches a valid logic-zero level before driving pulses on MDDI_Stb. This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_Stb. The client first detects the wake-up pulse using a low-power differential receiver having a +125mV input offset voltage.

E. The host drivers are fully enabled and MDDI_Data0 is being driven to a logic-one level.
The host begins to toggle MDDI_Stb in a manner consistent with having a logic-zero level on MDDI_Data0 for a duration of 150 MDDI_Stb cycles.

F. The host drives MDDI_Data0 to logic-zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub-frame Header Packet after MDDI_Data0 is at logic-zero level for 40 MDDI_Stb cycles.

G. The host begins to transmit data on the forward link by sending a Sub-frame Header Packet.
Beginning at point G the MDDI host generates MDDI_Stb based on the logic level on MDDI_Data0 so that proper data-strobe encoding commences from point G.

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Client-initiated Link Wake-up Procedure

An example of a typical client-initiated service request event with no contention is illustrated in the following figure.

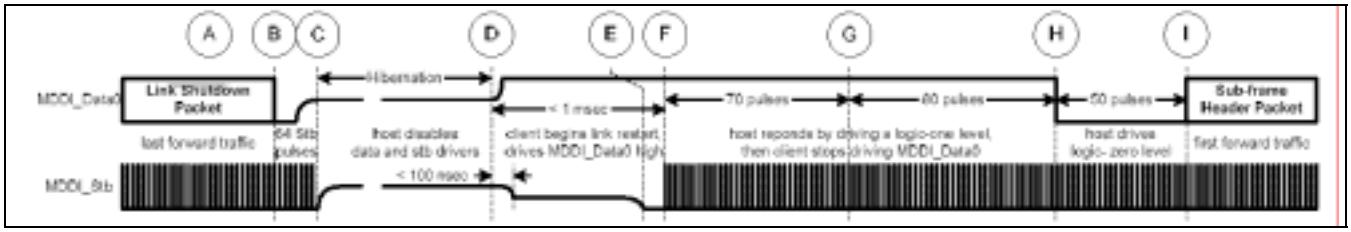

Figure 82. Client-initiated link wake-up sequence

The Detailed descriptions for labeled events are as follows:

A. The host sends a Link Shutdown Packet to inform the client that the link will transition to the low-power hibernation state.

B. Following the CRC of the Link Shutdown Packet the host toggles MDDI_Stb for 64 cycles to allow processing in the client to finish before it stops MDDI_Stb from toggling which stops the recovered clock in the client device.
Also during this interval the host initially sets MDDI_Data0 to a logic-zero level, and then disables the MDDI_Data0 output in the range of 16 to 48 MDDI_Stb cycles (including output disable propagation delays) after the CRC.
It may be desirable for the client to place its high-speed receivers for MDDI_Data0 and MDDI_Stb into a low power state any time after 48 MDDI_Stb cycles after the CRC and before point C.

C. The host enters the low-power hibernation state by disabling its MDDI_Data0 and MDDI_Stb driver outputs.
It is also allowable for MDDI_Stb to be driven to logic-zero level or to continue toggling during hibernation.
The client is also in the low-power hibernation state.

D. After a while, the client begins the link restart sequence by enabling the MDDI_Stb receiver and also enabling an offset in its MDDI_Stb receiver to guarantee the state of the received version of MDDI_Stb is a logic-zero level in the client before the host enables its MDDI_Stb driver.
The client will need to enable the offset in MDDI_Stb immediately before enabling its MDDI_Stb receiver to ensure that the MDDI_Stb receiver in the client is always receiving a valid differential signal and to prevent erroneous received signals from propagating into the client.
After that, the client enables its MDDI_Data0 driver while driving MDDI_Data0 to a logic-one level. It is allowed for MDDI_Data0 and MDDI_Stb to be enabled simultaneously if the time to enable the offset and enable the standard MDDI_Stb differential receiver is less than 200 nsec.

E. Within 1 msec the host recognizes the service request pulse, and the host begins the link restart sequence by enabling the MDDI_Data0 and MDDI_Stb driver outputs.
The host drives MDDI_Data0 to a logic-one level and MDDI_Stb to a logic-zero level for at least the time it takes for the drivers to fully enable their outputs. The host shall wait at least 200 nsec after MDDI_Data0 reaches a valid logic-one level and MDDI_Stb reaches a valid fully-driven logic-zero level before driving pulses on MDDI_Stb.
This gives the client sufficient time to prepare to receive high-speed pulses on MDDI_Stb.

F. The host begins outputting pulses on MDDI_Stb and shall keep MDDI_Data0 at a logic-one level for a total duration of 150 MDDI_Stb pulses through point H. The host generates MDDI_Stb in a manner consistent with sending a logic-zero level on MDDI_Data0. When the client recognizes the first pulse on MDDI_Stb it shall disable the offset in its MDDI_Stb receiver.

G. The client continues to drive MDDI_Data0 to a logic-one level for 70 MDDI_Stb pulses, and the client disables its MDDI_Data0 driver at point G. The host continues to drive MDDI_Data0 to a logic-one level for duration of 80 additional MDDI_Stb pulses, and at point H drives MDDI_Data0 to logic-zero level.

H. The host drives MDDI_Data0 to logic-zero level for 50 MDDI_Stb cycles. The client begins to look for the Sub-frame Header Packet after MDDI_Data0 is at logic-zero level for 40 MDDI_Stb cycles.

I. After asserting MDDI_Data0 to logic-zero level and driving MDDI_Stb for duration of 50 MDDI_Stb pulses the host begins to transmit data on the forward link at point I by sending a Sub-frame Header Packet.
The client begins to look for the Sub-frame Header Packet after MDDI_Data0 is at logic-zero level for 40 MDDI_Stb cycles.

Preliminary

GPIO CONTROL

S6D0139 offers 10(maximum) GPIO that can be used as input or output independently.
Some application or device on the upper clamshell needs several control signals which are supplied by base band modem or application processor directly. If number of application on the upper clamshell increases, also control signals increase, causing the interface more costly.
In S6D0139, GPIO can be the solution for that problem. User may control the 10 GPIOs as input or output by use of simple register setting. So additional connection between base band modem / AP (application processor) and components on upper clamshell are not needed.

The following table shows several set of register for GPIO.

Register	width	Description		Reset value
GPIO (75h)	[9:0]	Write	For GPIO output mode: output GPIO register(75H) value to GPIO PAD	10'h000
		Read	GPIO PAD status	
GPIO_CON (76h)	[9:0]	Write	GPIO PAD input/output mode control : (0 : input / 1 : output)	10'h000
		Read	GPIO_CON (76h) register value	
GPCLR (77h)	[9:0]	Write	For GPIO input mode: clear specified GPIO interrupt (set by GPIO PAD input).	10'h000
		Read	GPIO interrupt state (set by GPIO PAD input).	
GPIO_EN (78h)	[9:0]	Write	For GPIO input mode: enable specified GPIO interrupt	10'h000
		Read	GPIO_EN (78h) register value.	
GPPOL (79h)	[9:0]	Write	For GPIO input mode: GPIO interrupt polarity setting	10'h3FF
		Read	GPPOL (79h) register value.	

In GPIO output mode, the IC output GPIO (75h) register value to the defined PAD.
Set GPIO_CON register as output mode before use GPIO output.

10 different GPIO output can be controlled simultaneously using 1-register access packet (75h register access) so that minimum access time for each GPIO output will be 1-register access time.

GPIO input mode can only be used as client-initiated link wake-up.
For more information, refer to GPIO based link wake-up section.

Preliminary

CLIENT-INITIATED LINK WAKE-UP

S6D0139 supports 2-types of client-initiated link wake-up: VSYNC based Link Wake-up & GPIO based Link Wake-up. As client-initiated wake-up action is executed in hibernation state only, register setting for each wake-up have to be set before link shut-down.

VSYNC Based Link Wake-up

In display-ON state, when the IC finishes displaying all internal GRAM data, data request must be transferred to MDDI host for new video data. As MDDI link is usually in hibernation for reducing interface power consumption, MDDI link wake-up must be done before internal GRAM update. In that case, client initiated link wake-up can be used as data request.

When VSYNC based link wake-up register (50h: VWAKE_EN) is set, client initiated wake-up is executed in synchronization with the vertical-sync signal which generated in S6D0139.
Using VSYNC based link wake-up, tearing-less display can be accomplished if interface speed and wake-up time is well known.

The following figure shows detailed timing for VSYNC based link wake-up.

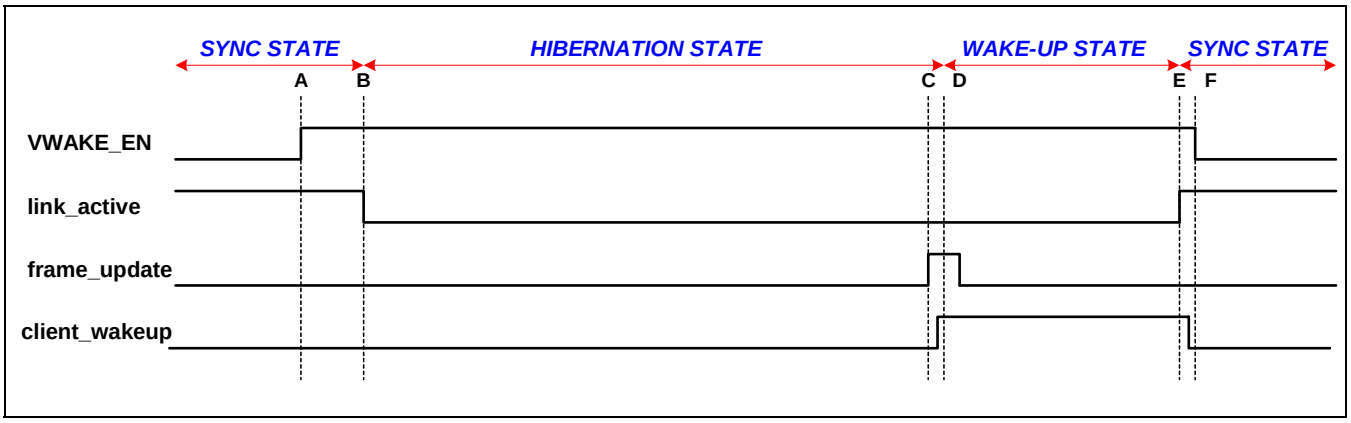

Figure 83. VSYNC based link wake-up procedure

The Detailed descriptions for labeled events are as follows:

A. MDDI host writes to the VSYNC based link wakeup register to enable a wake-up based on internal vertical-sync signal.

B. link_active goes low when the host puts in the link into hibernation after no more data needs to be sent to the S6D0139.

C. frame_update, the internal vertical-sync signal goes high indicating that update pointer has wrapped around and is now reading from the beginning of the frame buffer. Link wake-up point can be set using WKF and WKL (51h) registers. WKF specifies the number of frame before wake-up; WKL specifies the number of lines before wake-up.

D. client_wakeup input to the MDDI client goes high to start the client initiated link wake-up.

E. link_active goes high after the host brings the link out of hibernation.

F. After link wake-up, client_wakeup signal and the VWAKE_EN register are cleared automatically.

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GPIO Based Link Wake-up

In VSYNC-based link wake-up, wake-up enable register setting prior to link shut-down. GPIO based Link wake-up is enabled by interrupt from outside of the IC. For GPIO based link wake-up, GPIO interrupt enable and GPIO PAD mode (to input mode) setting must be set. Once S6D0139 receive interrupt, internal GPIO base link wake-up flag set to high, and the following procedure is similar to that of VSYNC based link wake-up.
The following figure shows detailed timing for GPIO based link wake-up.

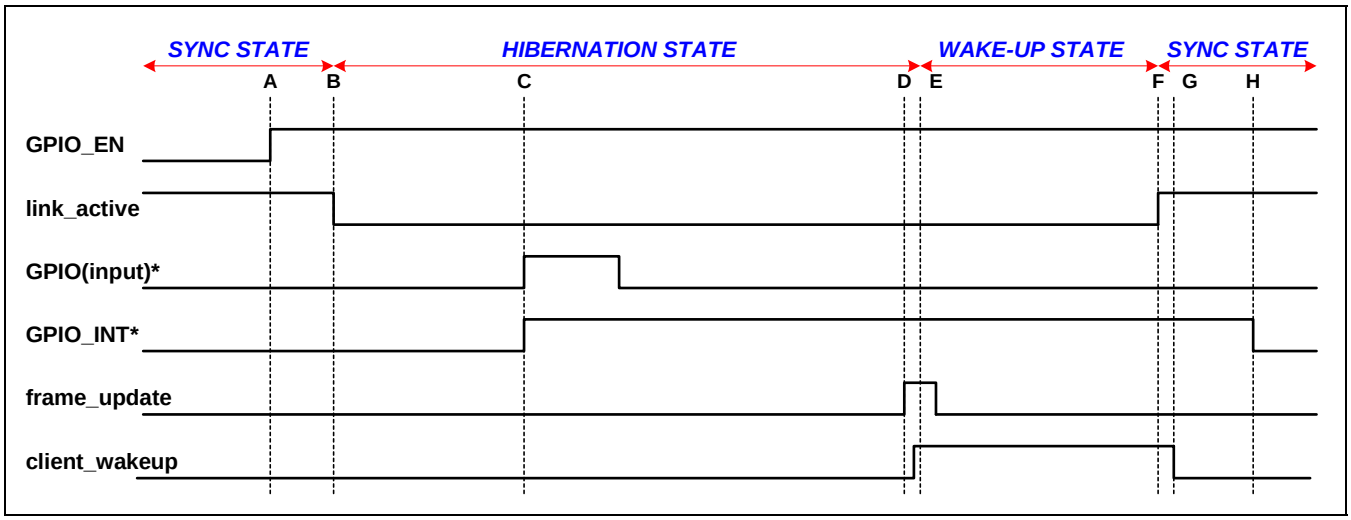

Figure 84. GPIO based link wake-up procedure

The Detailed descriptions for labeled events are as follows:

A. Host sets the GPIO interrupt enable register (78h: GPIO_EN) for a particular GPIO through register access packet.

B. Link goes into hibernation (and link_active goes low) when the host has no more data to send to the IC.

C. GPIO input goes high, and the GPIO interrupt (GPIO_INT) is latched.

D. Frame_update signal goes high indicating that the display has wrapped around. Link wake-up point can be set using WKF and WKL (51h) registers.

E. Client_wakeup input to the MDDI client goes high to start the client initiated link wake-up.

F. Link_active goes high after the host brings the link out of hibernation.

G. After link wake-up, client_wakeup signal is reset to low.

H. MDDI host clears the interrupt by writing to the interrupt clear register with the bit set for that particular interrupt (GPCLR: 77h). Between point G and H the host will have read the GPIO_INT values to see what interrupts are active.

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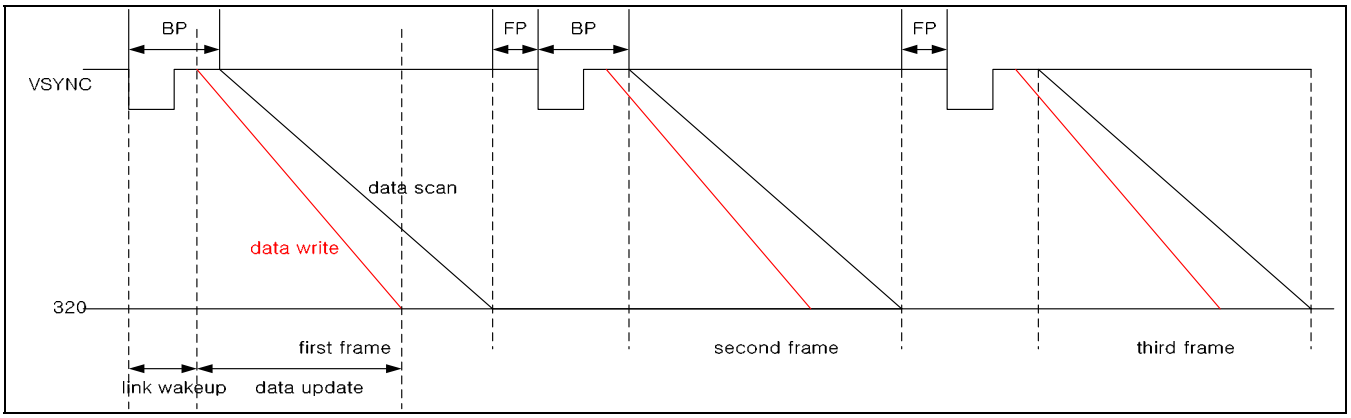
VSYNC MODE IN MDDI (HOST INITIATED WAKE-UP)

VSYNC mode in MDDI can enable host initiated wakeup. Using this mode, special signal to wake up from hibernation state is not needed. Host only sends wakeup signal & data synchronizing with VSYNC signal. The way to operate VSYNC mode is to set DM bit (0Ch) to '10'. Next figures show timing for data writing to GRAM and displaying written data.

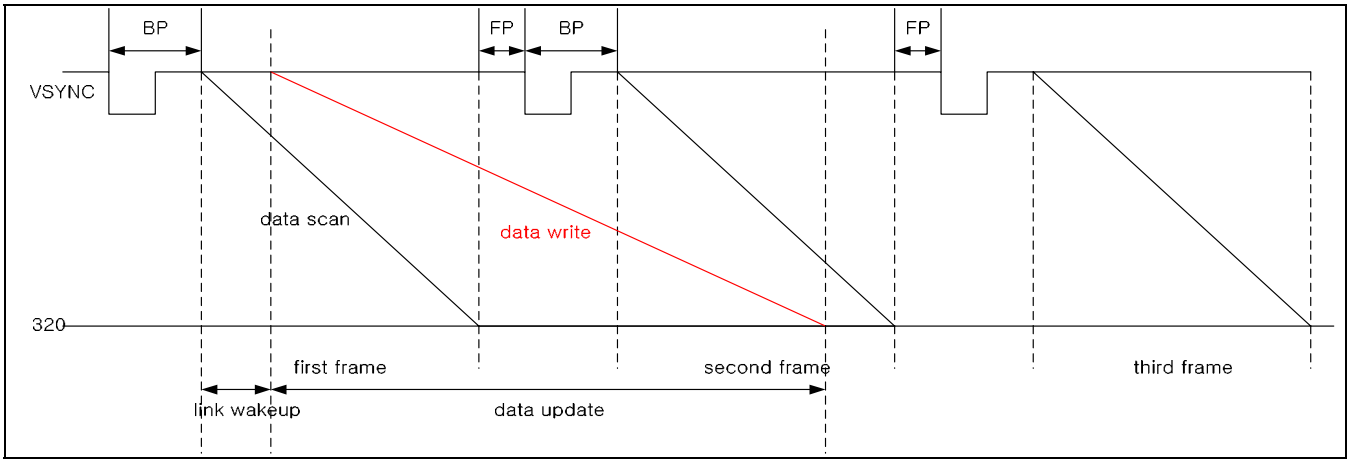
Data write operation is completed during 1 frame time.

In case that data write speed is faster than that of written data display.



Data write operation is completed during over 1 frame time.

In case that data write speed is slower than that of written data display.



SAMSUNG ELECTRONICS

Preliminary

MDDI OPERATING STATE

In MDDI, six operation modes are available. The following table describes six modes.

STATE	OSC	Step-up Circuit	Internal Logic status	MDDI I/O	Wake-up by
SLEEP	ON	Disabled	Display OFF MDDI Link hibernation	Hibernation driver ON	Host – Initiated
WAIT	ON	Disabled	Display OFF MDDI Link in SYNC	standard driver ON	-
Normal	ON	Enabled	Display ON MDDI Link in SYNC	standard driver ON	-
NAP	ON	Disabled	Display OFF MDDI Link in SYNC	standard driver ON	-
IDLE	ON	Enabled	Display ON MDDI Link hibernation	Hibernation driver ON	Host – Initiated Client – Initiated (Vsync, GPIO)
STOP	OFF	Disabled	Display OFF MDDI Link OFF	Driver All OFF	RESET

SLEEP: Initial status when external power is connected to the IC.
In this state, internal oscillator is operating, and MDDI link is in hibernation state.
As no command or signal is applied to the IC except RESET input, internal logic or step-up circuit is OFF.

WAIT: After the wake-up sequence, the IC is in WAIT state. MDDI link is in SYNC, and internal logic or step-up is still OFF because no other register access or video stream packet is transferred to the IC.

NORMAL: MDDI link, step-up circuit, and internal logic circuit is ON. Register access or Video data transfer is available in NORMAL state.

IDLE: When no more video data update is needed, MDDI link is in hibernation so that interface power can be reduced. Internal step-up & logic circuits are still operating. MDDI link wakeup will be accomplished when vsync wakeup register is set before hibernation or GPIO interrupt is set.

NAP: This state is set by register access. Step-up and Internal logic is OFF, but MDDI link is ON.
MDDI link have to be in SYNC because the IC must receive commands for power save or normal operation

STOP: STOP state is set by register access (R10h). In this state, MDDI link, internal oscillator, step-up, and logic circuit are all OFF. To release STOP state, input reset signal. After reset, status is SLEEP state.

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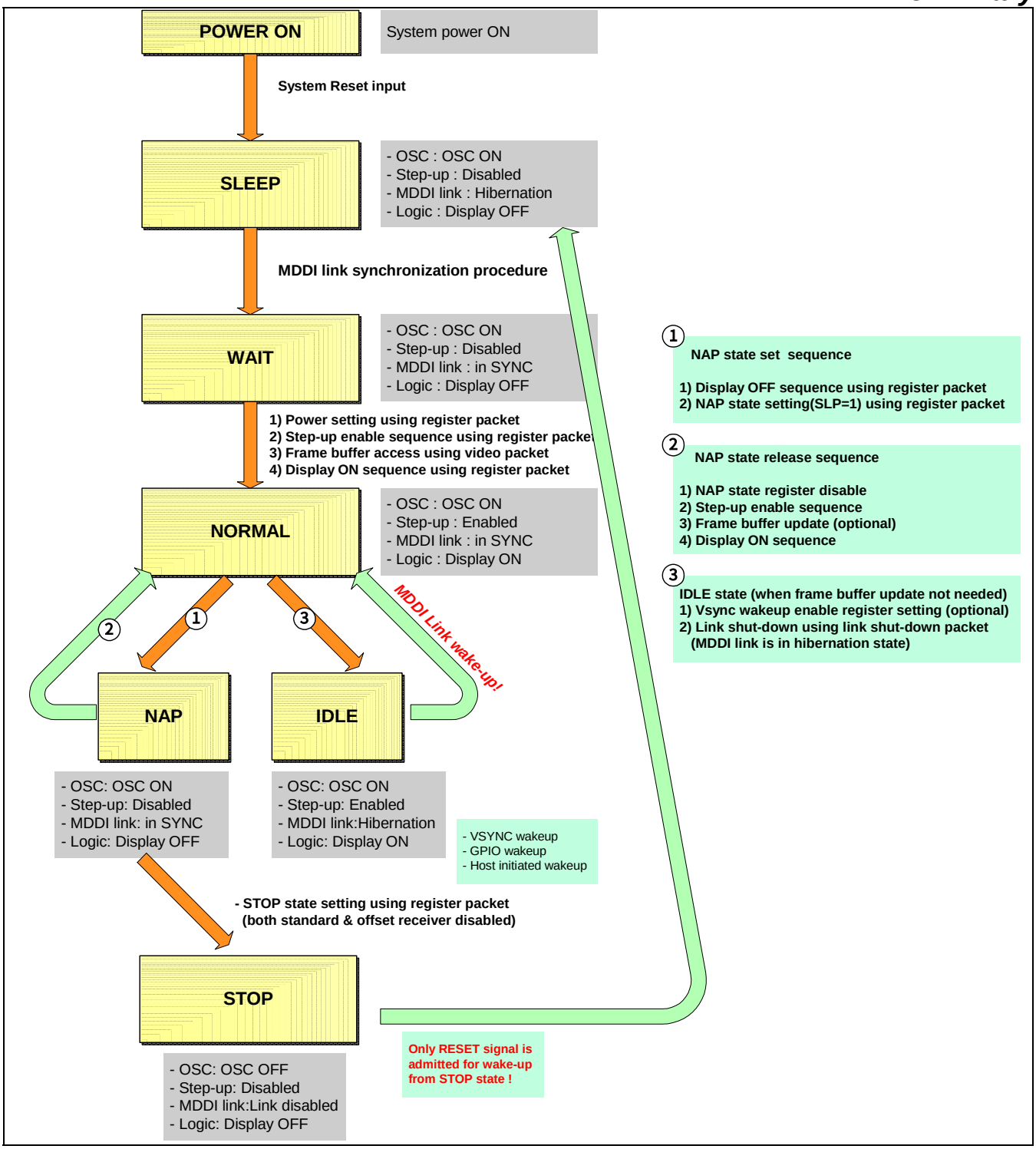


Figure 85. Operating state in MDDI mode

Preliminary

SUB PANEL CONTROL

S6D0139 support sub panel control function which controls sub panel driver IC using 80-mode protocol (CSB, RS, WRB & DB). When MDDI host (Base band modem) sends several packets to S6D0139, if the packet is for sub panel, the IC converts the packet to 80-mode protocol & sends them to sub panel driver IC. So separated line for sub panel control are not needed. After all, S6D0139 enables the sub panel driver IC which doesn't support MDDI to be applied to the system. S6D0139 supports only 80-mode 18/16 bit format for sub panel control.

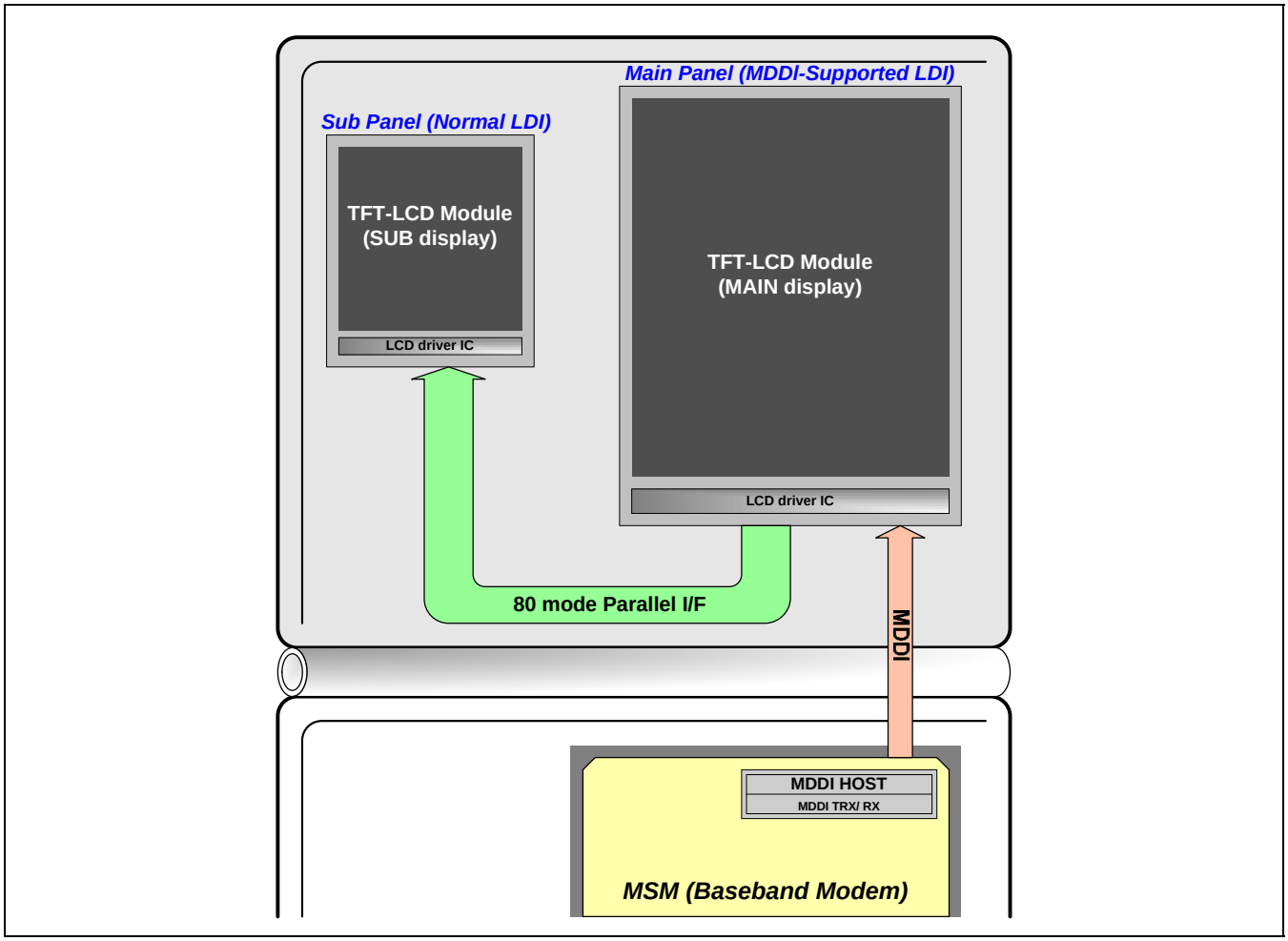


Figure 86. Schematic diagram of sub panel control function

Preliminary

MAIN / SUB PANEL SELECTION

Using 7Ah register (7Ah address can be changed using SUB_SEL register), main / sub panel data path can be selected. When S6D0139 receives register access packet (Initially 7Ah index) from MDDI host, it decodes the packet and checks the last bit of the register data field is '1' or '0'. If the last bit is '0', the following register access packet or video stream packet is transferred to the sub panel control signal generation block.

Sub panel selection address (Initially 7Ah) can be changed using SUB_SEL register. Do not change the SUB_SEL value to previously occupied address.

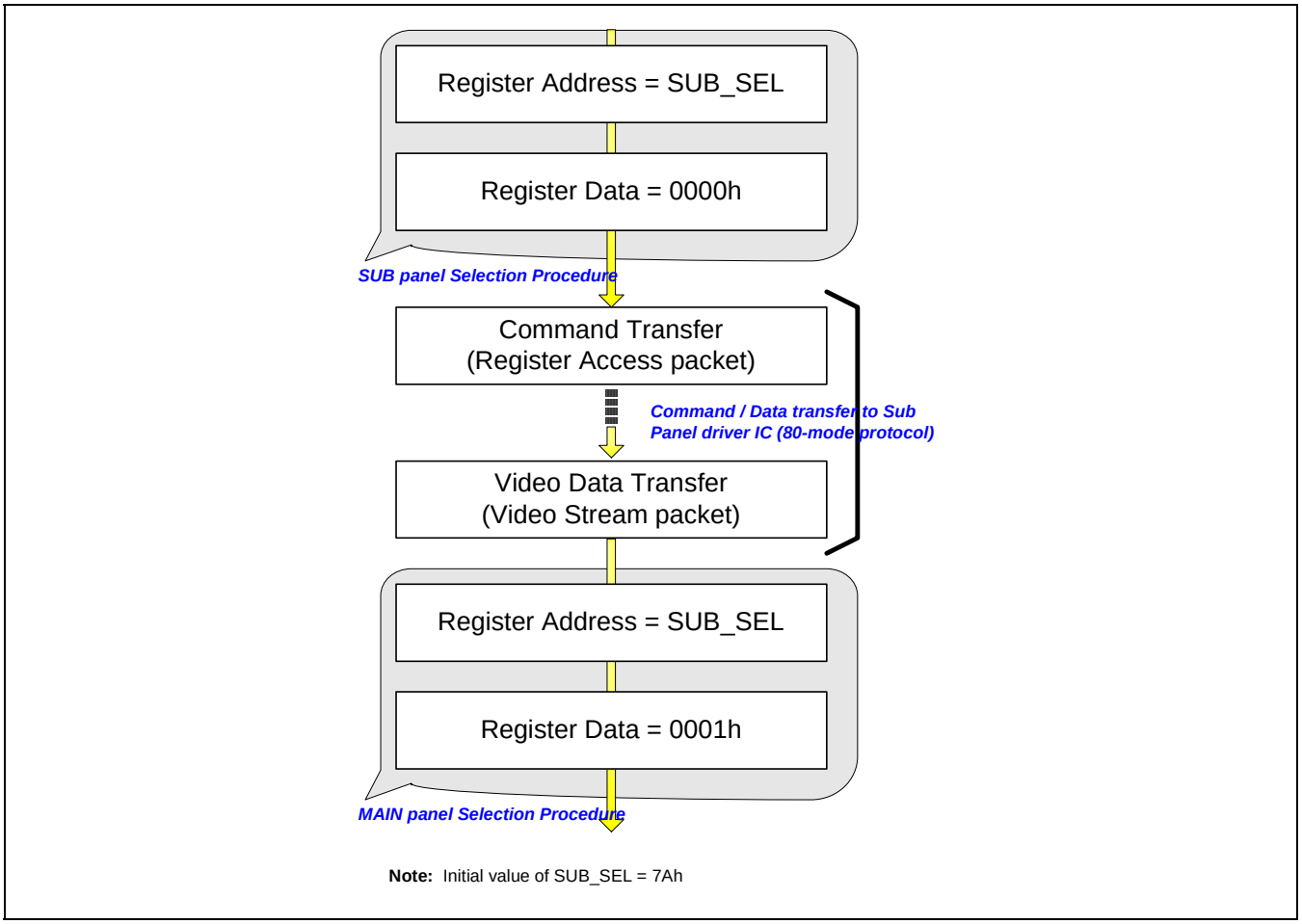


Figure 87. Main / Sub panel selection procedure

When video data is transferred to the sub panel driver IC via S6D0139, additional GRAM access command (normally 22h) is automatically generated in S6D0139.

Preliminary

SUB PANEL CONTROL TIMING

1. TFT type sub panel timing

1.1 Register data transfer timing

If sub panel is selected, and sub panel type is TFT, register setting is executed like below figure.
Register data is transferred through S_DB[17:10] & S_DB[8:1] in 18/16 bit type. If 9/8 bit type is used, data is transferred thorough S_DB[17:10]. Refer to sub panel control(15h index) section.

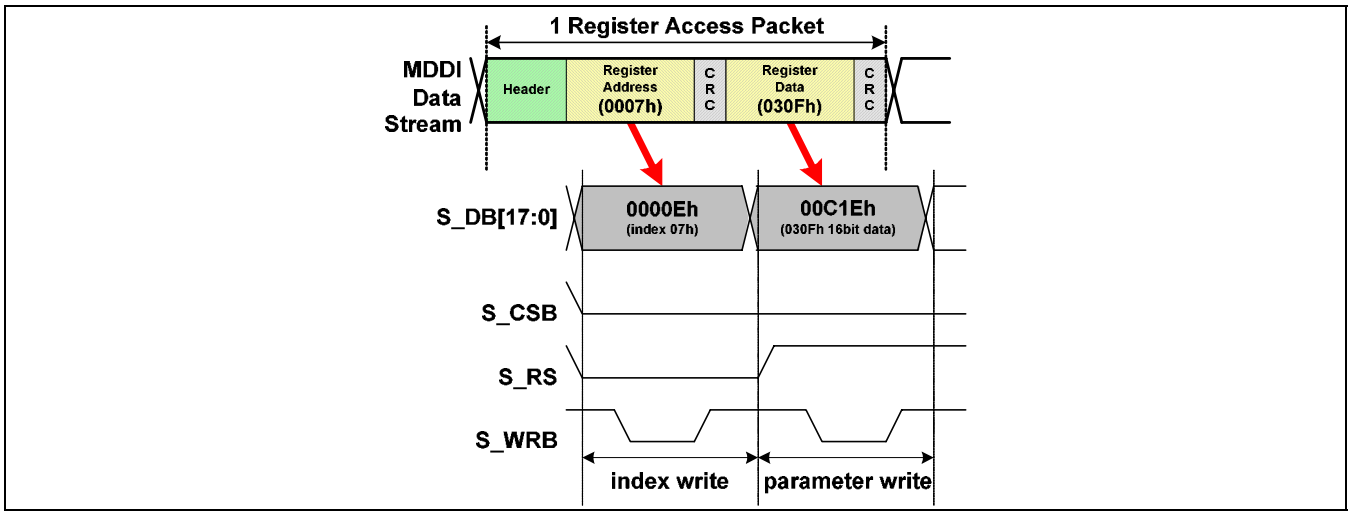


Figure 88. 18/16 bit type register access data transfer

In 9/8 bit mode, S_DB[17:10] is used. In this mode, data is transferred at two times. First transfer is MSB 8bit and second transfer is LSB 8bit.

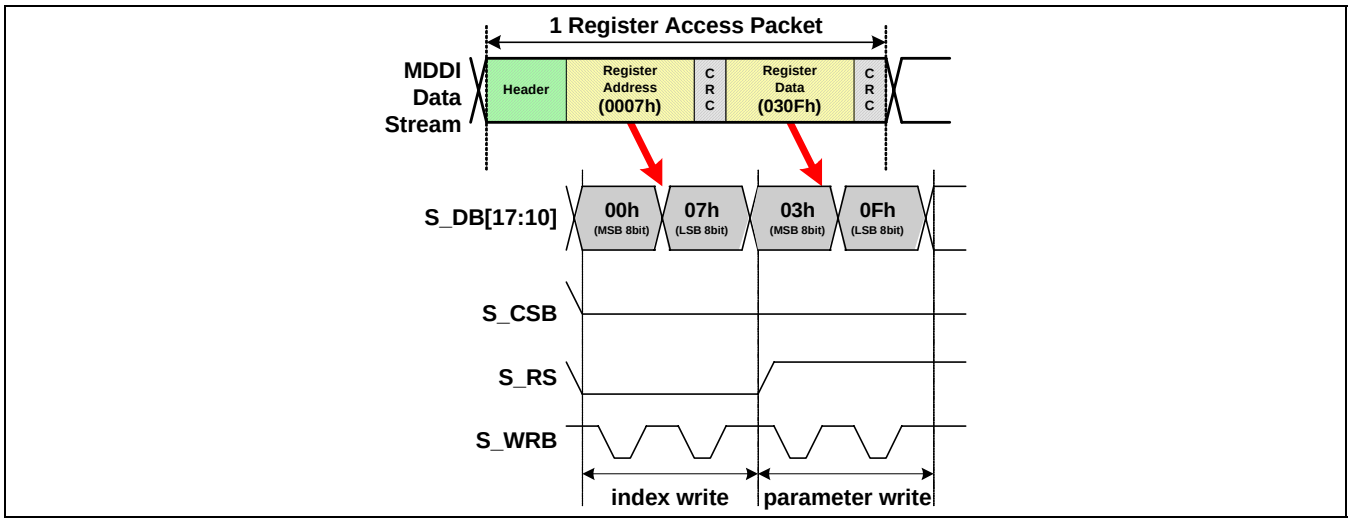


Figure 89. 9/8 bit type register access data transfer

This figure shows register setting in 18/16 bit & 68 mode. In 68 mode, S_WRB must be connected to E_RDB of sub panel module. RW_WRB of sub panel module must be tied to VSS. Because S6D0139 only writes data to sub panel module.

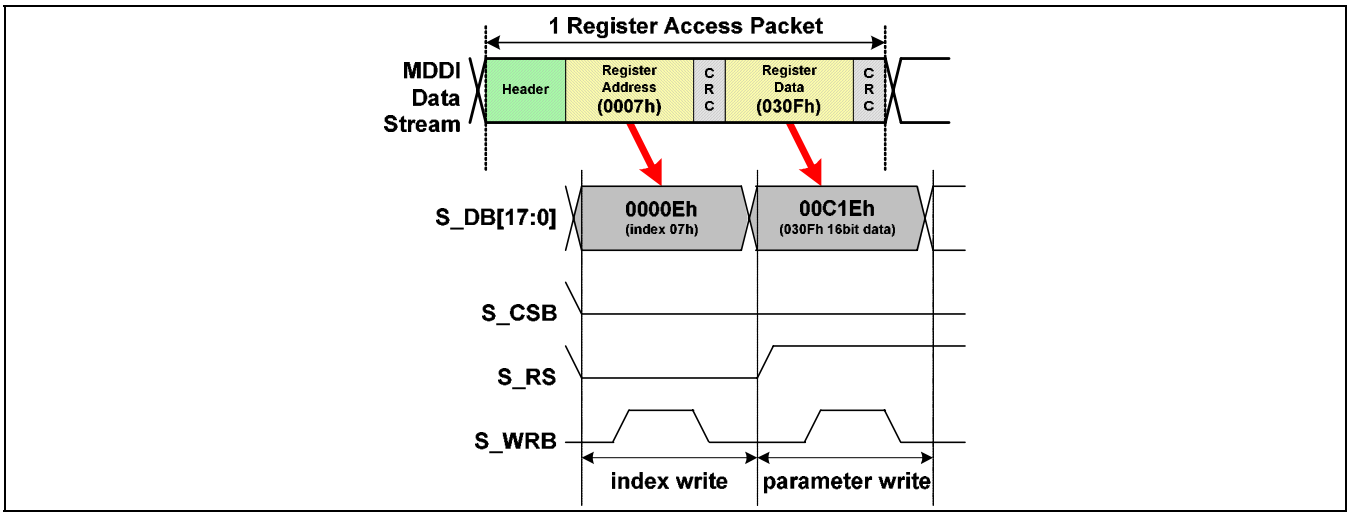


Figure 90. 68 mode 18 bit register data transfer

1.2 Video data transfer timing

In TFT type sub panel, STN_EN register in 15h index is “0”, and if user wants to use 68-mode interface protocol, then MPU_MODE is set to “1”. 18/16/9/8 mode is selected as setting SUB_IM register. Refer to 15h index description.

This figure shows 80 mode 18 bit Video data transfer.

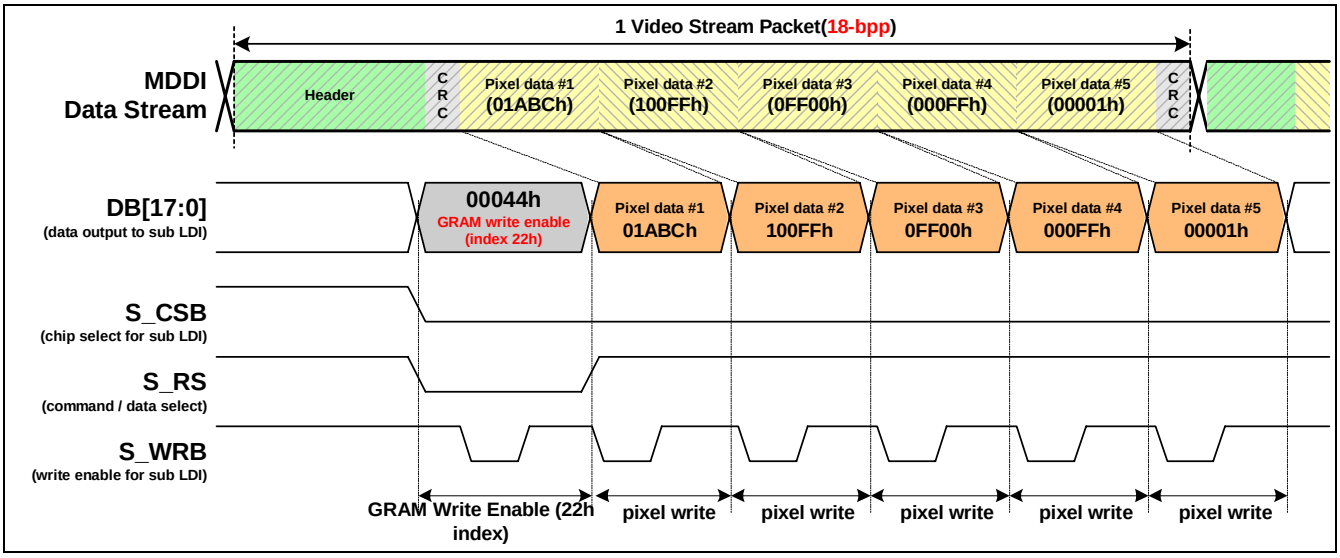


Figure 91. 80 mode 18 bit video data transfer

Preliminary

This fugure shows 68 mode 18 bit. In 68 mode, S_WRB must be connected to E_RDB of sub panel module. RW_WRB of sub panel module must be tied to VSS. Because S6D0139 only writes data to sub panel module.

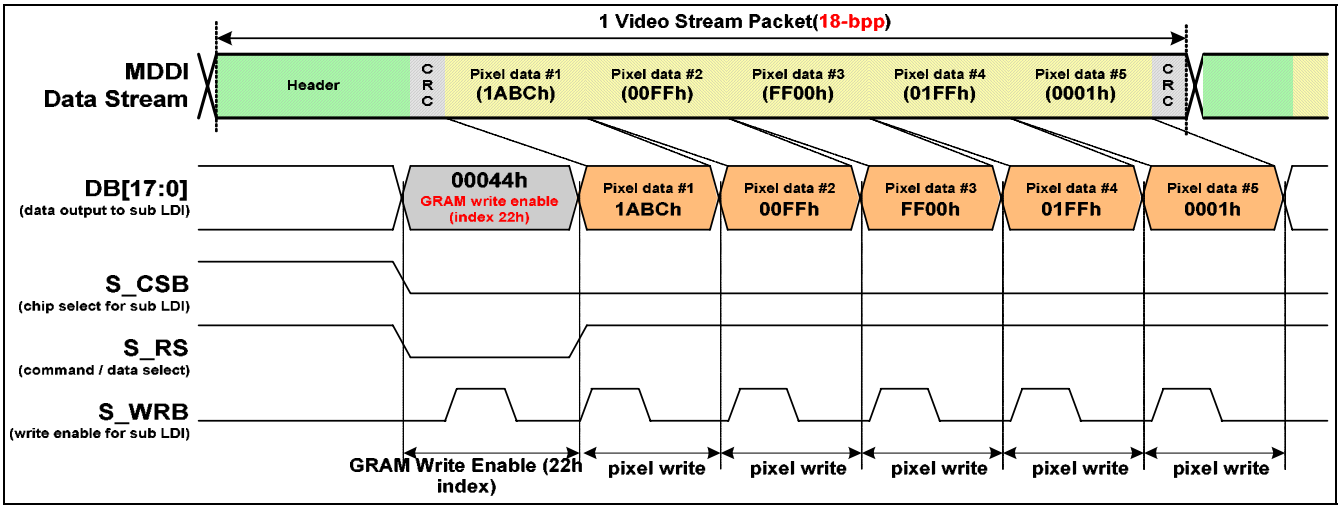


Figure 92. 68 mode 18 bit video data transfer

This figure shows 80-mode 16 bit Video data transfer.

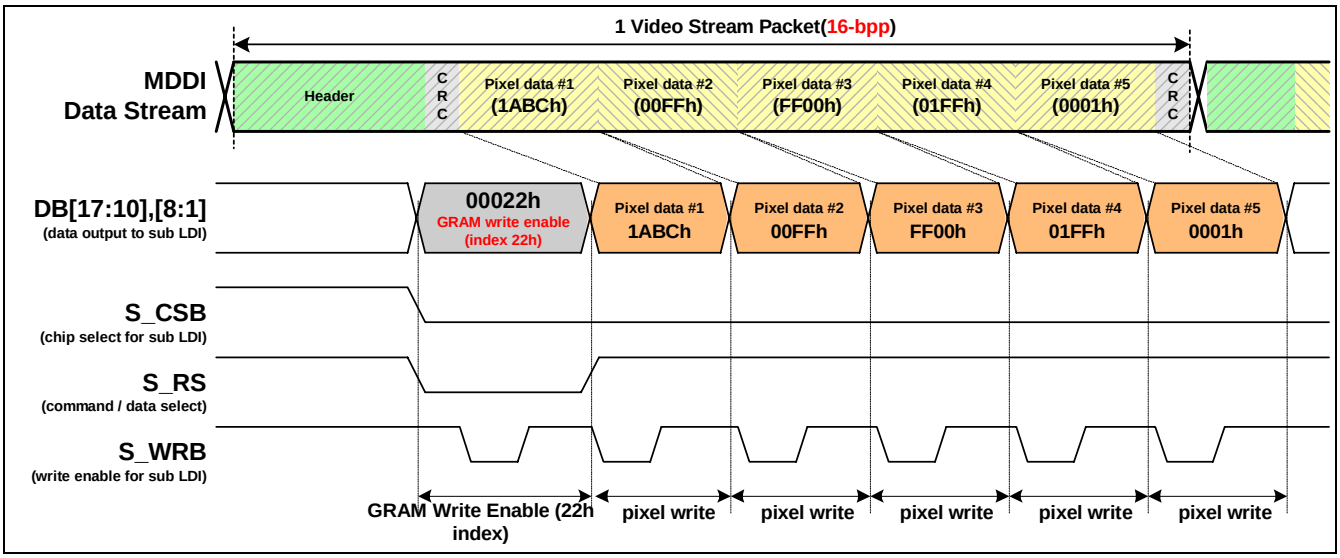


Figure 93. 80 mode 16 bit video data transfer

This figure shows 80-mode 9 bit Video data transfer.

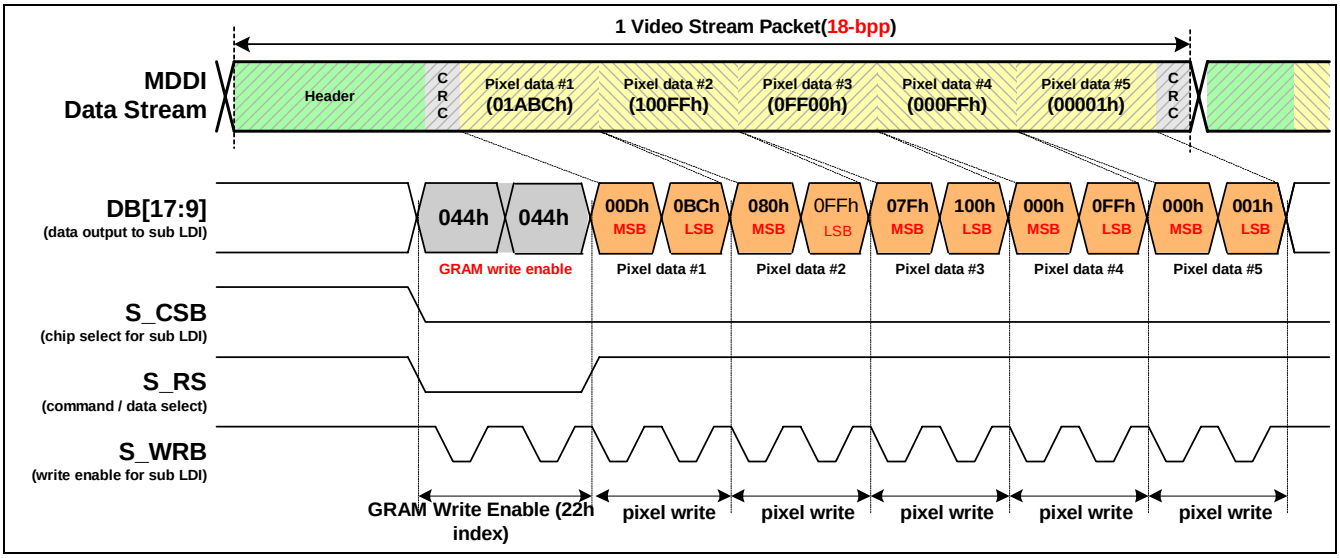


Figure 94. 80 mode 9 bit video data transfer

This figure shows 80-mode 8 bit Video data transfer.

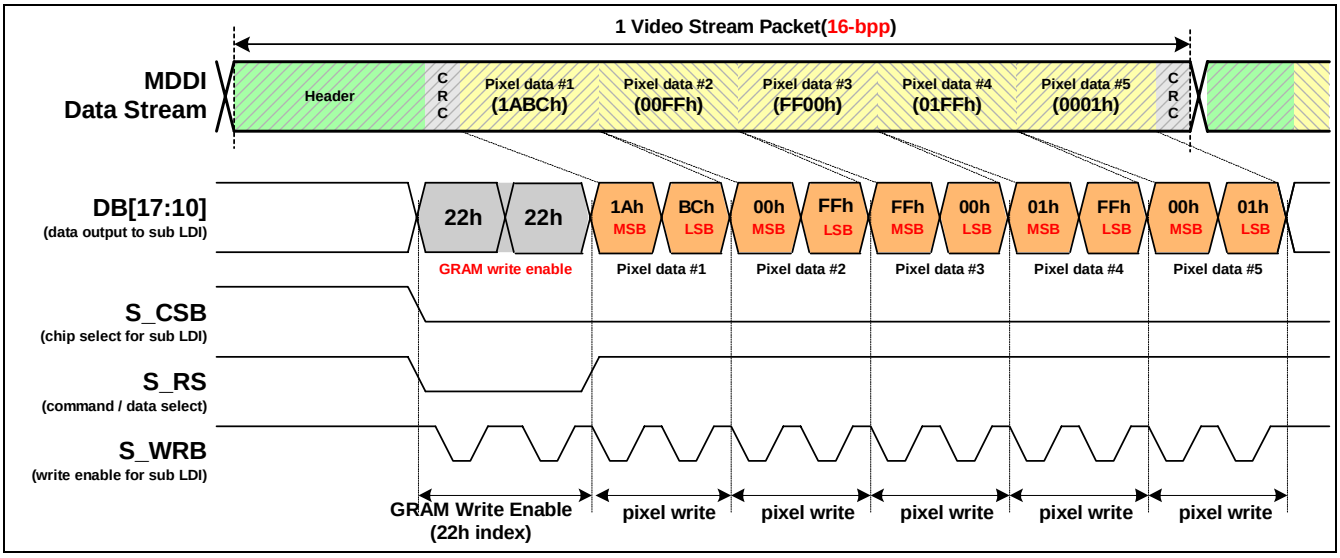


Figure 95. 80 mode 8 bit video data transfer

Preliminary

2. STN type sub panel timing

2.1 Register data transfer timing

This figure shows conventional type STN mode register data setting. Conventional type does not include parameter. Instruction type is only 8bit. To use STN type, STN_EN is set to “1”. In STN type, S6D0139 controls S_RS pin using register address[0] in register access packet. Register address[0] is “0”, then S_RS is set to “0”, and register address[0] is “1”, S_RS is set to “1”. Refer to sub panel control(15h index) section.

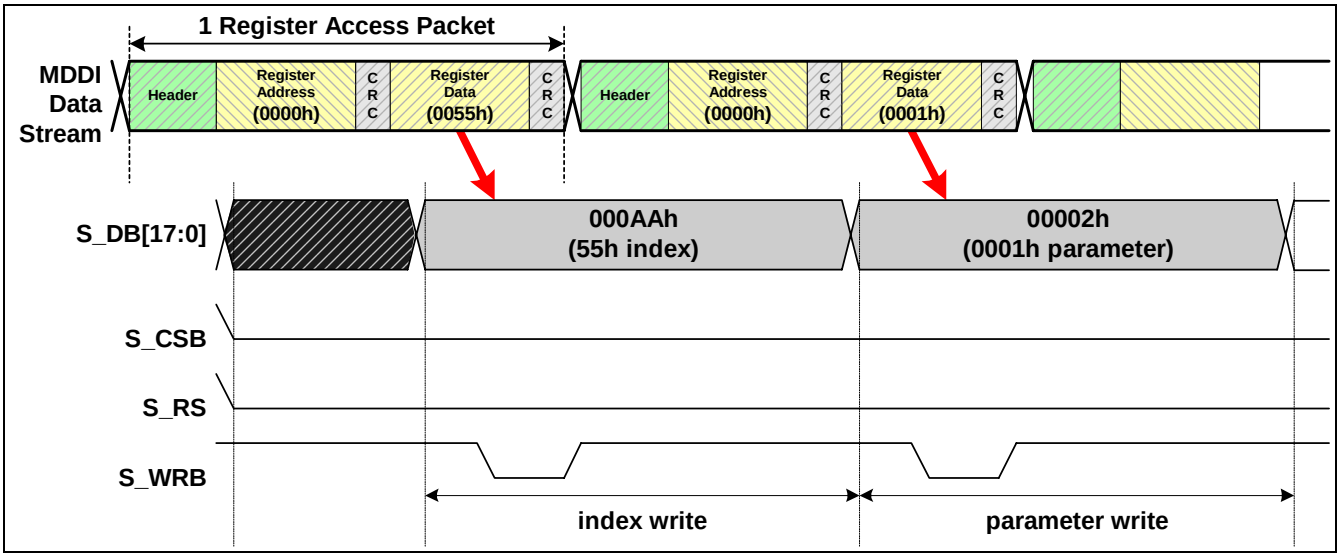


Figure 96. 80 mode STN type convetional register instruction

This type is used to include parameter. When instruction is transferred, S_RS is zero, and when parameter is transferred, S_RS is “1”. S_RS is controlled using register address[0] of register access packet.

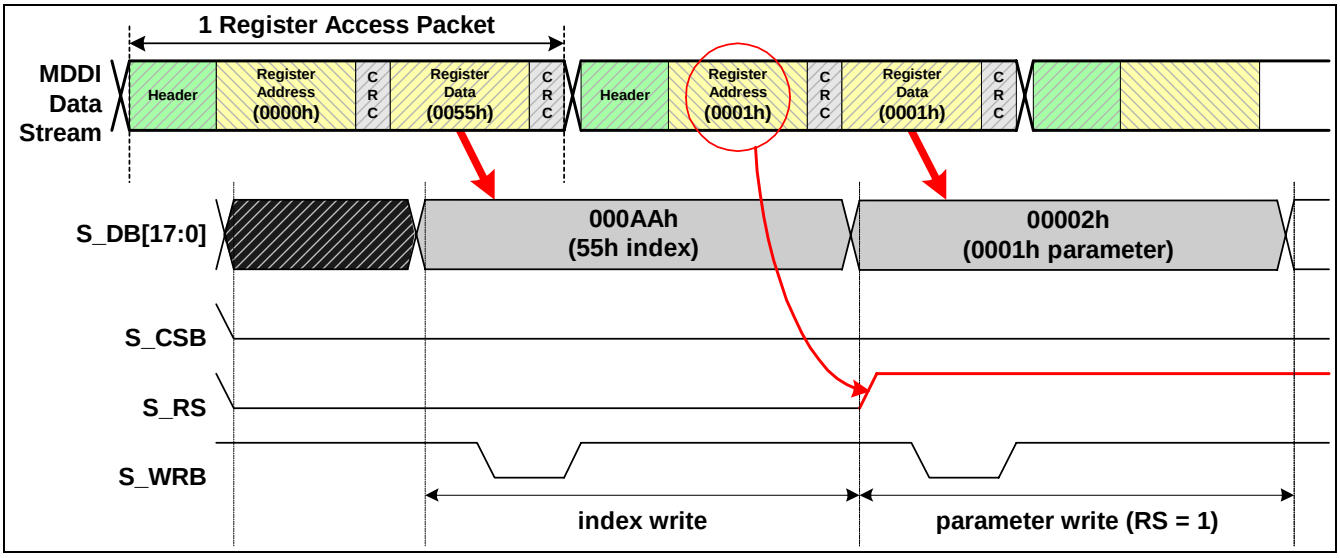


Figure 97. 80 mode STN type included parameter

2.2 Video data transfer timing

In STN mode, video data start register (like 22H is TFT mode) does not need generally. But some STN type needs video data start register. If those type STN DDI is used, user has to set the register index.
This figure shows STN 16 bit mode video data transfer.

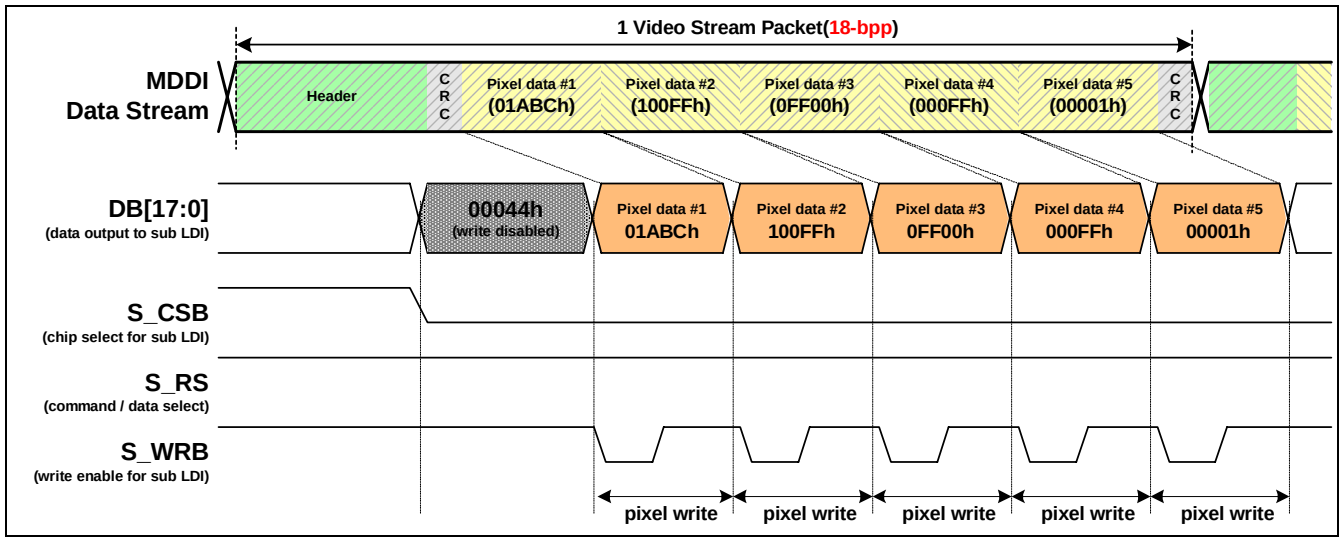


Figure 98. 80 mode STN type 16 bit video data transfer

This figure shows STN 8bit mode video data transfer. If STN video data is 16bit mode, data transfer is executed during 2 times. Fist transfer is MSB 8bits, and second is LSB 8bits.

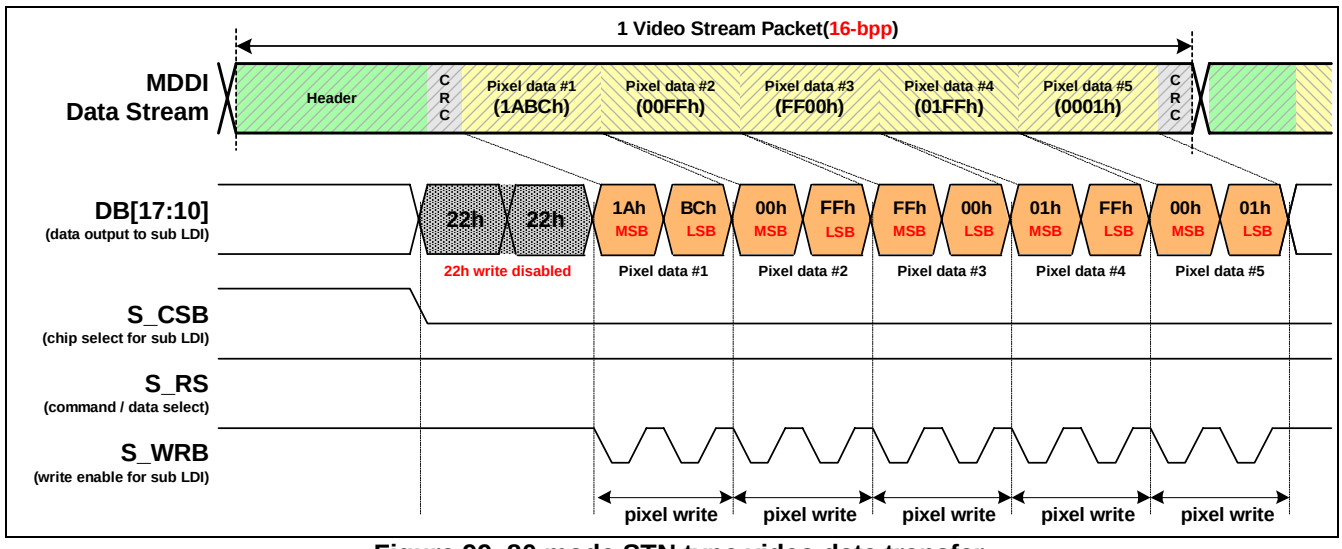
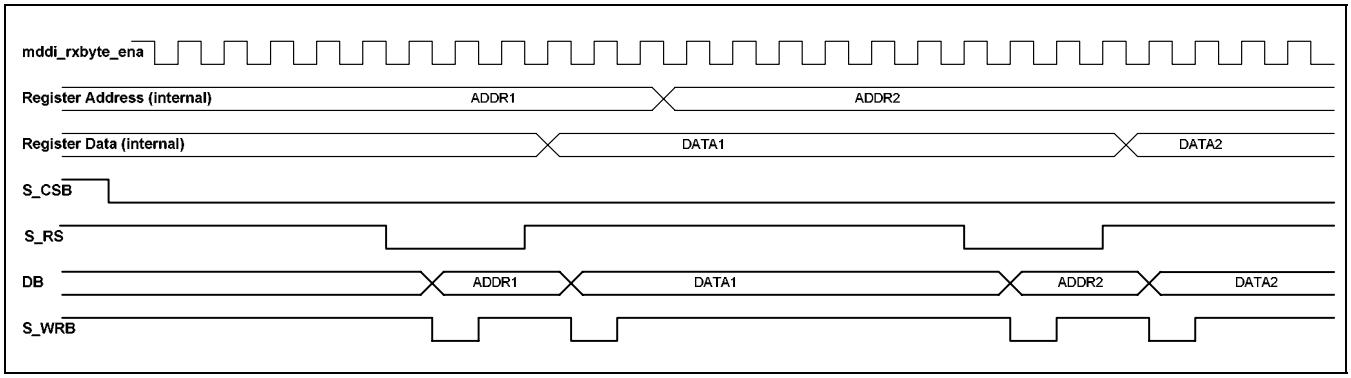


Figure 99. 80 mode STN type video data transfer

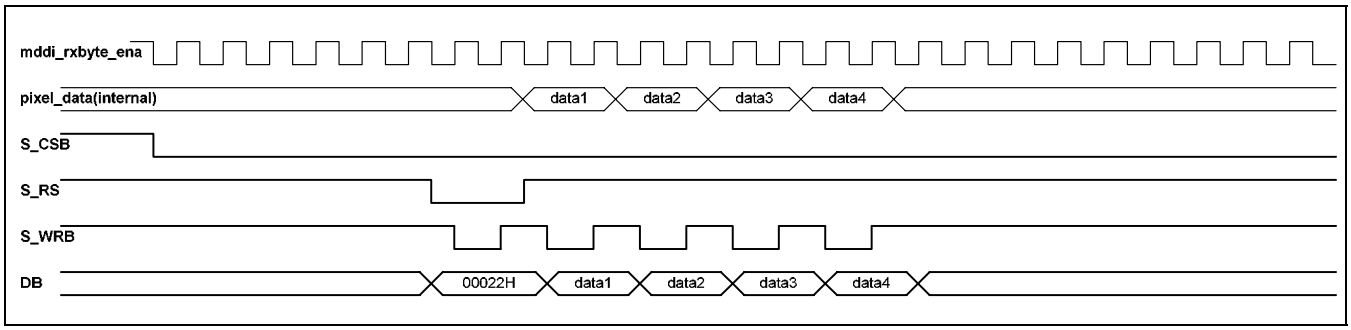
Preliminary

SUB PANEL CONTROL TIMING

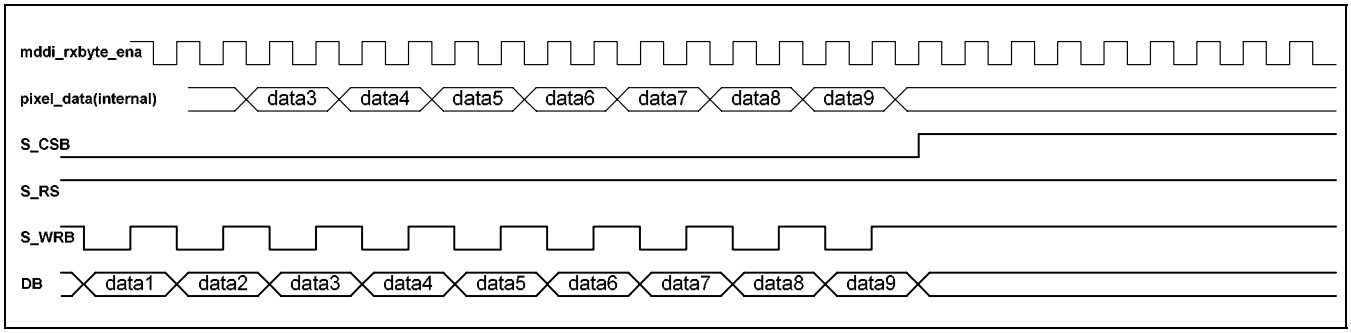
1.Index/parameter write for sub panel LDI



2. Image data write for sub panel LDI



3. Change data path from sub panel to main panel



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MDDI INTEGRATED SYSTEM STRUCTURE

MDDI support display system which incorporates GPIO and Sub panel control is seen below.
S6D0139 can display to a maximum of QVGA (240x320) resolution and sub panel resolution can be chosen according to the system requirement.

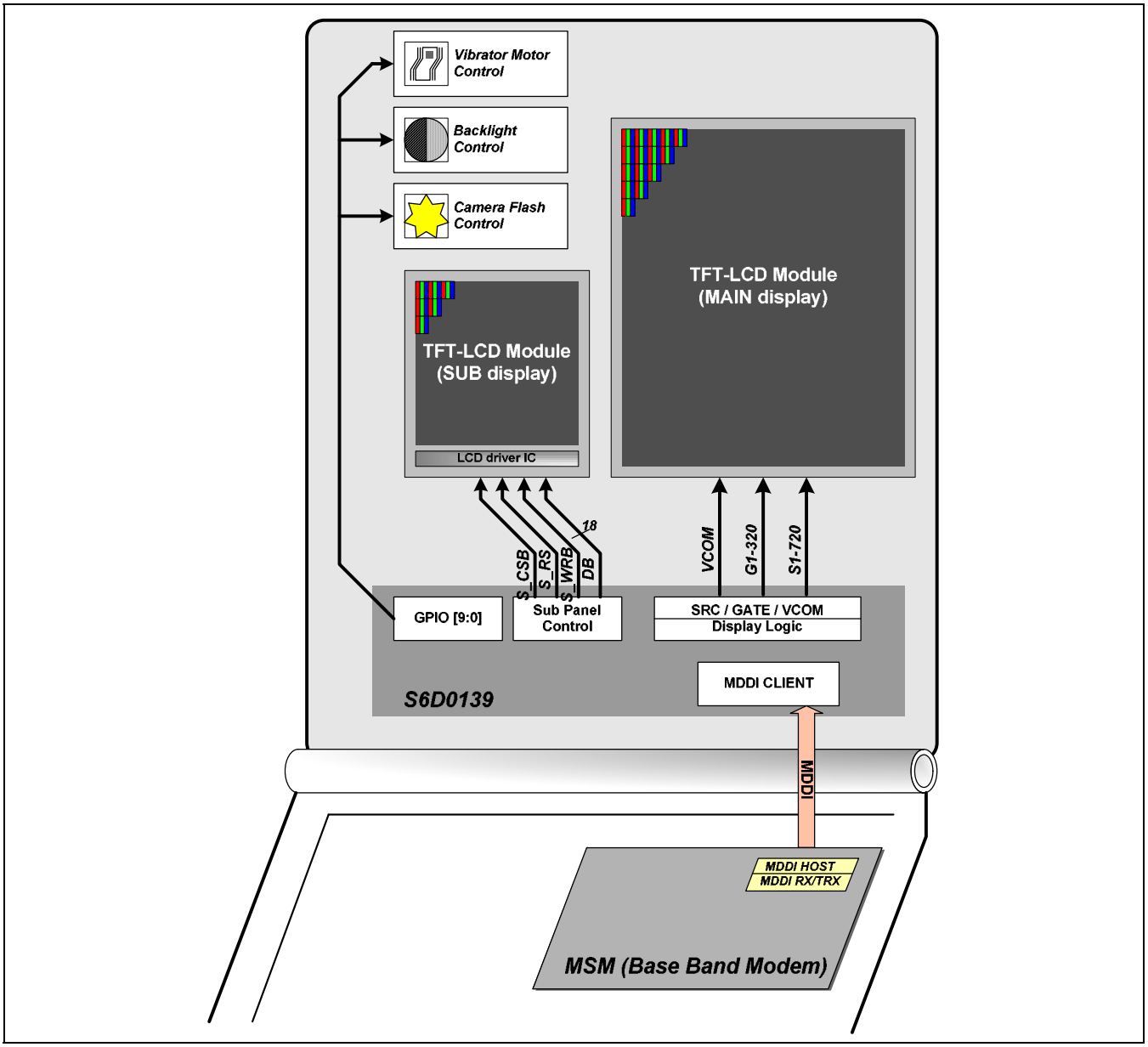

Figure 100. MDDI-integrated system structure

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MTP CALIBRATION MODE

S6D0139 supports the MTP function. This figure is a operation diagram of MTP.
Initially, MTP cell is not programmed and has VCOMH(6b'00000). When the external reset is applied, MTP mode is On.

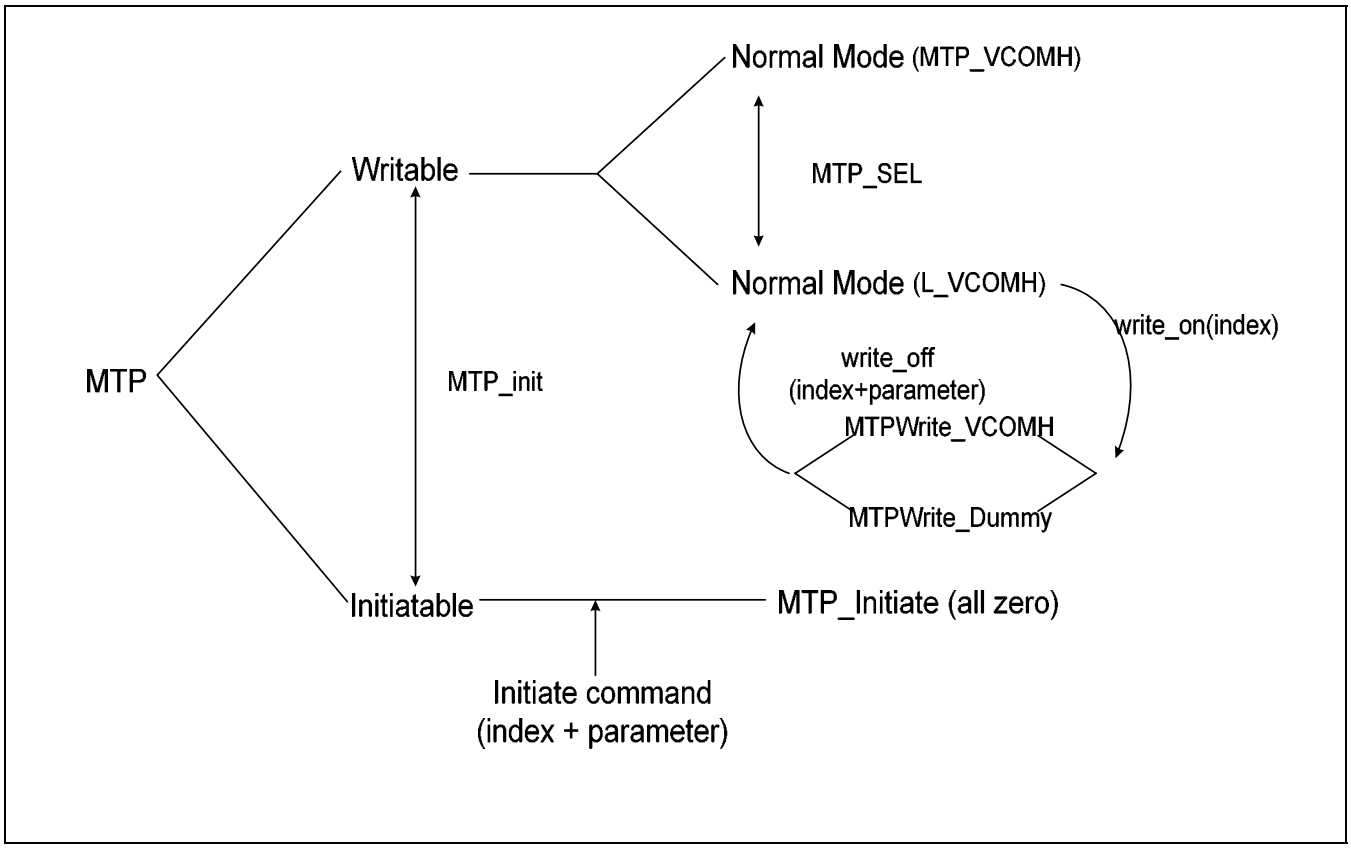

Figure 101. MTP Operation Diagram

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MTP CELL STRUCTURE

MTP (Multi Time Programmable) has been implemented on the S6D0139. The MTP Cell stores the offset volume for VCOMH calibration after device has been assembled and calibrated on a LCD module. For MTP programming, MTP_G, MTP_D pin used.

The MTP block of the S6D0139 consists of one array which has 7 bits. 1 bit is used for MTP mode protection bit, and 6 bits are used for VCOMH calibration (VCM0~VCM5). MPRT can be read or be written automatically in this LSI.

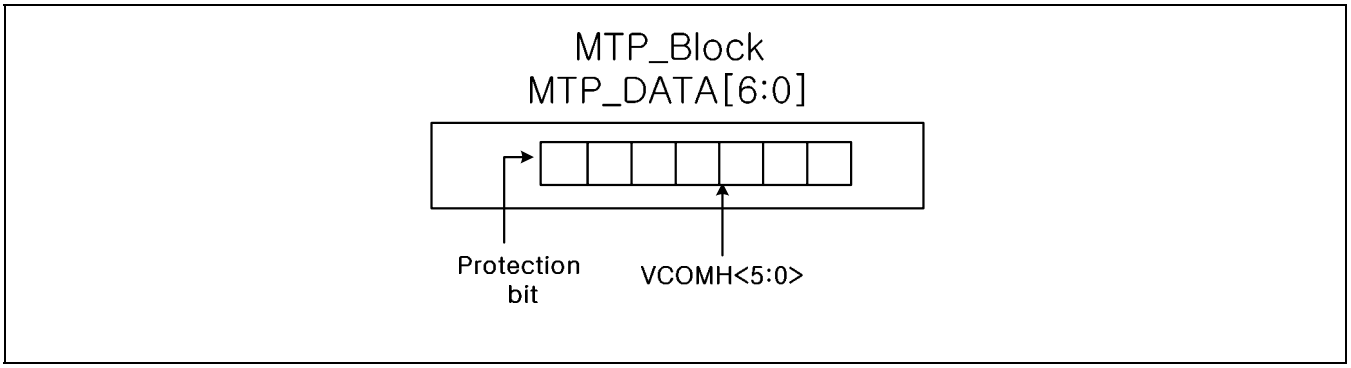

Figure 102. MTP Cell structure

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MTP TIMING DIAGRAM

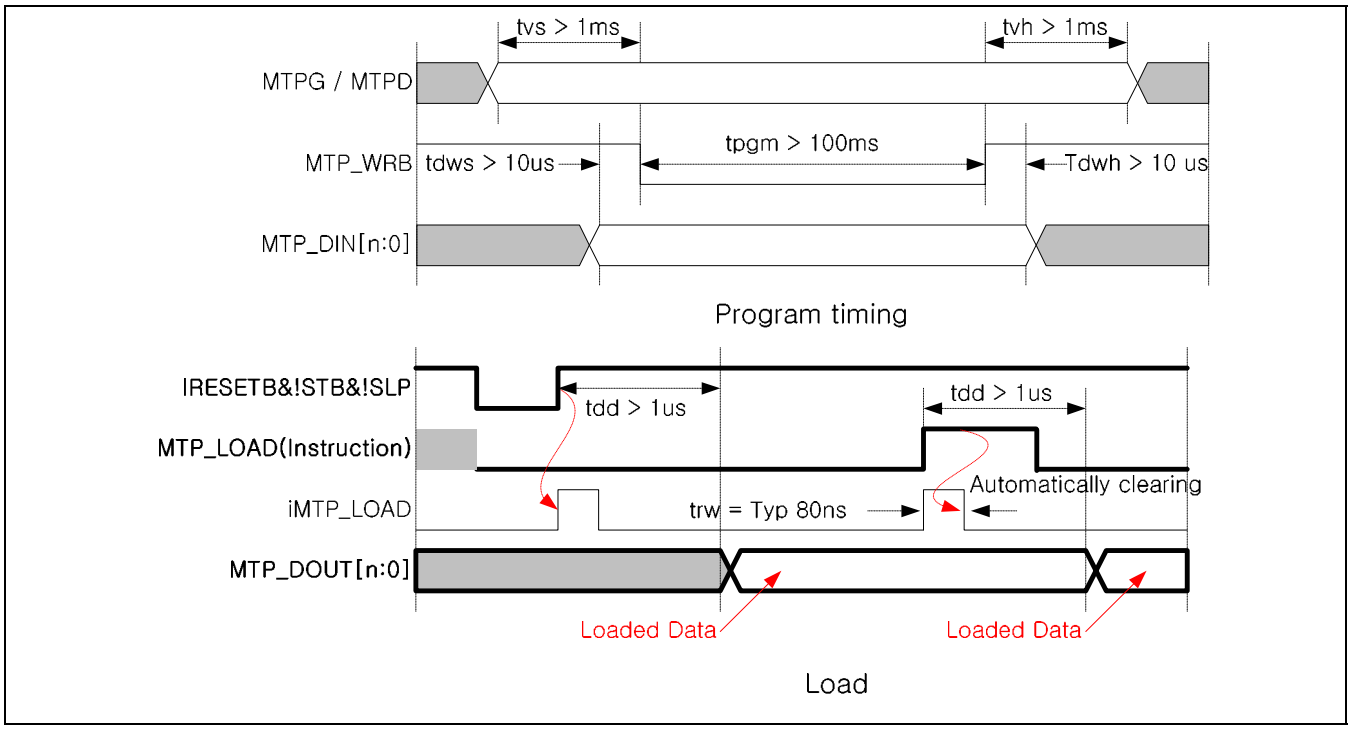

Figure 103. MTP Timing Diagram

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MTP SEQUENCE FLOW

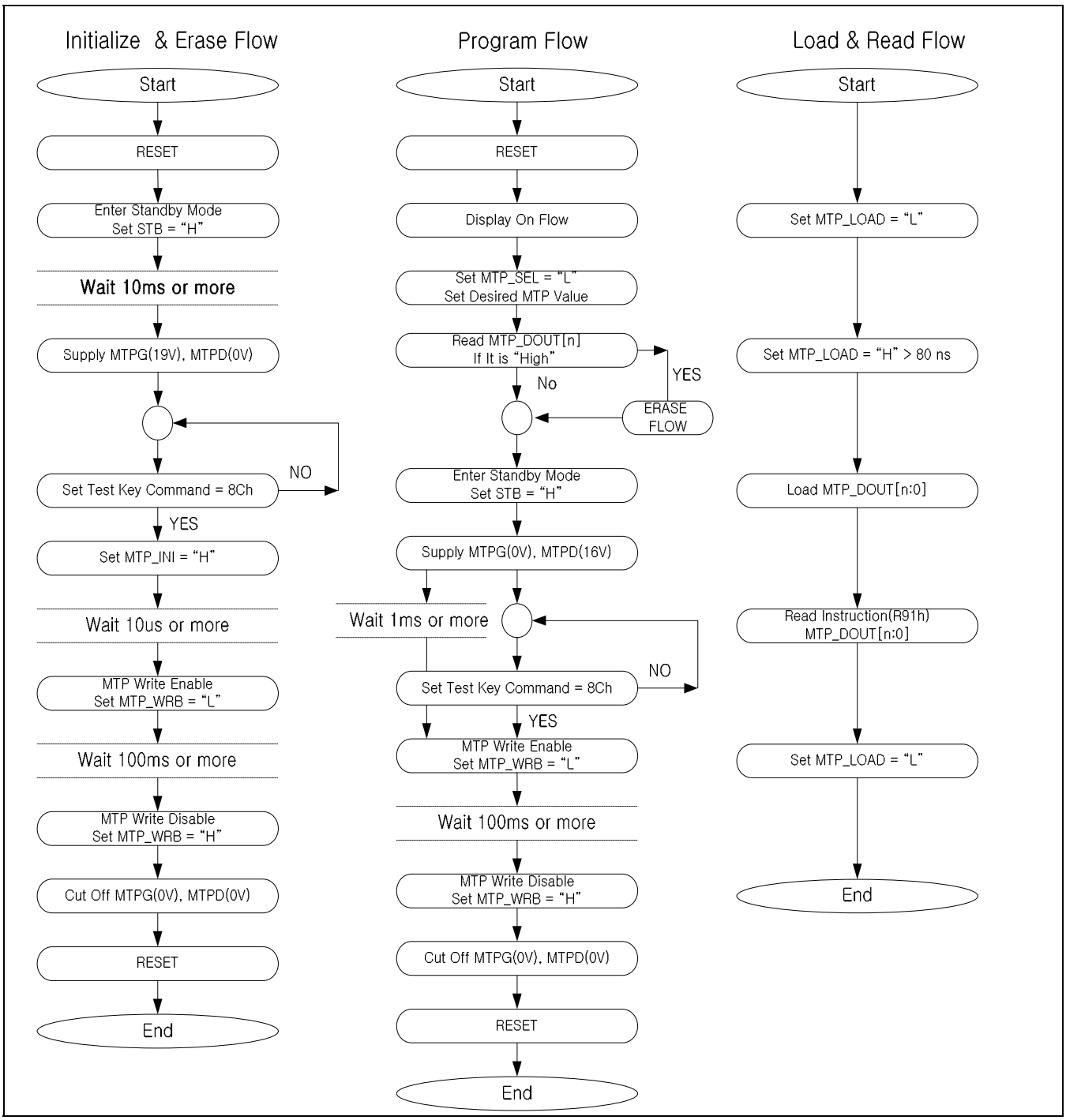

Figure 104. MTP Sequence Flow

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MIE FUNCTION

S6D0139 has a special image enhancement function, MIE(Mobile Image Enhancement) which enhances the luminance/contrast of original image and reduces power consumption of backlight. When MIE function is enabled, the original image data is written on RAM after being enhanced. MIE can operate without regard to interface mode, like as RGB I/F and CPU I/F.

During one frame image data transition, the feature of current frame is analyzed and the gamma value is calculated after end of transition. One of 9 gamma tables is selected by the calculated gamma value and the selected gamma table provides enhancement gain of each image pixel data for next one frame transition.

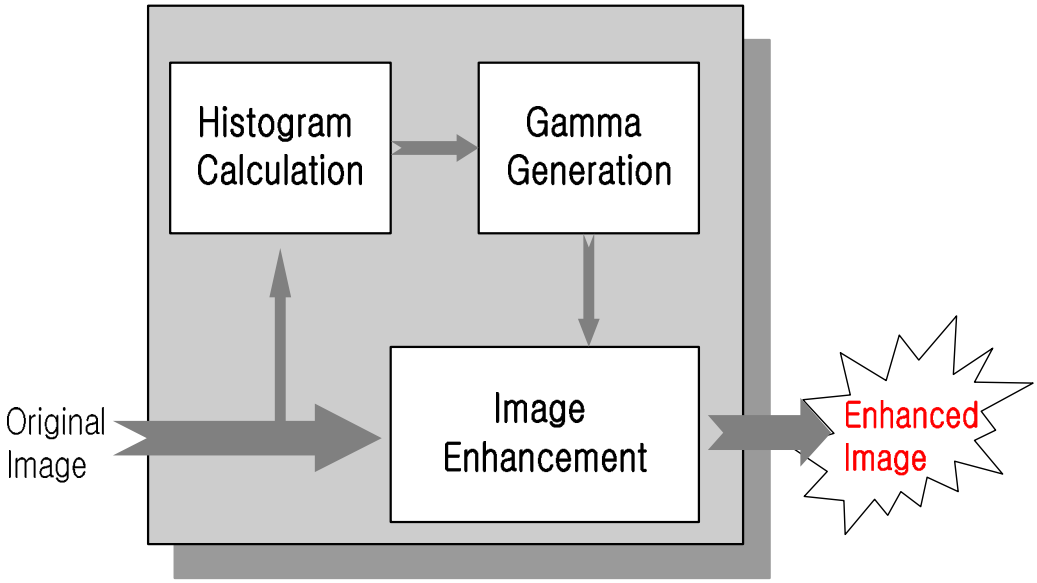

Figure 105. Operation of MIE

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MIE function has 3 modes “Normal/Halt/Off” and 3 sets of gamma table according to the values of MIE_MODE1-0 and SEL_TABLE1-0. The mode and gamma table of MIE are updated only before one frame image transition is started. If the register values of MIE_MODE1-0, SEL_TABLE1-0 are changed during transition, it will be updated after end of one frame transition.

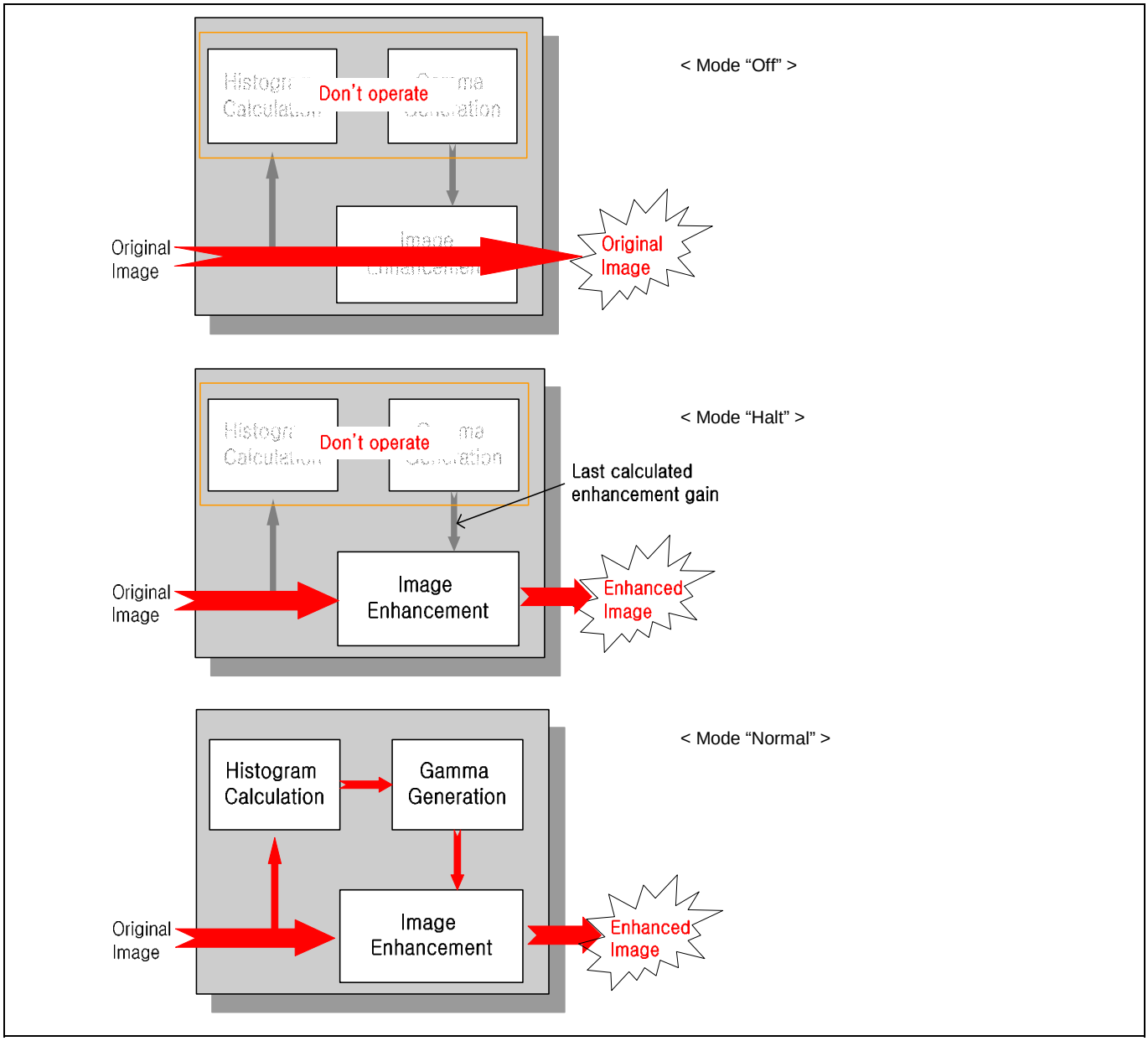


Figure 106. MIE mode and operation

Preliminary

WINDOW ADDRESS FUNCTION

When data is written to the on-chip GRAM, a window address-range that is specified by the horizontal address register (start: HSA7-0, end: HEA 7-0) and vertical address register (start: VSA8-0, end: VEA8-0) can be updated consecutively.

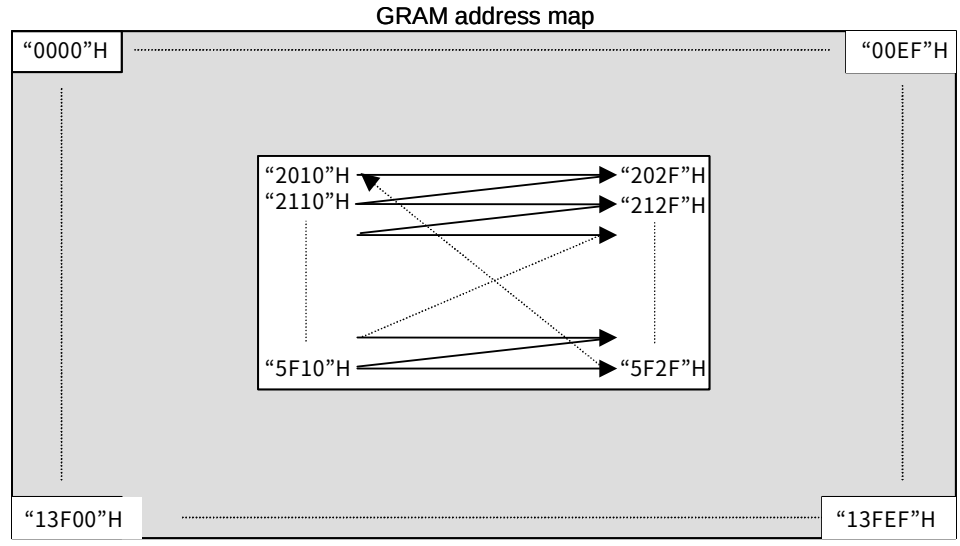
Data is written to addresses in the direction specified by the I/D1-0bit. When image data, etc. is being written, data can be written consecutively without thinking of a data wrap by doing this.

The window must be specified to be within the GRAM address area described as in the following example. Addresses must be set within the window address.

[Restriction on window address-range settings]

(horizontal direction) 00H ≤ HSA7-0 ≤ HEA7-0 ≤ EFH
(vertical direction) 00H ≤ VSA8-0 ≤ VEA8-0 ≤ 13F H

[Restriction on address settings during the window address]
(RAM address) HSA7-0 ≤ AD7-0 ≤ HEA7-0
VSA8-0 ≤ AD16-8 ≤ VEA8-0



Window address range specification area
HSA7-0 = "10"H HSE7-0 = "2F"H
VSA8-0 = "20"H VEA8-0 = "5F"H

I/D = 1 (increment)
AM = 0 (horizontal writing)

Figure 107. Example of address operation in the window address specification

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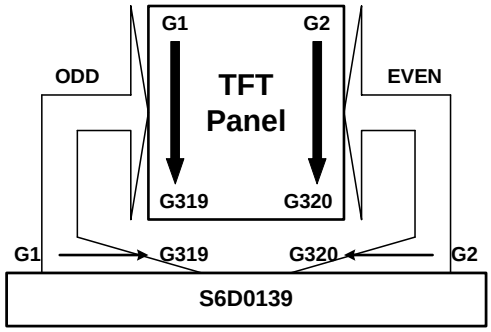
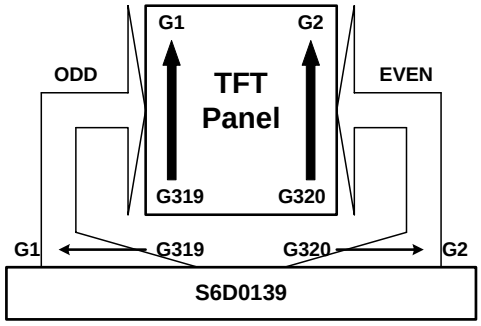
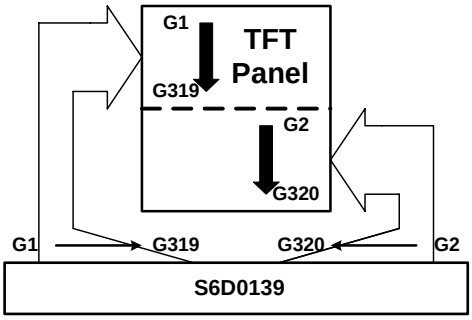
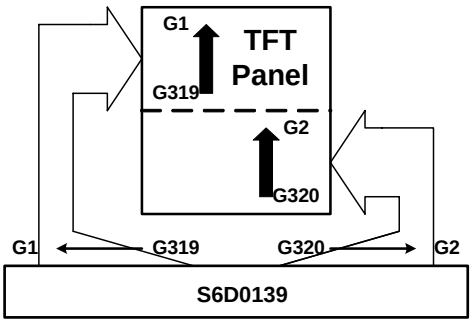
GATE DRIVER SCAN MODE SETTING

GS bit sets the gate scan mode of S6D0139, and determines the scan direction, whether the gate driver scans in the forward or reverse direction.

Figure 108. Scan mode setting

SM	GS	Scan Mode	
0	0		G1➔G2➔G3➔ G4➔····➔G317➔ G318➔G319➔G320
0	1		G320➔G319➔G318 G317➔····➔G4➔ G3➔G2➔G1
1	0		G1➔G3➔ G5➔····➔G317➔G319 G2➔G4➔ G6➔····➔G318➔G320
1	1		G320➔G318➔ G316➔····➔G4➔G2 G319➔G317➔ G315➔····➔G3➔G1

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GAMMA ADJUSTMENT FUNCTION

The S6D0139 provides the gamma adjustment function to display 262,144 colors simultaneously. The gamma adjustment executed by the gradient adjustment register and the micro-adjustment register that determines 8 grayscale levels. Furthermore, since the gradient adjustment register and the micro-adjustment register have the positive polarities and negative polarities, adjust them to match LCD panel respectively.

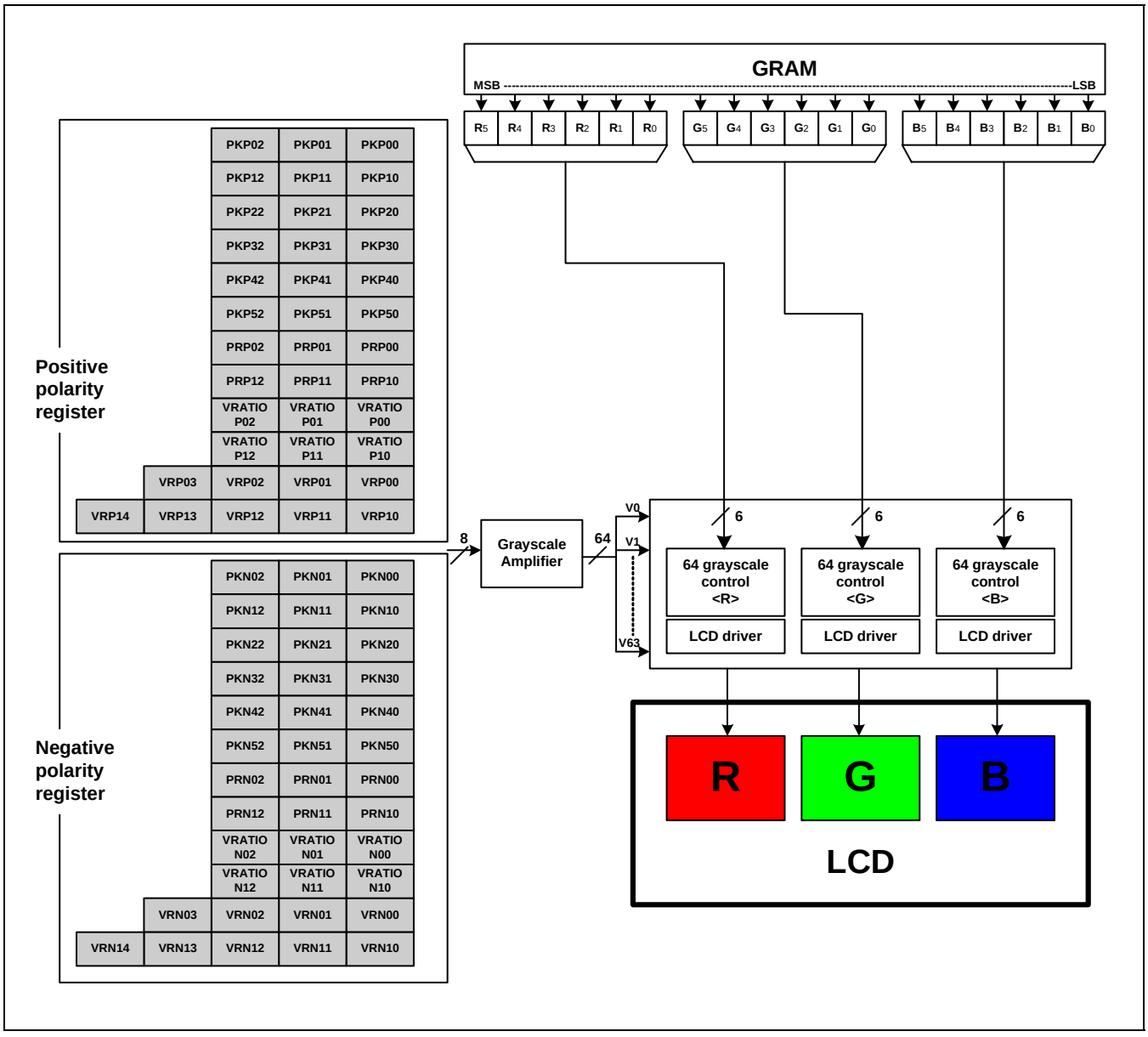

Figure 109. Grayscale control

Preliminary

STRUCTURE OF GRAYSCALE AMPLIFIER

The structure of the grayscale amplifier is shown as below. Determine 8-level (VIN0-VIN7) by the gradient adjuster and the micro adjustment register. The internal ladder resistance splits each level and levels from V0 to V63 are generated.

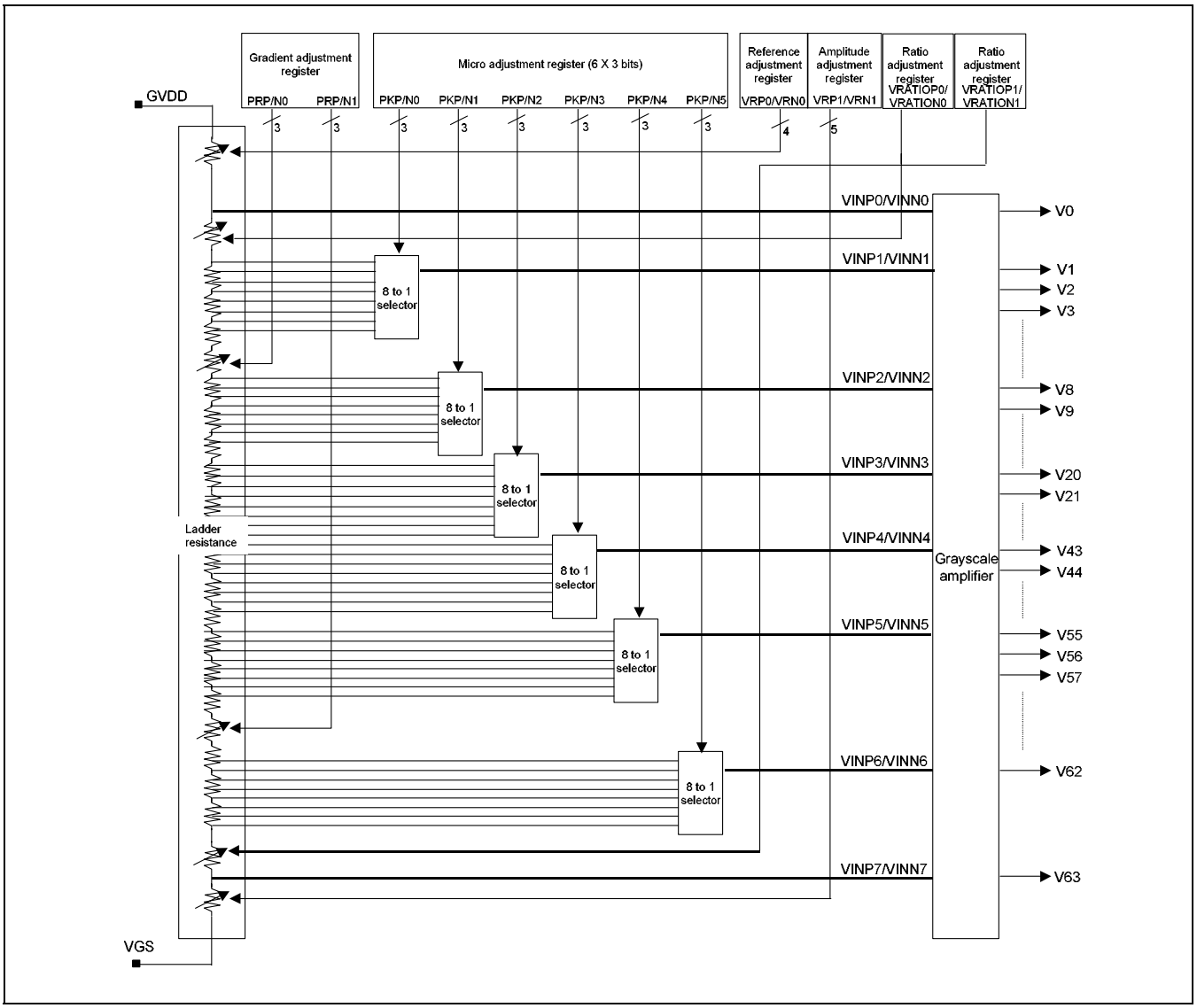

Figure 110. Structure of grayscale amplifier

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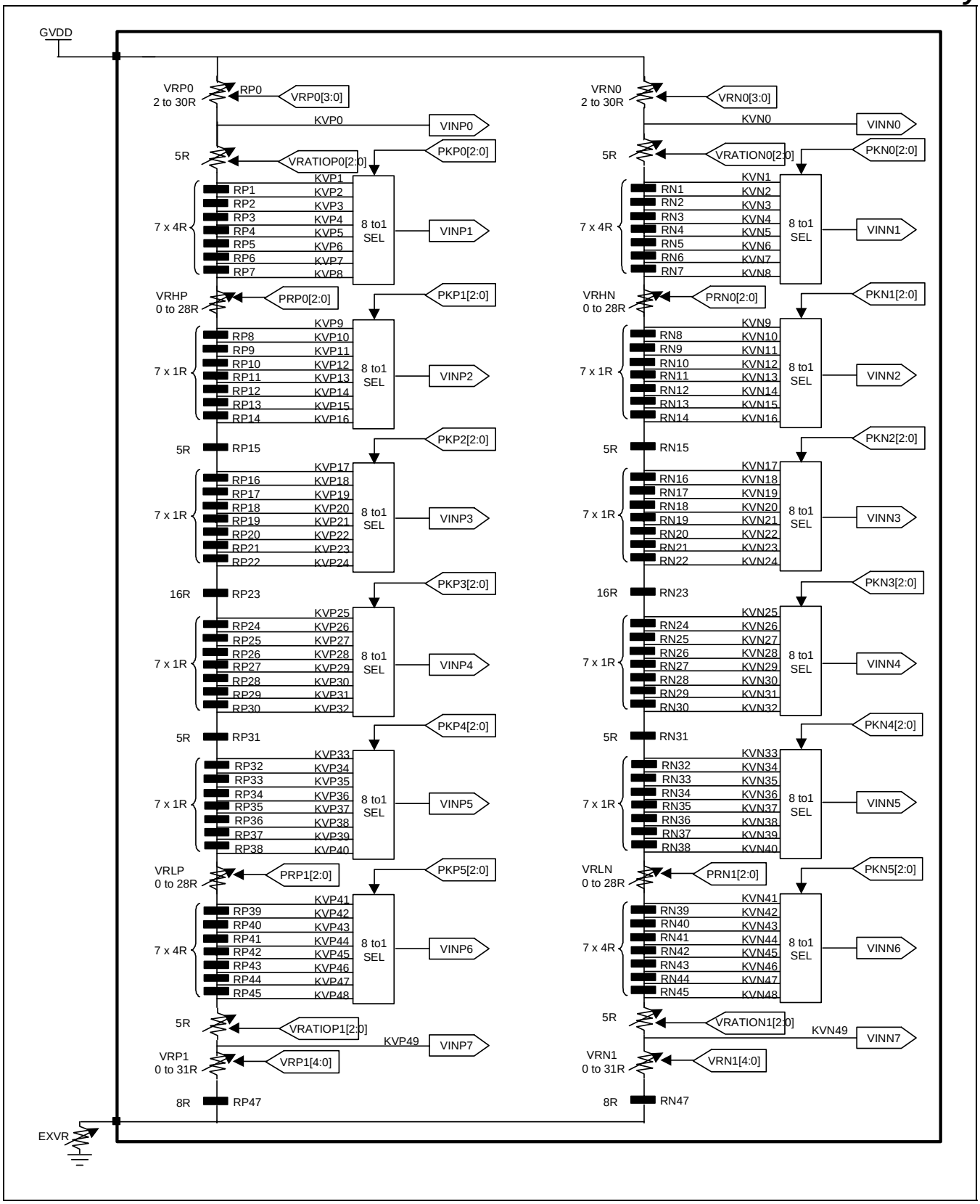

Figure 111. Structure of Ladder / 8 to 1 selector

Preliminary

GAMMA ADJUSTMENT REGISTER

This block has the register to set up the grayscale voltage according to the gamma specification of the LCD panel. These registers can be independently set up to positive/negative polarities and there are 4 types of register groups to adjust gradient and amplitude on number of the grayscale, characteristics of the grayscale voltage. (Average <R><G><B> are common.) The following figure indicates the operation of each adjusting register.

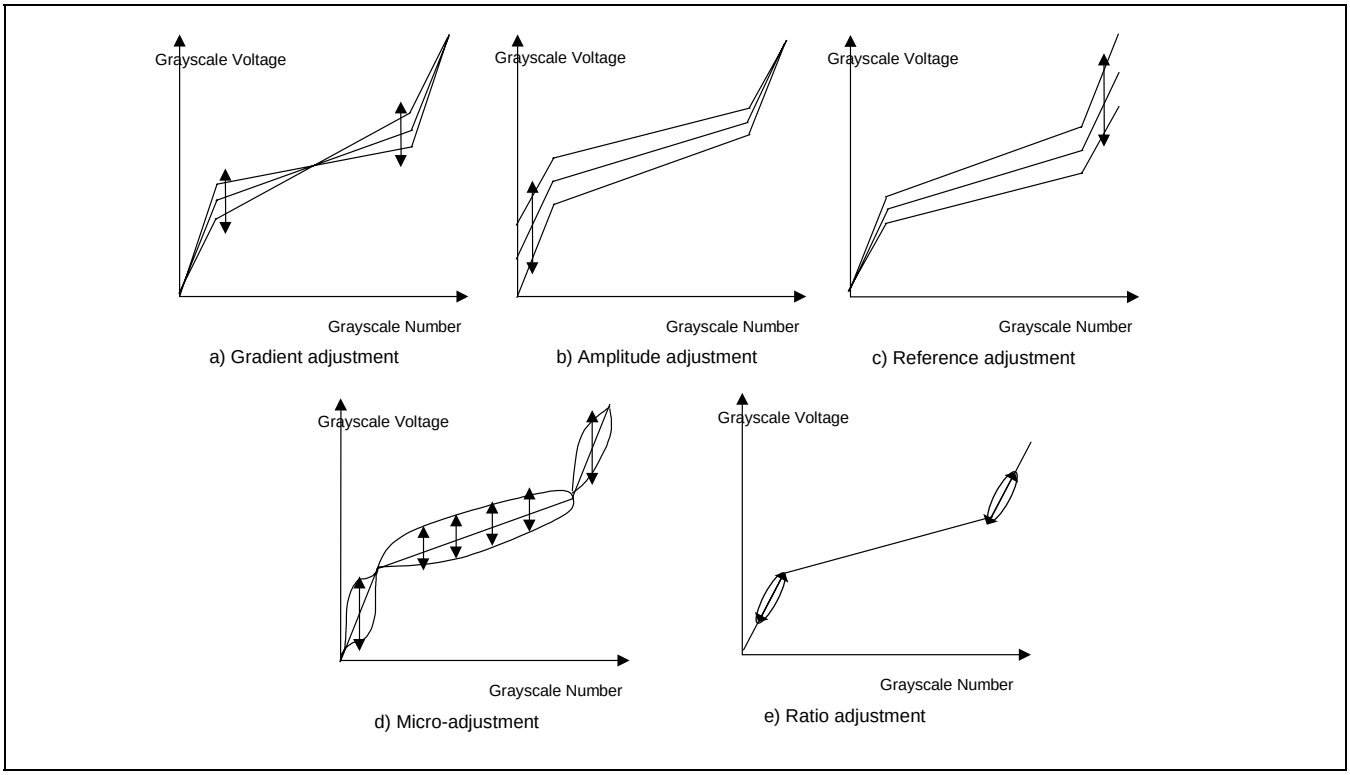

Figure 112. The operation of adjusting register

a) Gradient adjustment resistor

The gradient adjustment resistors are used to adjust the gradient in the middle of the grayscale characteristics for the voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistor (VRHP (N) / VRLP (N)) of the ladder resistor for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order to correspond to asymmetry drive.

b) Amplitude adjustment resistor

The amplitude-adjusting resistor is used to adjust the amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistor (VRP (N)) of the ladder resistor for the grayscale voltage generator located at lower side of the ladder resistor. (Adjust upper side by input GVDD level.) Also, there is an independent resistor on the positive/negative polarities as well as the gradient-adjusting resistor.

c) Reference adjustment resistor

The Reference-adjusting resistor is used to adjust the reference of the grayscale voltage. To accomplish the adjustment, it controls the variable resistor (VRP(N)0) of the ladder resistor for the grayscale voltage generator located at upper side of the ladder resistor.

d) Micro adjustment resistor

The micro adjustment resistor is used to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls each reference voltage level by the 8 to 1 selector towards the 8-leveled reference voltage generated from the ladder resistor. There is also an independent resistor on the positive/negative polarities as well as other adjusting resistors.

e) Ratio adjustment resistor

The ratio adjustment resistor is used to manipulate the value of grayscale voltage levels 1 and 62 respectively. To accomplish the adjustment, it controls the variable resistor (VRATIOP(N)0/1) of the ladder resistor for the grayscale voltage generator.

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Table 36. Gamma correction registers

Register	Positive polarity	Negative polarity	Set-up contents
Gradient adjustment	PRP0[2:0]	PRN0[2:0]	Variable resistor VRHP(N)
	PRP1[2:0]	PRN1[2:0]	Variable resistor VRLP(N)
Amplitude adjustment	VRP1[4:0]	VRN1[4:0]	Variable resistor VRP(N)1
Reference adjustment	VRP0[3:0]	VRN0[3:0]	Variable resistor VRP(N)0
Ratio adjustment	VRATIOP0[2:0]	VRATION0[2:0]	Variable resistor VRATIOP(N)0
Ratio adjustment	VRATIOP1[2:0]	VRATION1[2:0]	Variable resistor VRATIOP(N)1
Micro-adjustment	PKP0[2:0]	PKN0[2:0]	The voltage of grayscale number 1 is selected by the 8 to 1 selector
	PKP1[2:0]	PKN1[2:0]	The voltage of grayscale number 8 is selected by the 8 to 1 selector
	PKP2[2:0]	PKN2[2:0]	The voltage of grayscale number 20 is selected by the 8 to 1 selector
	PKP3[2:0]	PKN3[2:0]	The voltage of grayscale number 43 is selected by the 8 to 1 selector
	PKP4[2:0]	PKN4[2:0]	The voltage of grayscale number 55 is selected by the 8 to 1 selector
	PKP5[2:0]	PKN5[2:0]	The voltage of grayscale number 62 is selected by the 8 to 1 selector

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LADDER RESISTOR/8 TO 1 SELECTOR

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector which selects the voltage generated by the ladder resistance voltage. The variable resistors and 8 to 1 resistors are controlled by the gamma resistor. Also, there are pins that connect to the external volume resistor. In addition, it allows compensating the dispersion of length from one panel to another.

VARIABLE RESISTOR

There are 2 types of the variable resistors, of which one is used for the gradient adjustment (VRHP (N) / VRLP (N)) and the other for the amplitude adjustment (VRP (N)). The resistance value is set by the gradient adjusting resistor and the amplitude adjustment resistor as shown below.

Table 37. Clock Gradient Adjustment (1)

Register value PRP(N)0 [2:0]	Resistance value VRHP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 38. Gradient Adjustment (2)

Register value PRP(N)1 [2:0]	Resistance value VRLP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 39. Amplitude Adjustment (1)

Register value VRP(N)0 [3:0]	Resistance value VRP(N)0
0000	0R
0001	2R
0010	4R
. . .	. . .
1101	26R
1110	28R
1111	30R

Table 40. Amplitude Adjustment (2)

Register value VRP(N)1[4:0]	Resistance value VRP(N)1
00000	0R
00001	1R
00010	2R
. . .	. . .
11101	29R
11110	30R
11111	31R

Table 41. Ratio Adjustment (1)

Register value VRATIOP(N)0[2:0]	Resistance value VRATIOP(N)0
001	1R
010	2R
011	3R
100	4R
101	5R

Table 42. Ratio Adjustment (2)

Register value VRATIOP(N)1[2:0]	Resistance value VRATIOP(N)1
001	1R
010	2R
011	3R
100	4R
101	5R

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THE 8 TO 1 SELECTOR

In the 8 to 1 selector, the voltage level must be selected given by the ladder resistance and the micro-adjusting register. The output voltage is given by the six types of the reference voltage, the VIN1 to VIN6.
Following figure explains the relationship between the micro-adjusting register and the selecting voltage.

Table 41. Relationship between Micro-adjustment Register and Selected Voltage

Register value PKP(N) [2:0]	Selected voltage					
	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
000	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
001	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
010	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
011	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
100	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
101	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
110	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
111	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

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Table 42. Gamma Adjusting Voltage Formula (Positive polarity) 1

Pins	Formula	Micro-adjusting register value	Reference voltage
KVP0	GVDD-ΔV*VRP0/SUMRP	-	VINP0
KVP1	GVDD-ΔV*(VRP0+VRATIOP0)/SUMRP	PKP0[2:0] = “000”	VINP1
KVP2	GVDD-ΔV*(VRP0+ VRATIOP0 +4R)/SUMRP	PKP0[2:0] = “001”	
KVP3	GVDD-ΔV*(VRP0+ VRATIOP0 +8R)/SUMRP	PKP0[2:0] = “010”	
KVP4	GVDD-ΔV*(VRP0+ VRATIOP0 +12R)/SUMRP	PKP0[2:0] = “011”	
KVP5	GVDD-ΔV*(VRP0+ VRATIOP0 +16R)/SUMRP	PKP0[2:0] = “100”	
KVP6	GVDD-ΔV*(VRP0+ VRATIOP0 + 20R)/SUMRP	PKP0[2:0] = “101”	
KVP7	GVDD-ΔV*(VRP0+ VRATIOP0 +24R)/SUMRP	PKP0[2:0] = “110”	
KVP8	GVDD-ΔV*(VRP0+ VRATIOP0 +28R)/SUMRP	PKP0[2:0] = “111”	
KVP9	GVDD-ΔV*(VRP0+ VRATIOP0 +28R+VRHP)/SUMRP	PKP1[2:0] = “000”	VINP2
KVP10	GVDD-ΔV*(VRP0+ VRATIOP0 +29R +VRHP)/SUMRP	PKP1[2:0] = “001”	
KVP11	GVDD-ΔV*(VRP0+ VRATIOP0 +30R +VRHP)/SUMRP	PKP1[2:0] = “010”	
KVP12	GVDD-ΔV*(VRP0+ VRATIOP0 +31R +VRHP)/SUMRP	PKP1[2:0] = “011”	
KVP13	GVDD-ΔV*(VRP0+ VRATIOP0 +32R +VRHP)/SUMRP	PKP1[2:0] = “100”	
KVP14	GVDD-ΔV*(VRP0+ VRATIOP0 +33R +VRHP)/SUMRP	PKP1[2:0] = “101”	
KVP15	GVDD-ΔV*(VRP0+ VRATIOP0 +34R +VRHP)/SUMRP	PKP1[2:0] = “110”	
KVP16	GVDD-ΔV*(VRP0+ VRATIOP0 +35R +VRHP)/SUMRP	PKP1[2:0] = “111”	
KVP17	GVDD-ΔV*(VRP0+ VRATIOP0 +40R +VRHP)/SUMRP	PKP2[2:0] = “000”	VINP3
KVP18	GVDD-ΔV*(VRP0+ VRATIOP0 +41R +VRHP)/SUMRP	PKP2[2:0] = “001”	
KVP19	GVDD-ΔV*(VRP0+ VRATIOP0 +42R +VRHP)/SUMRP	PKP2[2:0] = “010”	
KVP20	GVDD-ΔV*(VRP0+ VRATIOP0 +43R +VRHP)/SUMRP	PKP2[2:0] = “011”	
KVP21	GVDD-ΔV*(VRP0+ VRATIOP0 +44R +VRHP)/SUMRP	PKP2[2:0] = “100”	
KVP22	GVDD-ΔV*(VRP0+ VRATIOP0 +45R +VRHP)/SUMRP	PKP2[2:0] = “101”	
KVP23	GVDD-ΔV*(VRP0+ VRATIOP0 +46R +VRHP)/SUMRP	PKP2[2:0] = “110”	
KVP24	GVDD-ΔV*(VRP0+ VRATIOP0 +47R +VRHP)/SUMRP	PKP2[2:0] = “111”	
KVP25	GVDD-ΔV*(VRP0+ VRATIOP0 +63R +VRHP)/SUMRP	PKP3[2:0] = “000”	VINP4
KVP26	GVDD-ΔV*(VRP0+ VRATIOP0 +64R +VRHP)/SUMRP	PKP3[2:0] = “001”	
KVP27	GVDD-ΔV*(VRP0+ VRATIOP0 +65R +VRHP)/SUMRP	PKP3[2:0] = “010”	
KVP28	GVDD-ΔV*(VRP0+ VRATIOP0 +66R +VRHP)/SUMRP	PKP3[2:0] = “011”	
KVP29	GVDD-ΔV*(VRP0+ VRATIOP0 +67R +VRHP)/SUMRP	PKP3[2:0] = “100”	
KVP30	GVDD-ΔV*(VRP0+ VRATIOP0 +68R +VRHP)/SUMRP	PKP3[2:0] = “101”	
KVP31	GVDD-ΔV*(VRP0+ VRATIOP0 +69R +VRHP)/SUMRP	PKP3[2:0] = “110”	
KVP32	GVDD-ΔV*(VRP0+ VRATIOP0 +70R +VRHP)/SUMRP	PKP3[2:0] = “111”	
KVP33	GVDD-ΔV*(VRP0+ VRATIOP0 +75R +VRHP)/SUMRP	PKP4[2:0] = “000”	VINP5
KVP34	GVDD-ΔV*(VRP0+ VRATIOP0 +76R +VRHP)/SUMRP	PKP4[2:0] = “001”	
KVP35	GVDD-ΔV*(VRP0+ VRATIOP0 +77R +VRHP)/SUMRP	PKP4[2:0] = “010”	
KVP36	GVDD-ΔV*(VRP0+ VRATIOP0 +78R +VRHP)/SUMRP	PKP4[2:0] = “011”	
KVP37	GVDD-ΔV*(VRP0+ VRATIOP0 +79R +VRHP)/SUMRP	PKP4[2:0] = “100”	
KVP38	GVDD-ΔV*(VRP0+ VRATIOP0 +80R +VRHP)/SUMRP	PKP4[2:0] = “101”	
KVP39	GVDD-ΔV*(VRP0+ VRATIOP0 +81R +VRHP)/SUMRP	PKP4[2:0] = “110”	
KVP40	GVDD-ΔV*(VRP0+ VRATIOP0 +82R +VRHP)/SUMRP	PKP4[2:0] = “111”	
KVP41	GVDD-ΔV*(VRP0+ VRATIOP0 +82R +VRHP+VRLP)/SUMRP	PKP5[2:0] = “000”	VINP6
KVP42	GVDD-ΔV*(VRP0+ VRATIOP0 +86R +VRHP+VRLP)/SUMRP	PKP5[2:0] = “001”	
KVP43	GVDD-ΔV*(VRP0+ VRATIOP0 +90R +VRHP+VRLP)/SUMRP	PKP5[2:0] = “010”	
KVP44	GVDD-ΔV*(VRP0+ VRATIOP0 +94R +VRHP+VRLP)/SUMRP	PKP5[2:0] = “011”	
KVP45	GVDD-ΔV*(VRP0+ VRATIOP0 +98R +VRHP+VRLP)/SUMRP	PKP5[2:0] = “100”	
KVP46	GVDD-ΔV*(VRP0+ VRATIOP0 +102R +VRHP+VRLP)/SUMRP	PKP5[2:0] = “101”	
KVP47	GVDD-ΔV*(VRP0+ VRATIOP0 +106R +VRHP+VRLP)/SUMRP	PKP5[2:0] = “110”	
KVP48	GVDD-ΔV*(VRP0+ VRATIOP0 +110R +VRHP+VRLP)/SUMRP	PKP5[2:0] = “111”	
KVP49	GVDD-ΔV*(VRP0+ VRATIOP0 + VRATIOP1+110R+VRHP+VRLP)/SUMRP	-	VINP7

SUMRP: Total of the positive polarity ladder resistance = VRP0 + VRATIOP0 + VRATIOP1 + 118R + VRHP + VRLP + VRP1
SUMRN: Total of the negative polarity ladder resistance = VRN0 + VRATION0 + VRATION1 + 118R + VRHN + VRLN + VRN1
ΔV: Electric potential difference between GVDD and VGS = GVDD*[SUMRP(N)/([SUMRP(N)+EXVR])

Table 43. Gamma Voltage Formula (Positive Polarity) 2

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINP0	V32	V20-(V20-V43)*(12/23)
V1	VINP1	V33	V20-(V20-V43)*(13/23)
V2	V1-(V1-V8)*(28/96)	V34	V20-(V20-V43)*(14/23)
V3	V1-(V1-V8)*(42/96)	V35	V20-(V20-V43)*(15/23)
V4	V1-(V1-V8)*(60/96)	V36	V20-(V20-V43)*(16/23)
V5	V1-(V1-V8)*(69/96)	V37	V20-(V20-V43)*(17/23)
V6	V1-(V1-V8)*(78/96)	V38	V20-(V20-V43)*(18/23)
V7	V1-(V1-V8)*(87/96)	V39	V20-(V20-V43)*(19/23)
V8	VINP2	V40	V20-(V20-V43)*(20/23)
V9	V8-(V8-V20)*(2/24)	V41	V20-(V20-V43)*(21/23)
V10	V8-(V8-V20)*(4/24)	V42	V20-(V20-V43)*(22/23)
V11	V8-(V8-V20)*(6/24)	V43	VINP4
V12	V8-(V8-V20)*(8/24)	V44	V43-(V43-V55)*(2/24)
V13	V8-(V8-V20)*(10/24)	V45	V43-(V43-V55)*(4/24)
V14	V8-(V8-V20)*(12/24)	V46	V43-(V43-V55)*(6/24)
V15	V8-(V8-V20)*(14/24)	V47	V43-(V43-V55)*(8/24)
V16	V8-(V8-V20)*(16/24)	V48	V43-(V43-V55)*(10/24)
V17	V8-(V8-V20)*(18/24)	V49	V43-(V43-V55)*(12/24)
V18	V8-(V8-V20)*(20/24)	V50	V43-(V43-V55)*(14/24)
V19	V8-(V8-V20)*(22/24)	V51	V43-(V43-V55)*(16/24)
V20	VINP3	V52	V43-(V43-V55)*(18/24)
V21	V20-(V20-V43)*(1/23)	V53	V43-(V43-V55)*(20/24)
V22	V20-(V20-V43)*(2/23)	V54	V43-(V43-V55)*(22/24)
V23	V20-(V20-V43)*(3/23)	V55	VINP5
V24	V20-(V20-V43)*(4/23)	V56	V55-(V55-V62)*(9/96)
V25	V20-(V20-V43)*(5/23)	V57	V55-(V55-V62)*(18/96)
V26	V20-(V20-V43)*(6/23)	V58	V55-(V55-V62)*(27/96)
V27	V20-(V20-V43)*(7/23)	V59	V55-(V55-V62)*(36/96)
V28	V20-(V20-V43)*(8/23)	V60	V55-(V55-V62)*(54/96)
V29	V20-(V20-V43)*(9/23)	V61	V55-(V55-V62)*(68/96)
V30	V20-(V20-V43)*(10/23)	V62	VINP6
V31	V20-(V20-V43)*(11/23)	V63	VINP7

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Table 44. Gamma Adjusting Voltage Formula (Negative polarity) 1

Pins	Formula	Micro-adjusting register value	Reference voltage
KVN0	GVDD-ΔV*VRN0/SUMRN	-	VINN0
KVN1	GVDD-ΔV*(VRN0+VRATION0)/SUMRN	PKN0[2:0] = “000”	VINN1
KVN2	GVDD-ΔV*(VRN0+VRATION0 +4R)/SUMRN	PKN0[2:0] = “001”	
KVN3	GVDD-ΔV*(VRN0+VRATION0 +8R)/SUMRN	PKN0[2:0] = “010”	
KVN4	GVDD-ΔV*(VRN0+VRATION0 +12R)/SUMRN	PKN0[2:0] = “011”	
KVN5	GVDD-ΔV*(VRN0+VRATION0 +16R)/SUMRN	PKN0[2:0] = “100”	
KVN6	GVDD-ΔV*(VRN0+VRATION0 + 20R)/SUMRN	PKN0[2:0] = “101”	
KVN7	GVDD-ΔV*(VRN0+ VRATION0 + 24R)/SUMRN	PKN0[2:0] = “110”	
KVN8	GVDD-ΔV*(VRN0+ VRATION0 + 28R)/SUMRN	PKN0[2:0] = “111”	
KVN9	GVDD-ΔV*(VRN0+ VRATION0 + 28R +VRHN)/SUMRN	PKN1[2:0] = “000”	VINN2
KVN10	GVDD-ΔV*(VRN0+ VRATION0 + 29R +VRHN)/SUMRN	PKN1[2:0] = “001”	
KVN11	GVDD-ΔV*(VRN0+ VRATION0 + 30R +VRHN)/SUMRN	PKN1[2:0] = “010”	
KVN12	GVDD-ΔV*(VRN0+ VRATION0 + 31R +VRHN)/SUMRN	PKN1[2:0] = “011”	
KVN13	GVDD-ΔV*(VRN0+ VRATION0 + 32R +VRHN)/SUMRN	PKN1[2:0] = “100”	
KVN14	GVDD-ΔV*(VRN0+ VRATION0 + 33R +VRHN)/SUMRN	PKN1[2:0] = “101”	
KVN15	GVDD-ΔV*(VRN0+ VRATION0 + 34R +VRHN)/SUMRN	PKN1[2:0] = “110”	
KVN16	GVDD-ΔV*(VRN0+ VRATION0 + 35R +VRHN)/SUMRN	PKN1[2:0] = “111”	
KVN17	GVDD-ΔV*(VRN0+ VRATION0 + 40R +VRHN)/SUMRN	PKN2[2:0] = “000”	VINN3
KVN18	GVDD-ΔV*(VRN0+ VRATION0 + 41R +VRHN)/SUMRN	PKN2[2:0] = “001”	
KVN19	GVDD-ΔV*(VRN0+ VRATION0 + 42R +VRHN)/SUMRN	PKN2[2:0] = “010”	
KVN20	GVDD-ΔV*(VRN0+ VRATION0 + 43R +VRHN)/SUMRN	PKN2[2:0] = “011”	
KVN21	GVDD-ΔV*(VRN0+ VRATION0 + 44R +VRHN)/SUMRN	PKN2[2:0] = “100”	
KVN22	GVDD-ΔV*(VRN0+ VRATION0 + 45R +VRHN)/SUMRN	PKN2[2:0] = “101”	
KVN23	GVDD-ΔV*(VRN0+ VRATION0 + 46R +VRHN)/SUMRN	PKN2[2:0] = “110”	
KVN24	GVDD-ΔV*(VRN0+ VRATION0 + 47R +VRHN)/SUMRN	PKN2[2:0] = “111”	
KVN25	GVDD-ΔV*(VRN0+ VRATION0 + 63R +VRHN)/SUMRN	PKN3[2:0] = “000”	VINN4
KVN26	GVDD-ΔV*(VRN0+ VRATION0 + 64R +VRHN)/SUMRN	PKN3[2:0] = “001”	
KVN27	GVDD-ΔV*(VRN0+ VRATION0 + 65R +VRHN)/SUMRN	PKN3[2:0] = “010”	
KVN28	GVDD-ΔV*(VRN0+ VRATION0 + 66R +VRHN)/SUMRN	PKN3[2:0] = “011”	
KVN29	GVDD-ΔV*(VRN0+ VRATION0 + 67R +VRHN)/SUMRN	PKN3[2:0] = “100”	
KVN30	GVDD-ΔV*(VRN0+ VRATION0 + 68R +VRHN)/SUMRN	PKN3[2:0] = “101”	
KVN31	GVDD-ΔV*(VRN0+ VRATION0 + 69R +VRHN)/SUMRN	PKN3[2:0] = “110”	
KVN32	GVDD-ΔV*(VRN0+ VRATION0 + 70R +VRHN)/SUMRN	PKN3[2:0] = “111”	
KVN33	GVDD-ΔV*(VRN0+ VRATION0 + 75R +VRHN)/SUMRN	PKN4[2:0] = “000”	VINN5
KVN34	GVDD-ΔV*(VRN0+ VRATION0 + 76R +VRHN)/SUMRN	PKN4[2:0] = “001”	
KVN35	GVDD-ΔV*(VRN0+ VRATION0 + 77R +VRHN)/SUMRN	PKN4[2:0] = “010”	
KVN36	GVDD-ΔV*(VRN0+ VRATION0 + 78R +VRHN)/SUMRN	PKN4[2:0] = “011”	
KVN37	GVDD-ΔV*(VRN0+ VRATION0 + 79R +VRHN)/SUMRN	PKN4[2:0] = “100”	
KVN38	GVDD-ΔV*(VRN0+ VRATION0 + 80R +VRHN)/SUMRN	PKN4[2:0] = “101”	
KVN39	GVDD-ΔV*(VRN0+ VRATION0 + 81R +VRHN)/SUMRN	PKN4[2:0] = “110”	
KVN40	GVDD-ΔV*(VRN0+ VRATION0 + 82R +VRHN)/SUMRN	PKN4[2:0] = “111”	
KVN41	GVDD-ΔV*(VRN0+ VRATION0 + 82R +VRHN+VRLN)/SUMRN	PKN5[2:0] = “000”	VINN6
KVN42	GVDD-ΔV*(VRN0+ VRATION0 + 86R +VRHN+VRLN)/SUMRN	PKN5[2:0] = “001”	
KVN43	GVDD-ΔV*(VRN0+ VRATION0 + 90R +VRHN+VRLN)/SUMRN	PKN5[2:0] = “010”	
KVN44	GVDD-ΔV*(VRN0+ VRATION0 + 94R +VRHN+VRLN)/SUMRN	PKN5[2:0] = “011”	
KVN45	GVDD-ΔV*(VRN0+ VRATION0 + 98R +VRHN+VRLN)/SUMRN	PKN5[2:0] = “100”	
KVN46	GVDD-ΔV*(VRN0+ VRATION0 + 102R +VRHN+VRLN)/SUMRN	PKN5[2:0] = “101”	
KVN47	GVDD-ΔV*(VRN0+ VRATION0 + 106R +VRHN+VRLN)/SUMRN	PKN5[2:0] = “110”	
KVN48	GVDD-ΔV*(VRN0+ VRATION0 + 110R +VRHN+VRLN)/SUMRN	PKN5[2:0] = “111”	
KVN49	GVDD-ΔV*(VRN0+VRATION0+VRATION1+110R+VRHN+VRLN)/SUMRN	-	VINN7

SUMRP: Total of the positive polarity ladder resistance = VRP0 + VRATIOP0 + VRATIOP1 + 118R + VRHP + VRLP + VRP1
SUMRN: Total of the negative polarity ladder resistance = VRN0 + VRATION0 + VRATION1 + 118R + VRHN + VRLN + VRN1
ΔV: Electric potential difference between GVDD and VGS = GVDD*[SUMRP(N)/([SUMRP(N)+EXVR)]

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Table 45. Gamma Voltage Formula (Negative Polarity) 2

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINN0	V32	V20-(V20-V43)*(12/23)
V1	VINN1	V33	V20-(V20-V43)*(13/23)
V2	V1-(V1-V8)*(28/96)	V34	V20-(V20-V43)*(14/23)
V3	V1-(V1-V8)*(42/96)	V35	V20-(V20-V43)*(15/23)
V4	V1-(V1-V8)*(60/96)	V36	V20-(V20-V43)*(16/23)
V5	V1-(V1-V8)*(69/96)	V37	V20-(V20-V43)*(17/23)
V6	V1-(V1-V8)*(78/96)	V38	V20-(V20-V43)*(18/23)
V7	V1-(V1-V8)*(87/96)	V39	V20-(V20-V43)*(19/23)
V8	VINN2	V40	V20-(V20-V43)*(20/23)
V9	V8-(V8-V20)*(2/24)	V41	V20-(V20-V43)*(21/23)
V10	V8-(V8-V20)*(4/24)	V42	V20-(V20-V43)*(22/23)
V11	V8-(V8-V20)*(6/24)	V43	VINN4
V12	V8-(V8-V20)*(8/24)	V44	V43-(V43-V55)*(2/24)
V13	V8-(V8-V20)*(10/24)	V45	V43-(V43-V55)*(4/24)
V14	V8-(V8-V20)*(12/24)	V46	V43-(V43-V55)*(6/24)
V15	V8-(V8-V20)*(14/24)	V47	V43-(V43-V55)*(8/24)
V16	V8-(V8-V20)*(16/24)	V48	V43-(V43-V55)*(10/24)
V17	V8-(V8-V20)*(18/24)	V49	V43-(V43-V55)*(12/24)
V18	V8-(V8-V20)*(20/24)	V50	V43-(V43-V55)*(14/24)
V19	V8-(V8-V20)*(22/24)	V51	V43-(V43-V55)*(16/24)
V20	VINN3	V52	V43-(V43-V55)*(18/24)
V21	V20-(V20-V43)*(1/23)	V53	V43-(V43-V55)*(20/24)
V22	V20-(V20-V43)*(2/23)	V54	V43-(V43-V55)*(22/24)
V23	V20-(V20-V43)*(3/23)	V55	VINN5
V24	V20-(V20-V43)*(4/23)	V56	V55-(V55-V62)*(9/96)
V25	V20-(V20-V43)*(5/23)	V57	V55-(V55-V62)*(18/96)
V26	V20-(V20-V43)*(6/23)	V58	V55-(V55-V62)*(27/96)
V27	V20-(V20-V43)*(7/23)	V59	V55-(V55-V62)*(36/96)
V28	V20-(V20-V43)*(8/23)	V60	V55-(V55-V62)*(54/96)
V29	V20-(V20-V43)*(9/23)	V61	V55-(V55-V62)*(68/96)
V30	V20-(V20-V43)*(10/23)	V62	VINN6
V31	V20-(V20-V43)*(11/23)	V63	VINN7

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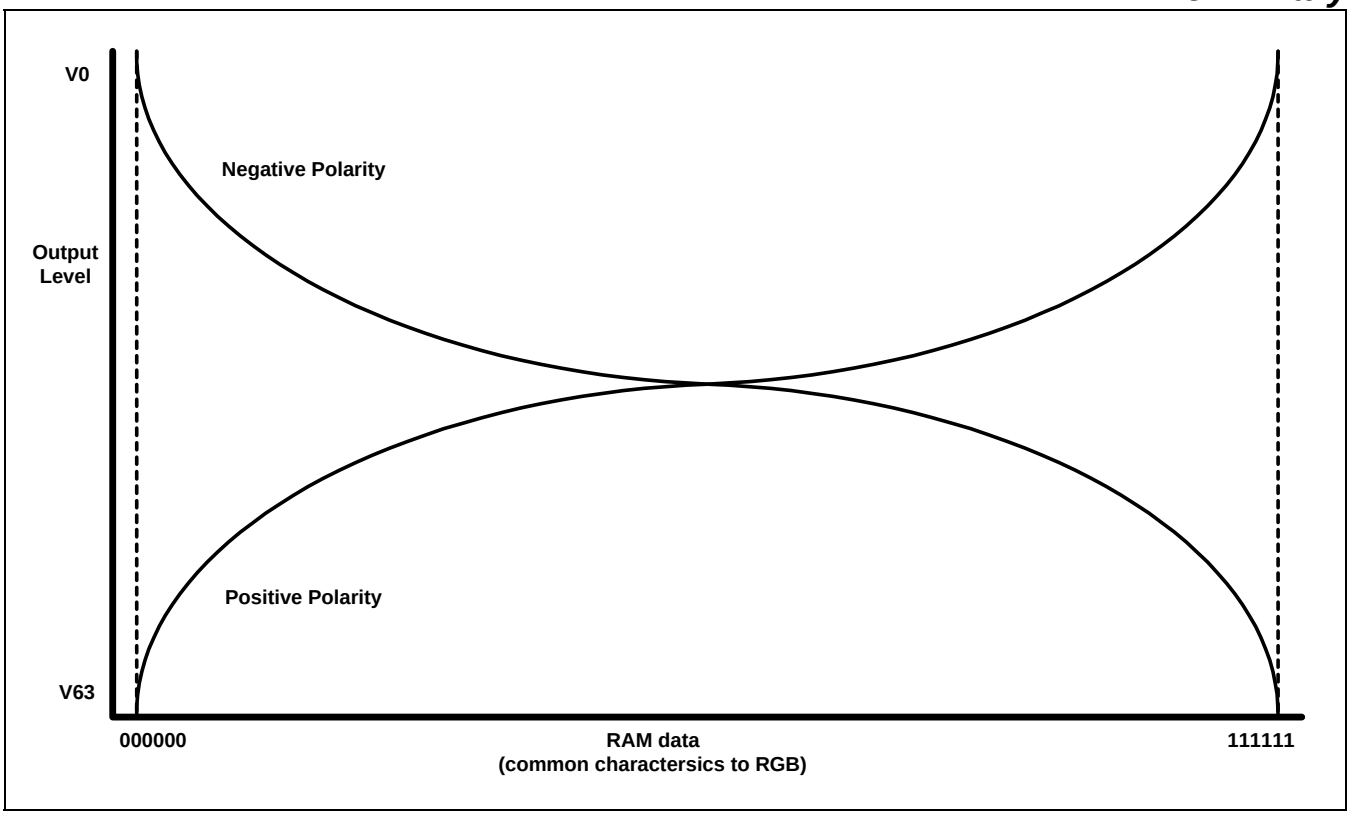

Figure 113. Relationship between RAM data and output voltage

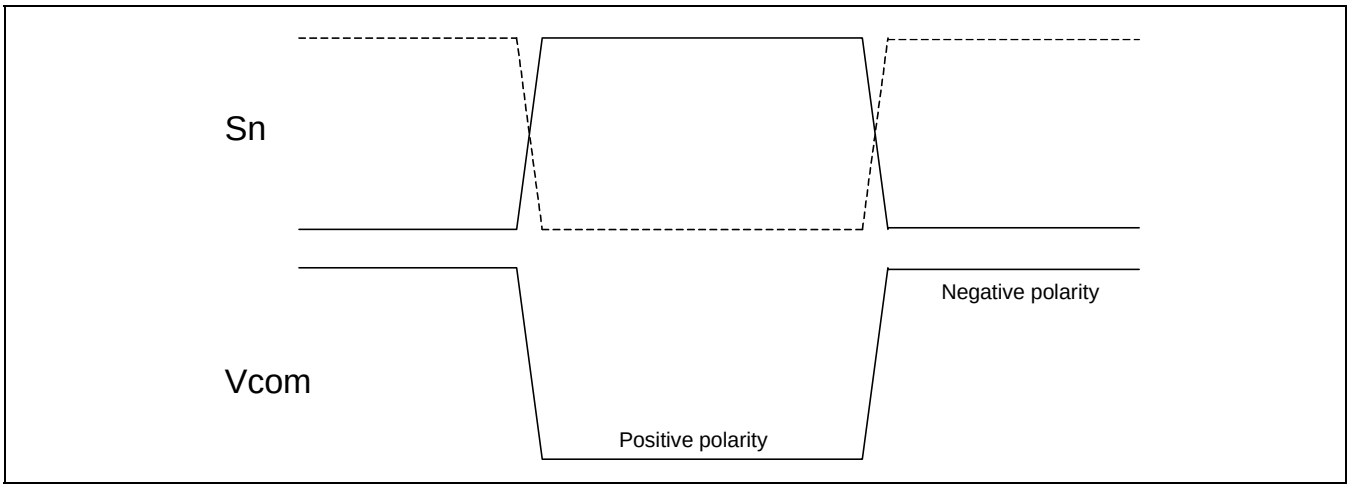

Figure 114. Relationship between source output and Vcom

Preliminary

THE 8-COLOR DISPLAY MODE

The S6D0139 incorporates 8-color display mode. The used grayscale levels are V0 and V63 and all the other levels (V1~V62) are halted, so that the power consumption is lowered.
During the 8-color mode, the Gamma micro adjustment register, PKP00-PKP52 and PKN00-PKN52 are invalid. The level power supply (V1-V62) is in OFF condition during the 8-color mode in order to select V0/V63.

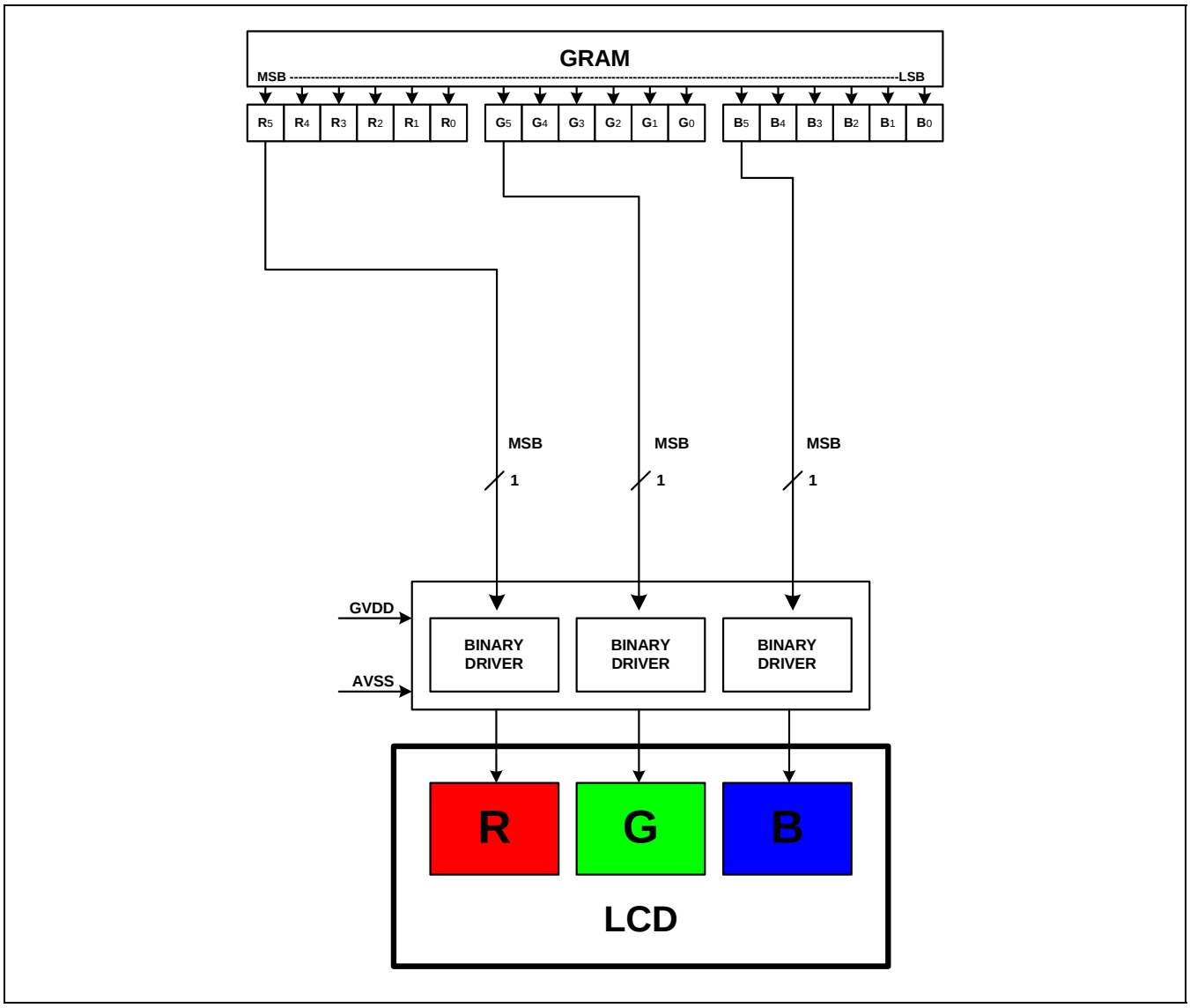

Figure 115. 8-color display control

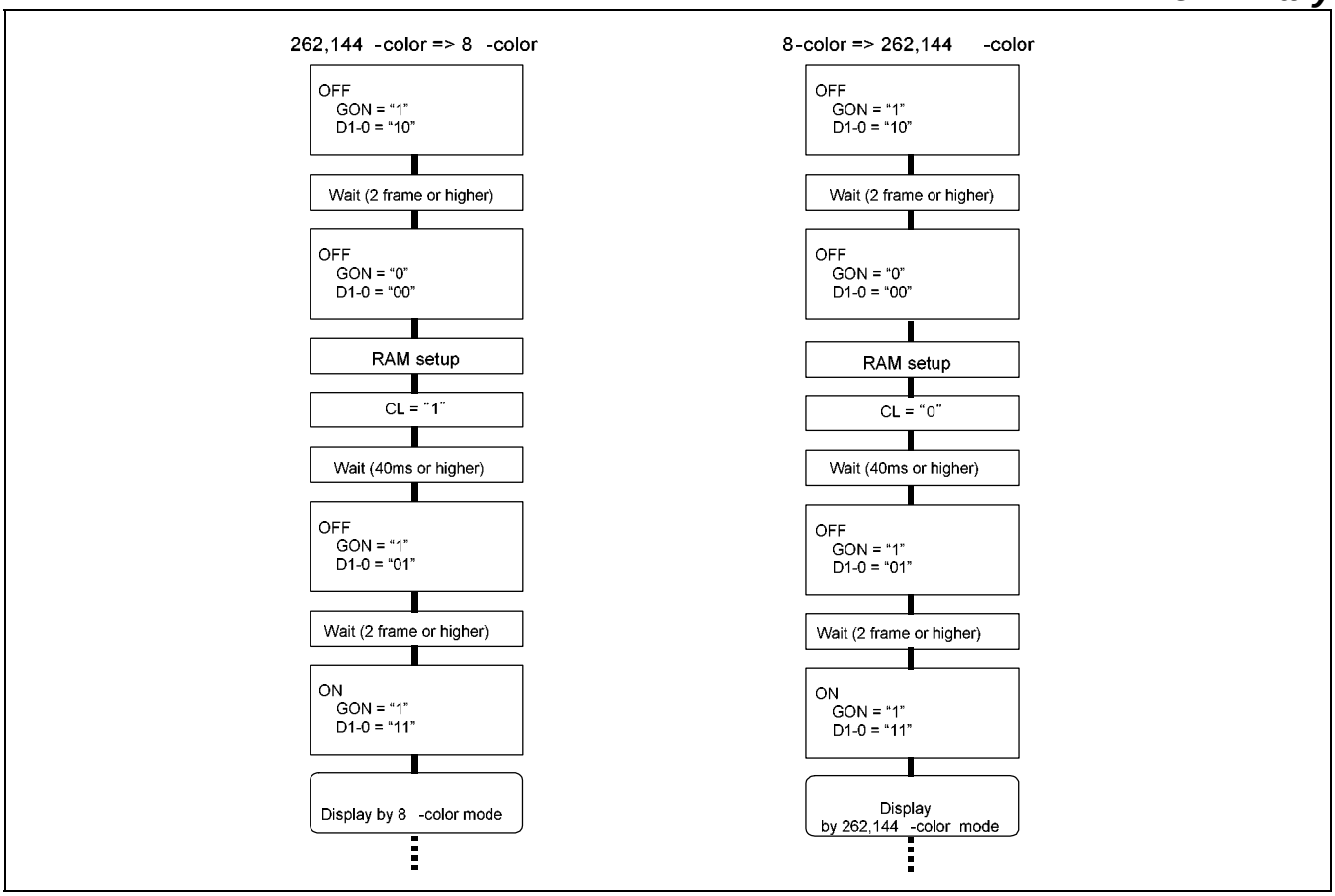

Figure 116. Set up procedure for the 8-color mode

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SYSTEM STRUCTURE EXAMPLE

The following figure indicates the system structure, which composes the 240 (width) x 320 (length) dots TFT-LCD panel.

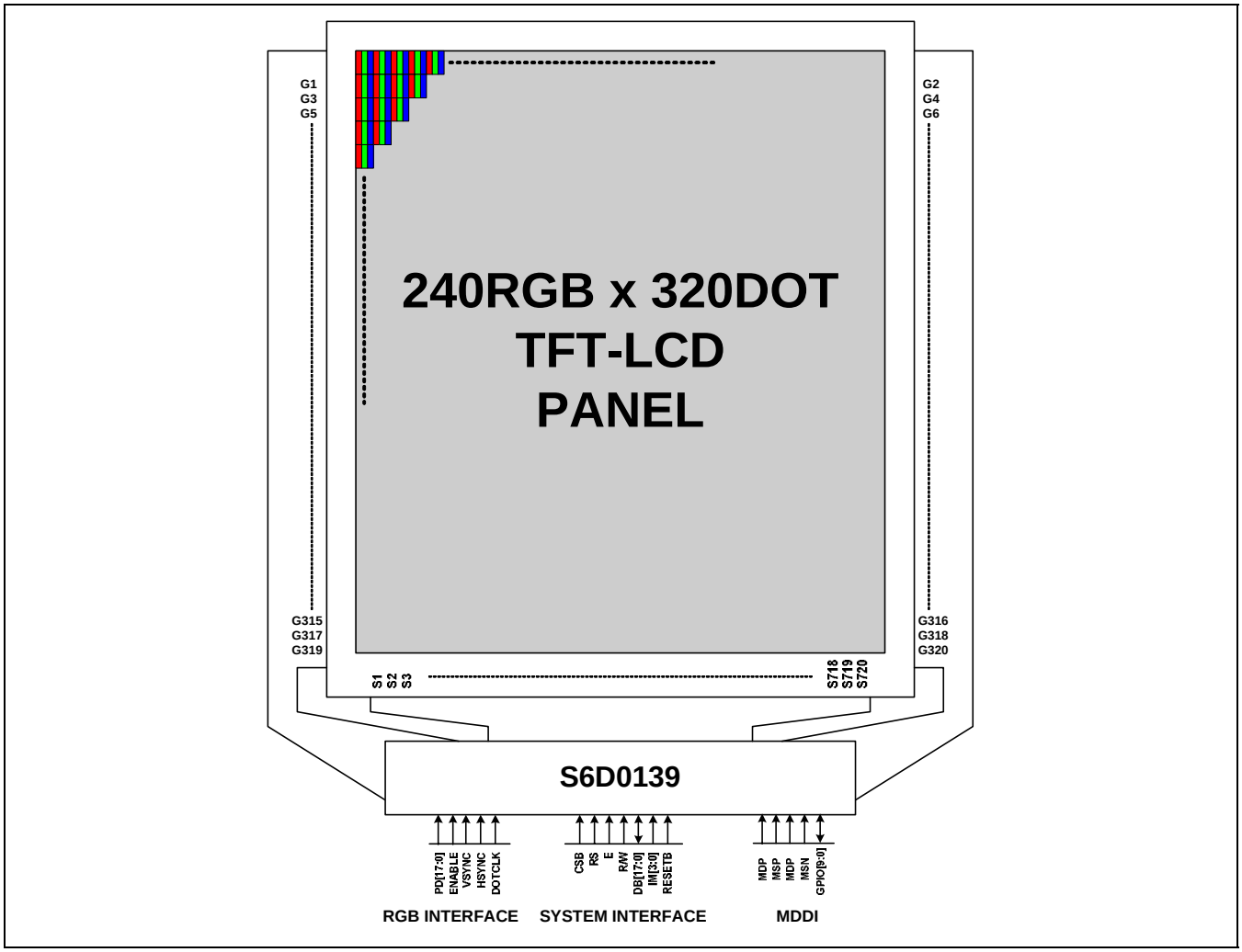

Figure 117. System structure(Panel : Top View, Drive IC : Top View)

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INSTRUCTION SET UP FLOW

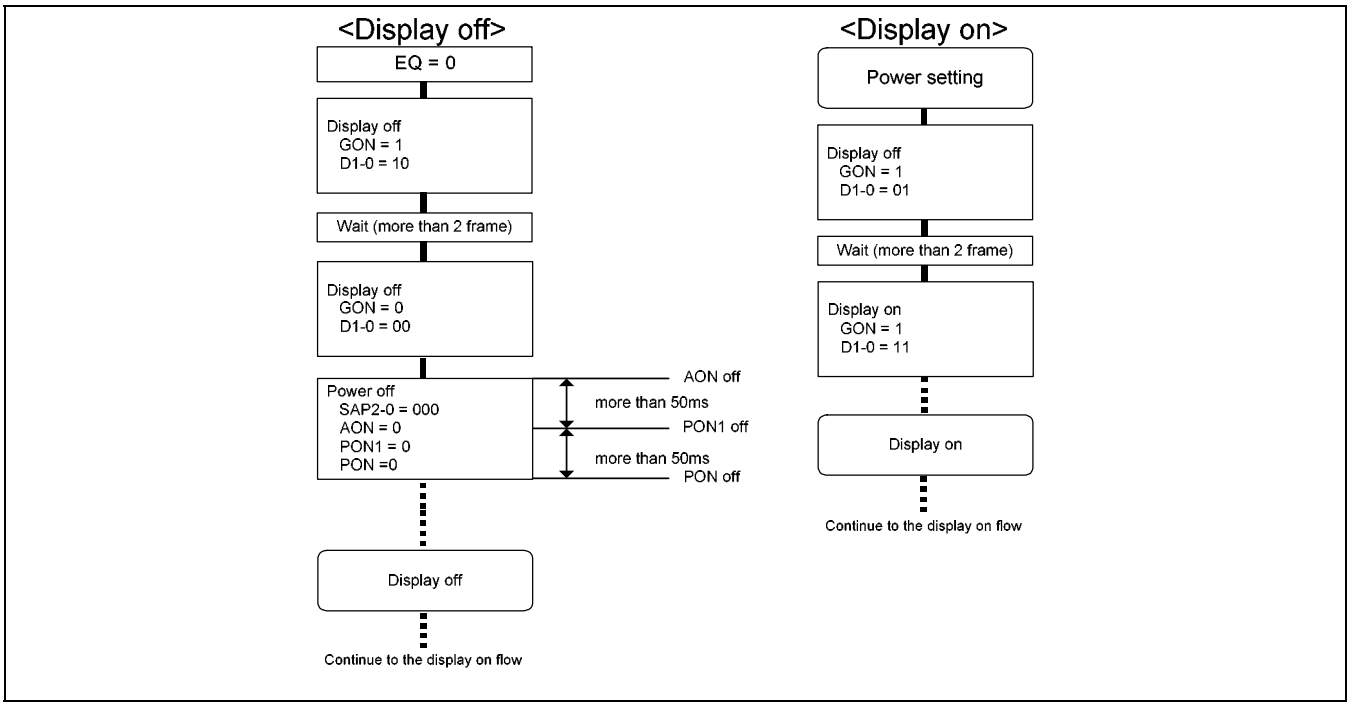

Figure 118. Instruction set up flow

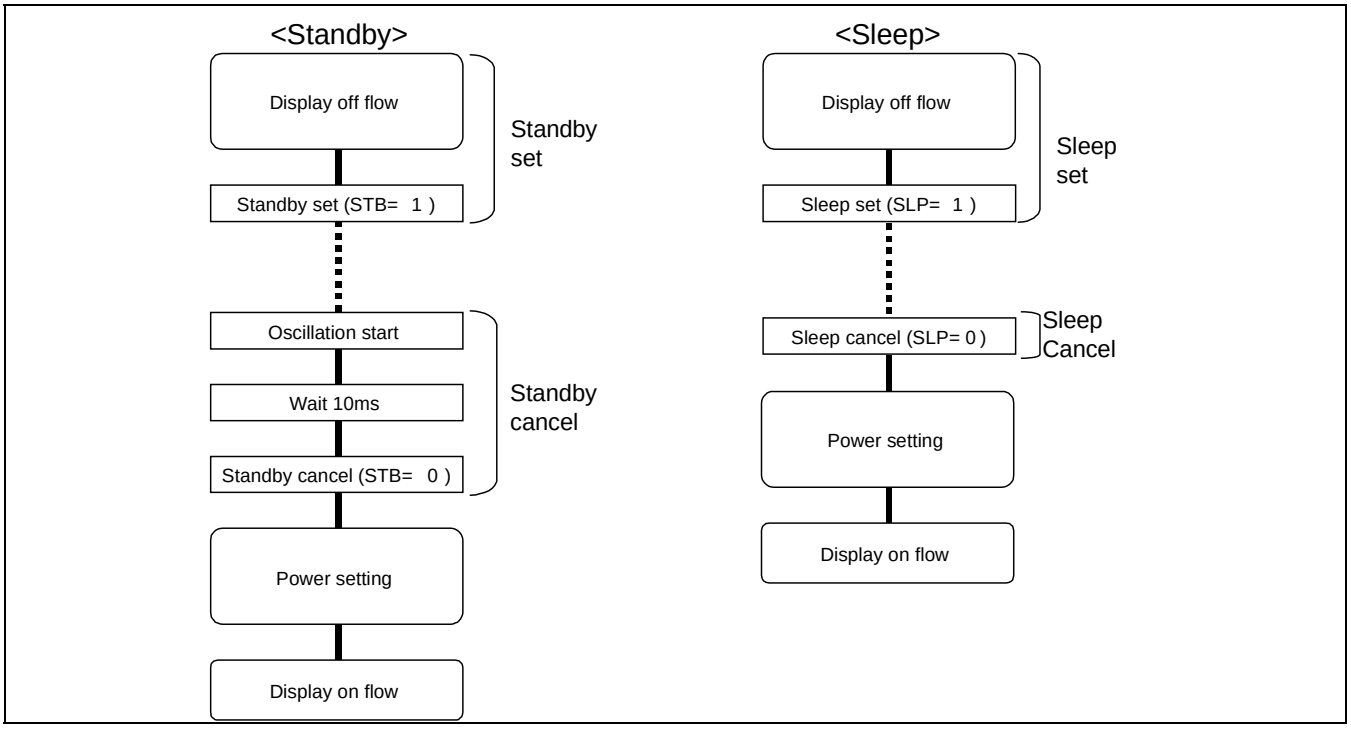

Figure 119. Instruction setup flow (continued)

Preliminary

OSCILLATION CIRCUIT

The S6D0139 can oscillate between the OSC1 and OSC2 pins using an internal R-C oscillator with an external oscillation resistor. Note that in R-C oscillation, the oscillation frequency is changed according to the external resistance value, wiring length, or operating power-supply voltage. If Rf is increased or power supply voltage is decreased, the oscillation frequency will decrease. For the relationship between Rf resistor value and oscillation frequency, see the Electric Characteristics Notes section.

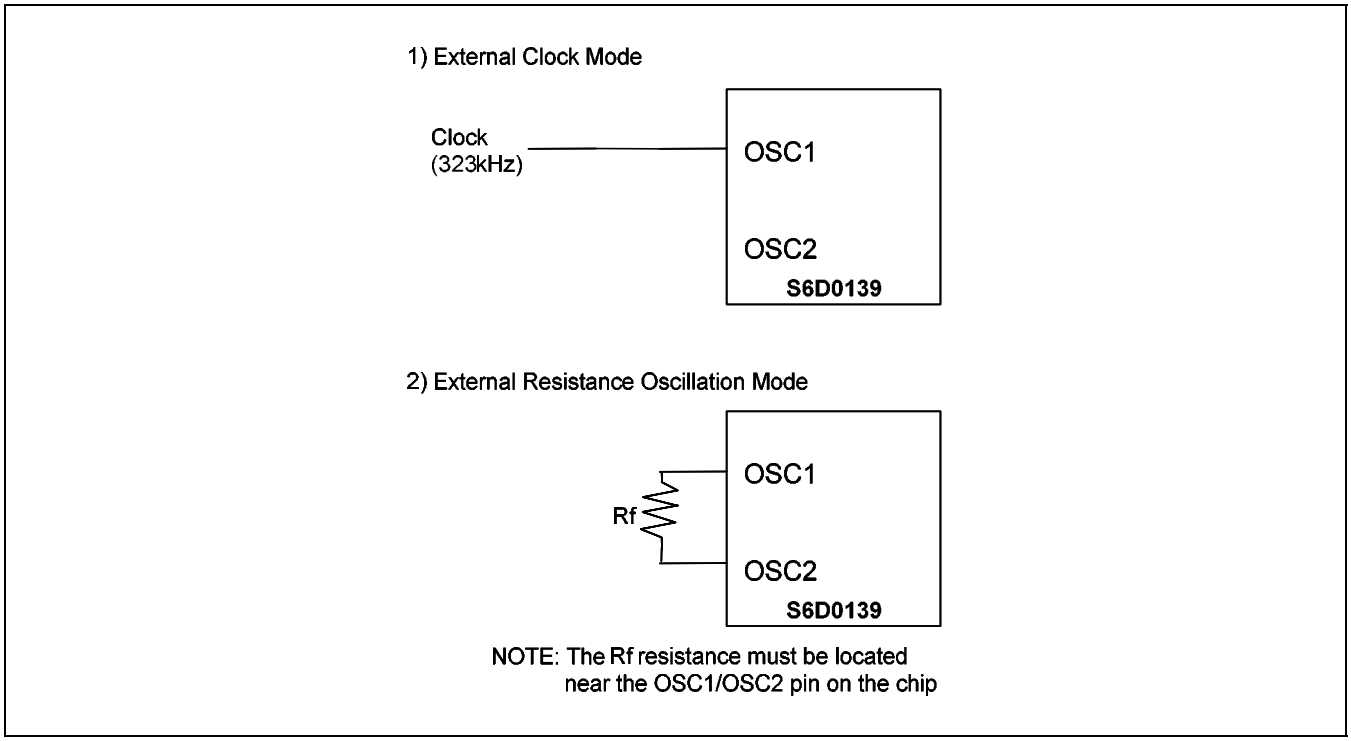

Figure 120. Oscillation Circuit

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N-RASTER-ROW REVERSED AC DRIVE

The S6D0139 supports not only the LCD reversed AC drive in a one-frame unit but also the one-raster-row reversed AC drive which alternates in a one-raster-row unit. When a problem affecting display quality occurs, the one-raster-row reversed AC drive can improve the quality.

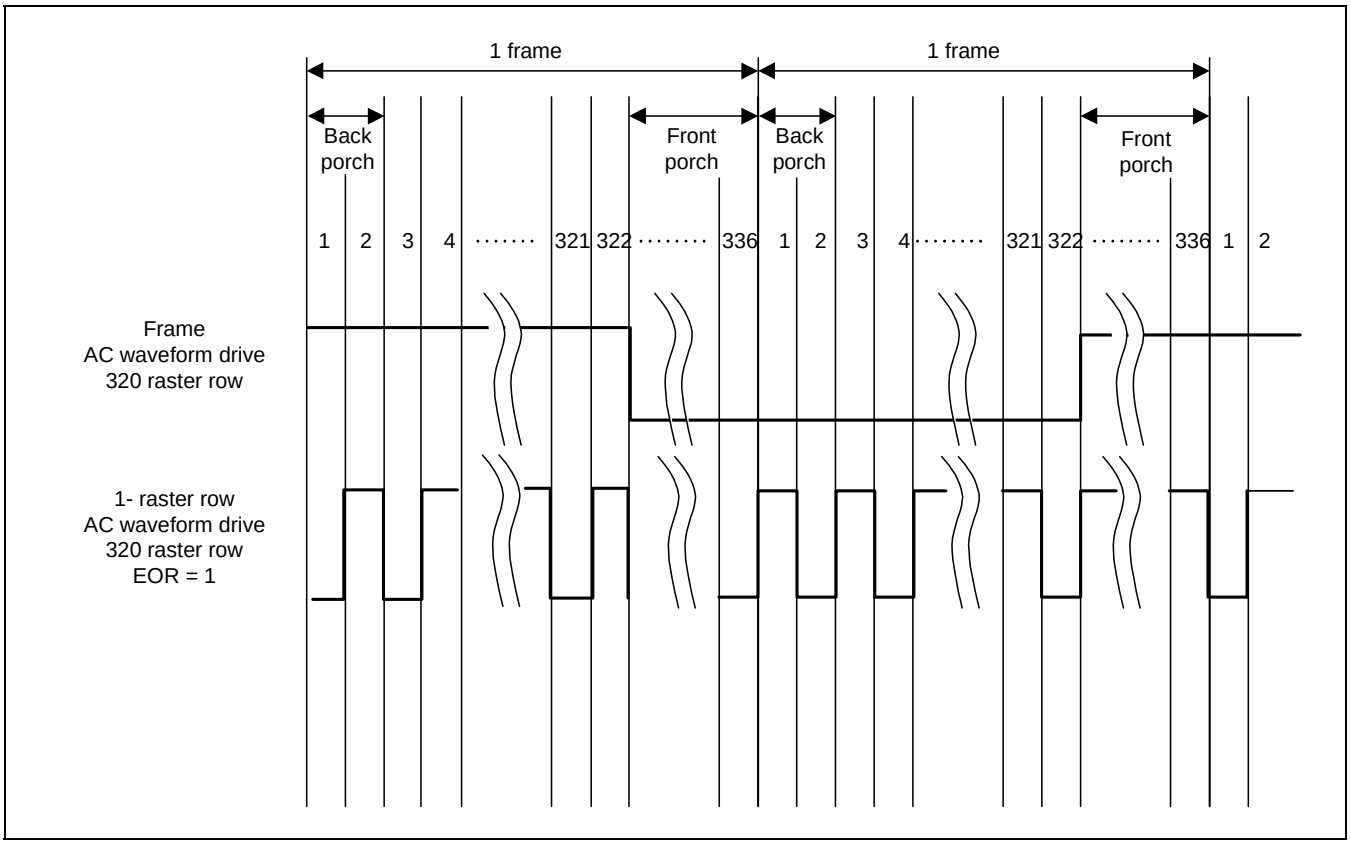

Figure 121. Example of an AC signal under one-raster-row reversed AC drive (BP=2, FP=14)

SAMSUNG ELECTRONICS

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INTERLACE DRIVE

S6D0139 supports the interlace drive to protect from the flicker. It splits one frame into n fields and drives. Determine the n fields (FLD bit stetting value) after confirming on the actual LCD display.
Following table indicates n fields: the gate selecting position when it is 1 or 3. The diagram below indicates the output waveform when the fields interlace drive is active.

GS = "0"

FLD1-0 :setting value	01	11		
Gate \ Field	-	(1)	(2)	(3)
G1	O	O		
G2	O		O	
G3	O			O
G4	O	O		
G5	O		O	
G6	O			O
G7	O	O		
G8	O		O	
G9	O			O
G317	O		O	
G318	O			O
G319	O	O		
G320	O		O	

GS = "1"

FLD1-0 :setting value	01	11		
Gate \ Field	-	(1)	(2)	(3)
G320	O	O		
G319	O		O	
G318	O			O
G317	O	O		
G316	O		O	
G315	O			O
G314	O	O		
G313	O		O	
G312	O			O
G4	O		O	
G3	O			O
G2	O	O		
G1	O		O	

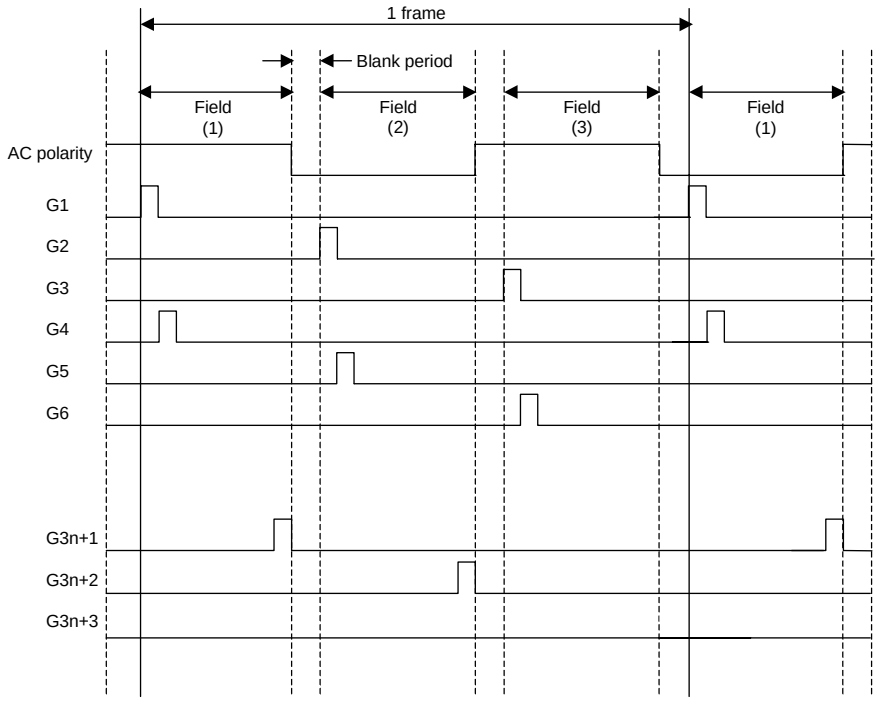

Figure 122. Interlace drive and output waveform

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A/C TIMING

Following diagram indicates the A/C timing on each A/C drive method. After every drawing, the A/C timing occurs on the reversed frame AC drive. After the A/C timing, the blank (all gate output: VGL level) period described below is inserted. When it is on the interlace drive, blank period is inserted every A/C timing. When the reversed n-raster-row is driving, a blank period is inserted after all screens are drawn. Front and Back porch can be adjusted using FP3-0 and BP3-0 bits (R08h).

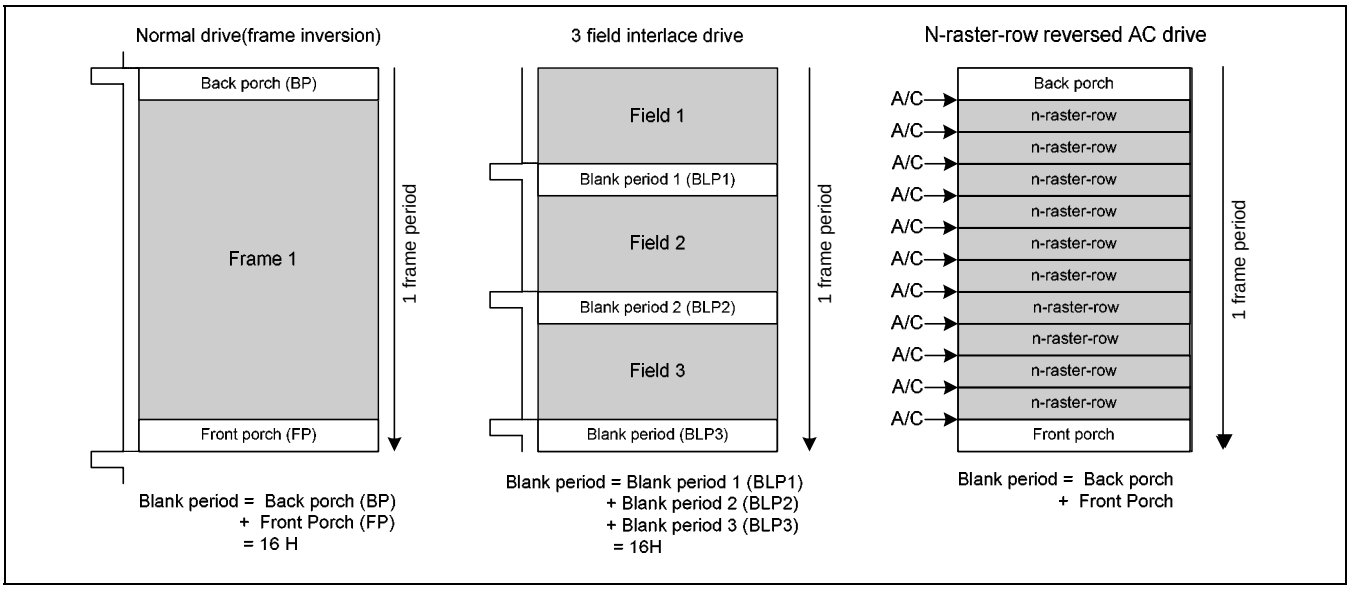

Figure 123. A/C timing

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FRAME FREQUENCY ADJUSTING FUNCTION

The S6D0139 has an on-chip frame-frequency adjustment function. The frame frequency can be adjusted by the instruction setting (DIV, RTN) during the LCD driver as the oscillation frequency is always same.
If the oscillation frequency is set to high, animation or a static image can be displayed in suitable ways by changing the frame frequency. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching for an animated display, etc. is required, the frame frequency can be set high.

RELATIONSHIP BETWEEN LCD DRIVE DUTY AND FRAME FREQUENCY

The relationships between the LCD drive duty and the frame frequency is calculated by the following expression. The frame frequency can be adjusted in the 1H period adjusting bit (RTN) and in the operation clock division bit (DIV) by the instruction.

$$\text{Frame Frequency} = \frac{f_{osc}}{\text{Clock cycles per raster-row x division ratio x (Line+B)}} \text{ [Hz]}$$

f_{osc}: R-C oscillation frequency
Line: Number of raster-rows (NL bit)
Clock cycles per raster-row: RTN bit
Division ratio: DIV bit
B: Blank period(Back porch + Front Porch)

Figure 124. Formula for the frame frequency

Example calculation

Driver raster-row: 320
1H period: 16 clock (RTN3 to 0 = 0000)
Operation clock division ratio: 1division
B: Blank period (BP + FP): 16

fosc = 60Hz x (0+16) clock x 1 division x (320+16) lines = 323 [kHz]

In this case, the RC oscillation frequency becomes 323 kHz. The external resistance value of the RC oscillator must be adjusted to be 323 kHz.

Preliminary

SCREEN-DIVISION DRIVING FUNCTION

The S6D0139 can select and drive two screens at any position with the screen-driving position registers (R42h/ R43h and R44h/R45h). Any two screens required for display are selectively driven and hence leads to a reduction in LCD-driving voltage and power consumption.

For the 1st division screen, start line (SS18 to 10) and end line (SE18 to 10) are specified by the 1st screen-driving position register (R42h/R43h). For the 2nd division screen, start line (SS28 to 20) and end line (SE28 to 20) are specified by the 2nd screen-driving position register (R44h/R45h). The 2nd screen control is effective when the SPT bit is 1. The total count of selection-driving lines for the 1st and 2nd screens must correspond to the LCD-driving duty set value. The address of selection-driving lines for the 1st and 2nd screens must be specified within the NL5-0 register setting value (LCD-driving duty set value).

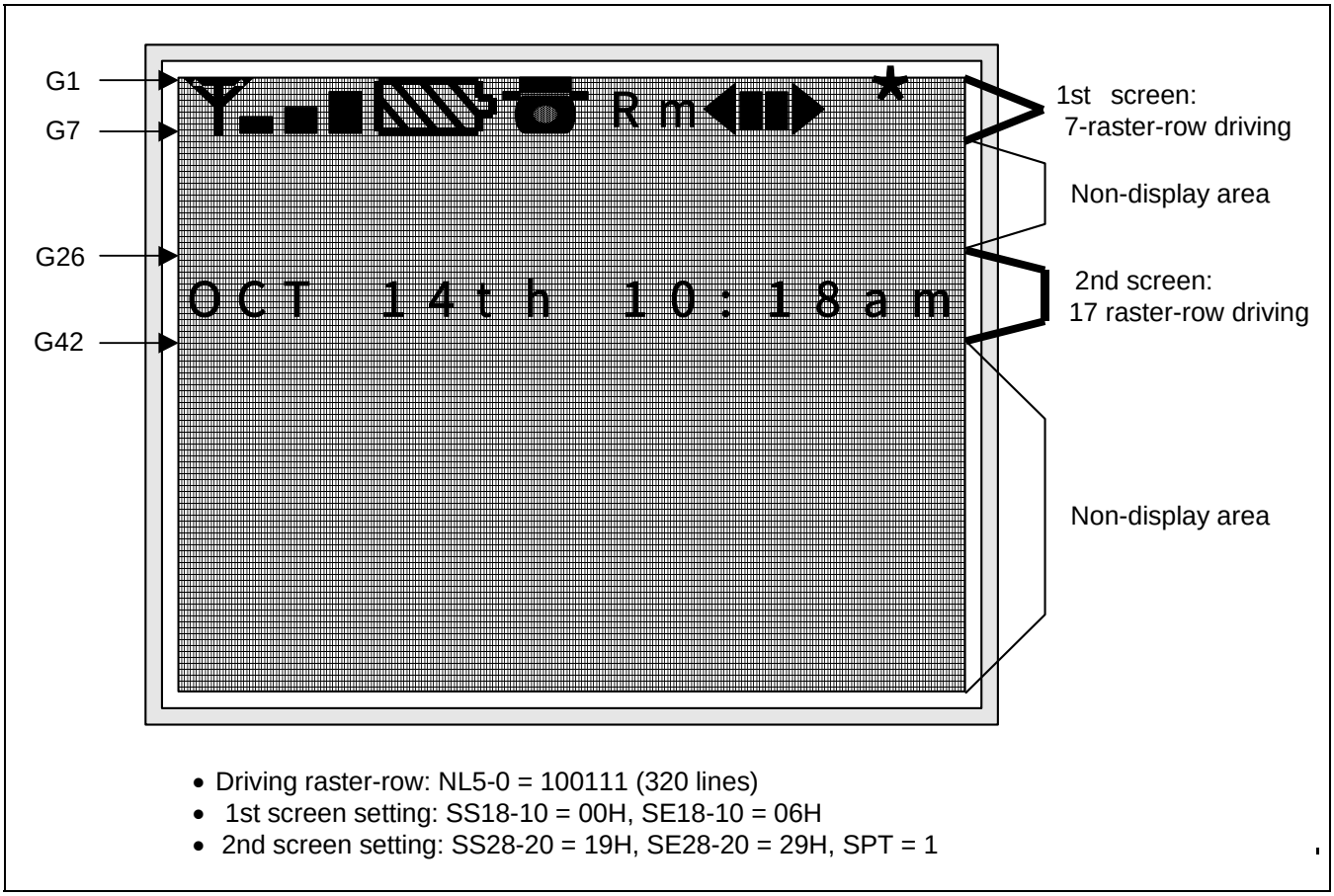

Figure 125. Driving on 2 screen

Preliminary

RESTRICTION ON THE 1ST/2ND SCREEN DRIVING POSITION REGISTER SETTINGS

The following restrictions must be satisfied when setting the start line (SS18 to 10) and end line (SE18 to 10) of the 1st screen driving position register (R42h/R43h) and the start line (SS28 to 20) and end line (SE28 to 20) of the 2nd screen driving position register (R44h/R45h) for the S6D0139. Note that incorrect display may occur if the restrictions are not satisfied.

Table 46. Restrictions on the 1st/2nd Screen Driving Position Register Setting

1st Screen Driving (SPT=0)

Register setting	Display operation
(SE18 to 10) – (SS18 to 10) = NL	Full screen display Normally displays (SE18 to 10) to (SS18 to 10)
(SE18 to 10) – (SS18 to 10) < NL	Partial display Normally displays (SE18 to 10) to (SS18 to 10) White display for all other times (RAM data is not related at all)
(SE18 to 10) – (SS18 to 10) > NL	Setting disabled

NOTE 1: SS18 to 10 ≤ SE18 to 10 ≤ 13Fh
NOTE 2: Setting SE28 to 20 and SS28 to 20 are invalid

2nd Screen Driving (SPT=1)

Register setting	Display operation
((SE18 to 10) – (SS18 to 10)) + ((SE28 to 20) – (SS28-20)) = NL	Full screen display Normally displays (SE28 to 10) to (SS18 to 10)
((SE18 to 10) – (SS18 to 10)) + ((SE28 to 20) – (SS28-20)) < NL	Partial display Normally displays (SE28 to 10) to (SS18 to 10) White display for all other times (RAM data is not related at all)
((SE18 to 10) – (SS18 to 10)) + ((SE28 to 20) – (SS28-20)) > NL	Setting disabled

NOTE 1: SS18 to 10 ≤ SE18 to 10 < SS28 to 20 ≤ SE28 to 20 ≤ 13Fh
NOTE 2: (SE28 to 20) – (SS18 to 10) ≤ NL

The driver output can't be set for non-display area during the partial display. Decision is based on the specification of the panels.

CL	PT1	PT0	Source Output on Non-display Area		VCOM Output on Non-display Area		Gate Output for Non-display Area
			Positive	Negative	Positive	Negative	
0	0	0	VGS	VGS	VCOML	VCOML	operating
0	0	1	VGS	GVDD	VCOML	VCOMH	
0	1	0	GVDD	VGS	VCOML	VCOMH	
0	1	1	Setting disable				
1	0	0	AVSS	AVSS	VCOML	VCOML	operating
1	0	1	AVSS	GVDD	VCOML	VCOMH	
1	1	0	GVDD	AVSS	VCOML	VCOMH	
1	1	1	Setting disable				

Refer to the following flow to set up the partial display.

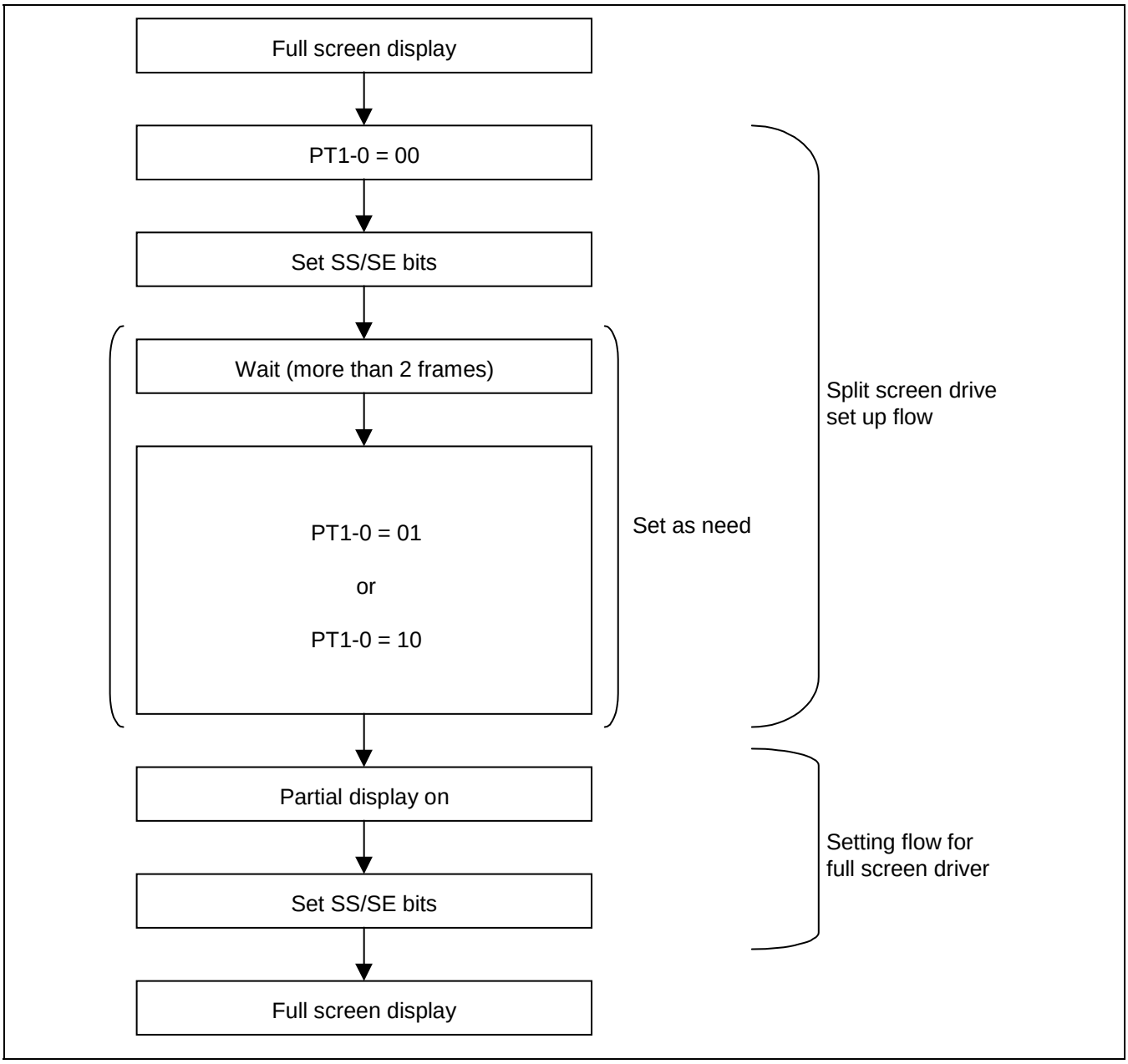

Figure 126. Partial display set up flow

Preliminary

APPLICATION CIRCUIT

The following figure indicates a schematic diagram of application circuit for S6D0139.
The interface used in the circuit is MDDI, and GPIO is also used as in/out port.
Sub panel driver interface is supported (80-mode 18/16 bit)

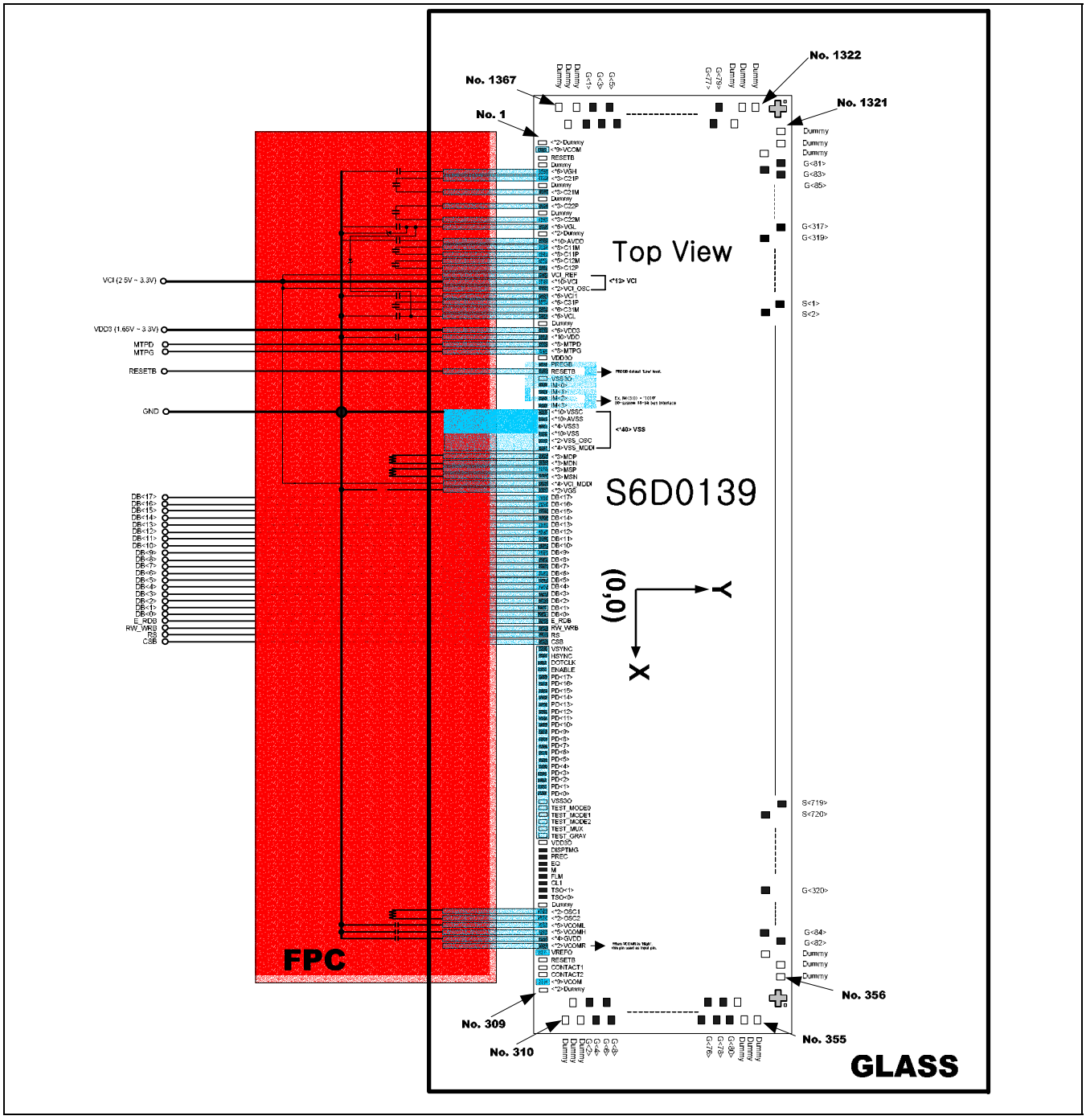

Figure 127. Application Circuit (18 bits - 80 CPU Interface Mode)

Preliminary

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 47. Absolute Maximum Rating

(VSS = 0V)

Item	Symbol	Rating	Unit
Supply voltage	VDD – VSS	-0.3 ~ 3.0	V
Supply voltage 3	VDD3 – VSS	-0.3 ~ 5.0	V
Supply voltage for step-up circuit	VCI - VSS	-0.3 ~ 5.0	V
LCD Supply Voltage range	AVDD - VSS	-0.3 ~ 6.5	V
	VSS - VCL	-0.3 ~ 5.0	V
	|VGH – VGL|	-0.3 ~ 35	V
Input Voltage range	Vin	-0.3 to VDD3 +0.3	V
Operating temperature	T_{opr}	-40 ~ 85	°C
Storage temperature	T_{stg}	-55 ~ 110	°C

Notes:

1. Absolute maximum rating is the limit value beyond which the IC may be broken. They do not assure operations.
2. Operating temperature is the range of device-operating temperature. They do not guarantee chip performance.
3. Absolute maximum rating is guaranteed when our company's package used.

Preliminary

DC CHARACTERISTICS

Table 48. DC Characteristics

(VSS = 0V)

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
Operating voltage	VDD		1.4	1.5	1.6	V	*1
	VDD3		1.65	-	3.3	V	*1
LCD driving voltage	VGH		7	-	18	V	
	VGL		-18	-	-3.5	V	
	VCL		-3.0	-	-1.75	V	
	AVDD		3.5	-	6.0	V	
	GVDD		3.	-	5.0	V	
Input high voltage	V_{IH}		0.8*VDD3	-	VDD3	V	*2
Input low voltage	V_{IL}		0	-	0.2*VDD3	V	*2
Output high voltage	V_{OH}	I_{OH} = -0.5mA	0.7*VDD3	-	VDD3	V	*3
Output low voltage	V_{OL}	I_{OL} = 0.5mA	0	-	0.3*VDD3	V	*3
Input leakage current	I_{IL}	VIN = VSS or VDD3	-1.0		1	uA	*2
Output leakage current	I_{OL}	VIN = VSS or VDD3	-3.0		3.0	uA	*3
Operating frequency	fosc	Frame freq. = 60 Hz Display line = 320		323		kHz	*4
External supply voltage	VCI		2.5		3.3	V	
1st step-up input voltage	VCI1		1.75		3.0	V	
1st step-up output efficiency	AVDD	ILOAD = 4 mA	90	95	100	%	*5
	AVDD	ILOAD = 7 mA	90	95	100	%	*6
2nd step-up output efficiency	VGH	ILOAD = 0.1 mA	90	95	100	%	*7
3rd step-up output efficiency	VGL	ILOAD = 0.1 mA	90	95	100	%	*7
4th step-up output efficiency	VCL	ILOAD = 0.6 mA	90	95	100	%	*5

Notes :

1. VSS = 0V.
2. Applied pins; IM3-0, CSB, E_RDB, RW_WRB, RS, DB0 to DB17, PD0 to PD17, PREGB, RESETB.
3. Applied pins; DB0 to DB17
4. Target frame frequency = 60 Hz, Display line = 320, Back porch = 8, Front porch = 8
   Internal RTN[1:0] register = “00”, Internal DIV[1:0] register = “00”
   (You Can measure OSC2(fosc) or CL1(fosc/16))
5. VCI=3.0V, VC=3, In normal load condition, only C11P & C11M can be used for AVDD boosting.
   And, at this time, C12P&C12M should be floated
6. VCI=3.0V, VC=3, , In high load condition, C11P&C11M&C12P&C12M should be used for AVDD boosting.

7. VCI=3.0V, VC=3, BT=7

Preliminary

Table 49. DC Characteristics for LCD driver outputs

(VDD = 1.5V, VDD3 = 3.0V, VSS = 0V)

Characteristic	Symbol	CONDITION	MIN	TYP	MAX	Unit	Note
LCD gate driver output On resistance	Ron	VGH–VGL=30.0V, VGH=16.5V, VGL=-13.5V			2	kohm	
LCD source driver delay	t_{SD}	SAP = “001”	-	-	40(TBD)	us	*1
		SAP = “010”	-	-	36(TBD)	us	*1
		SAP = “011”	-	-	32(TBD)	us	*1
		SAP = “100”	-	-	28(TBD)	us	*1
		SAP = “101”			25(TBD)	us	*1
		SAP = “110”			23(TBD)	us	*1
		SAP = “111”			22(TBD)	us	*1
Output voltage deviation (Mean value)	ΔV_O	$4.2V \leq V_{SO}$	-	±20	±50	mV	*2
		$0.8V < V_{SO} < 4.2V$	-	±10	±25	mV	*2
		$V_{SO} \leq 0.8V$	-	±20	±50	mV	*2
LCD source driver output voltage range	V_{SO}	-	GVDD+0.1	-	GVDD-0.1	V	-
LCD source driver output On resistance	Ronp	AVDD=4.5V GVDD=4.5V	-	-	20	kΩ	-
LCD source driver output On resistance	Ronn	AVDD=4.5V VGS=GNDV	-	-	20	kΩ	-
Current consumption during standby mode	Istby	Standby mode, Ta = 25 °C			20	uA	
Current consumption during normal operation	I_{VDD}	100pF load, Ta = 25 °C VC=011, DC=011, BT=111, GVD=111111 VCM=111111 VML=111111			150	uA	
	I_{VCI}				TBD	mA	

Note :

1. AVDD = 5.5V, GVDD = 5.0V, Ta = 25°C

t_{SD} is measured from 10% to 90% of output rising or falling time.

t_{SD} : LCD Source driver delay

t_{SD} = 1 / [Frame Freq. x {The number of raster-row + The number of blank period (FP+BP)}] – The marginal time for pixel load charge

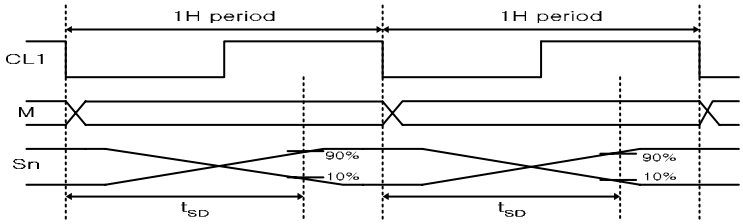

Figure 93. LCD Source driver delay

2. Vso the output voltage of analog output pins S1 to S720

SAMSUNG ELECTRONICS

Preliminary

AC CHARACTERISTICS

Table 50. Parallel Write Interface Characteristics (68 Mode)

(VDD = 1.4V to 1.6V, VDD3 = 1.65 to 3.3V, VCI = 2.5V to 3.3VT_A = -40 to +85 °C)

Characteristic		Symbol	Specification		Unit
			Min.	Max.	
Cycle time	Write	t_{CYCW68}	75	-	ns
	Read	t_{CYCR68}	500	-	
Pulse rise / fall time		t_R, t_F	-	10	
E pulse width high	Write	t_{WHW68}	27.5	-	
	Read	t_{WHR68}	250	-	
E pulse width low	Write	t_{WLW68}	27.5	-	
	Read	t_{WLR68}	250	-	
RW, RS and CSB Read setup time		t_{RAS68}	15	-	
RW, RS and CSB Write setup time		t_{WAS68}	10		
RW, RS and CSB hold time		t_{AH68}	2	-	
RW, RS and CSB wait time		t_{CSF68}	15		
Write data setup time		t_{WDS68}	60	-	
Write data hold time		t_{WDH68}	15	-	
Read data delay time		t_{RDD68}	-	200	
Read data hold time		t_{RDH68}	5	-	

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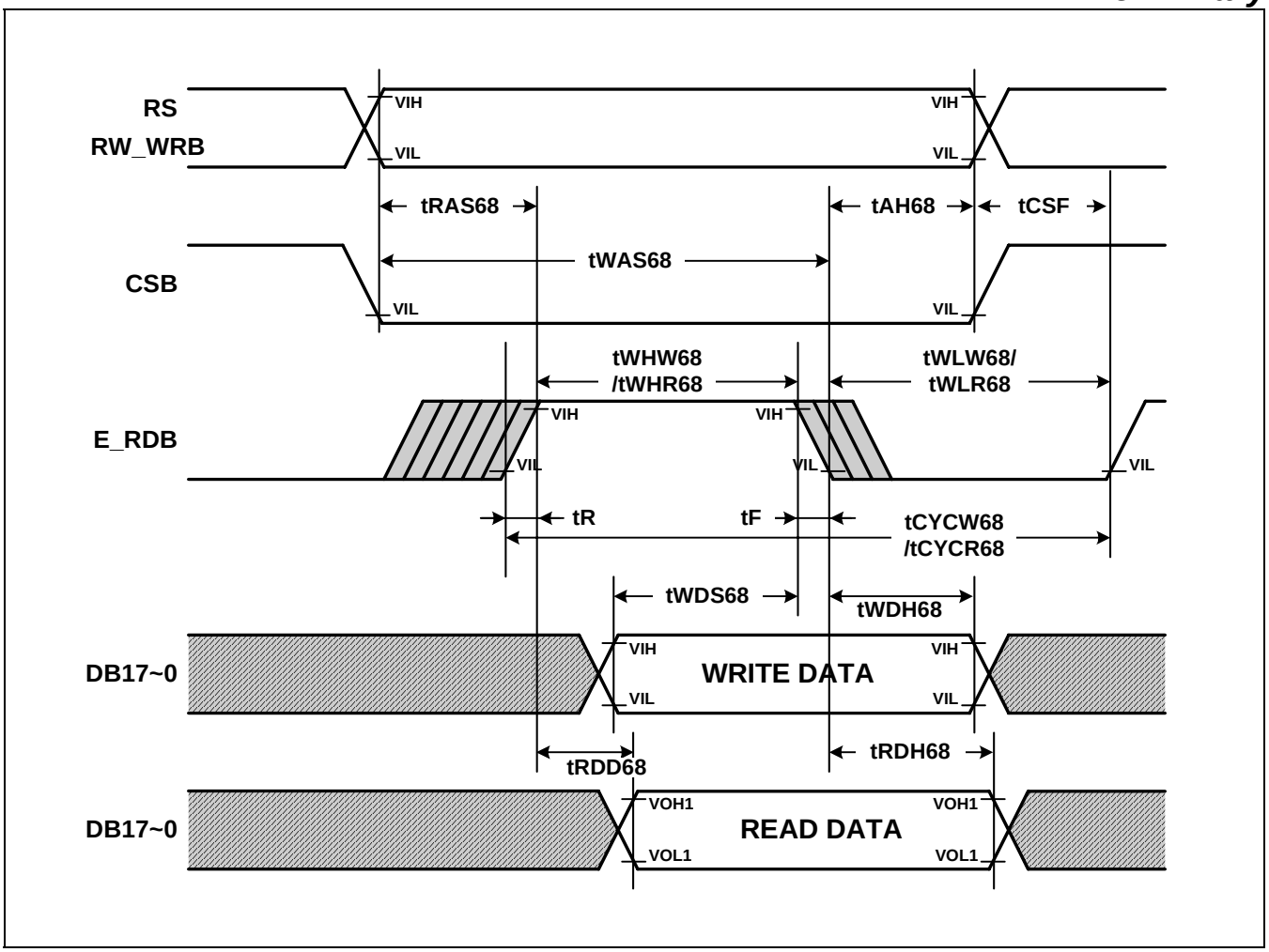

Figure 128. AC characteristics (68 Mode)

Preliminary

Table 51. Parallel Write Interface Characteristics (80 Mode)

(VDD = 1.4V to 1.6V, VDD3 = 1.65 to 3.3V, VCI = 2.5V to 3.3VT_A = -40 to +85 °C)

Characteristic		Symbol	Specification		Unit
			Min.	Max.	
Cycle time	Write	t_{CYCW80}	75	-	ns
	Read	t_{CYCR80}	500	-	
Pulse rise / fall time		t_R, t_F	-	10	
Pulse width low	Write	t_{WLW80}	27.5	-	
	Read	t_{WLR80}	250	-	
Pulse width high	Write	t_{WHW80}	27.5	-	
	Read	t_{WHR80}	250	-	
WRB and RS, CSB Read setup time		t_{AS80}	15	-	
WRB and RS, CSB Write setup time		t_{AS80}	10	-	
WRB and RS, CSB hold time		t_{AH80}	2		
WRB and RS, CSB wait time		t_{CSF80}	15	-	
Write data setup time		t_{WDS80}	20	-	
Write data hold time		t_{WDH80}	10	-	
Read data delay time		t_{RDD80}	-	200	
Read data hold time		t_{RDH80}	10	-	

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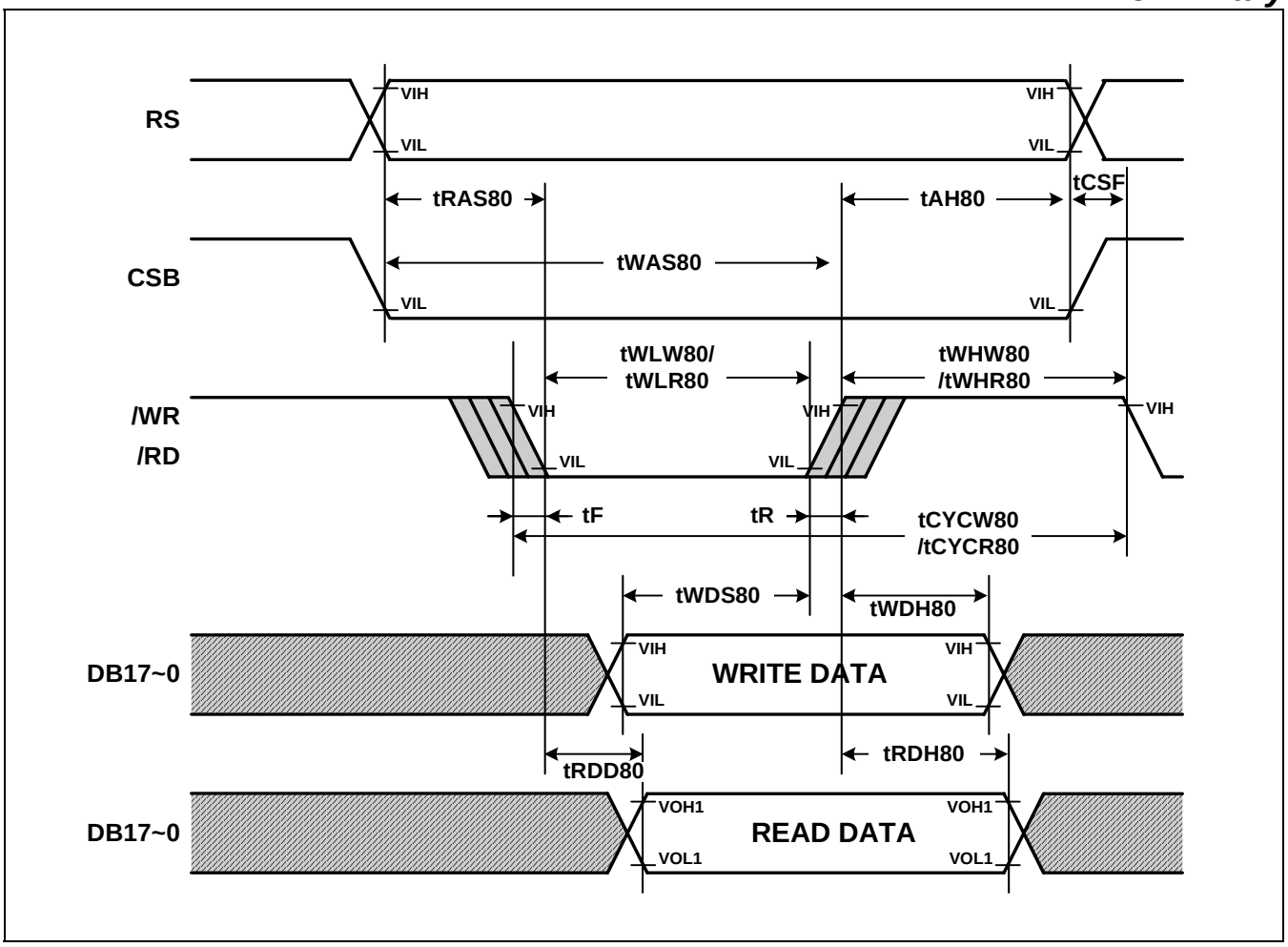

Figure 129. AC characteristics (80 Mode)

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Table 52. Clock Synchronized Serial Write Mode Characteristics

(VDD = 1.4V to 1.6V, VDD3 = 1.65 to 3.3V, VCI = 2.5V to 3.3VT_A = -40 to +85 °C)

Characteristic	Symbol	specification		Unit
		Min.	Max.	
Serial clock cycle time	tscyc	250	-	ns
Serial clock rise / fall time	tR, tF	-	10	ns
Pulse width high for write	tSCHW	40	-	ns
Pulse width high for read	tSCHR	230	-	ns
Pulse width low for write	tSCLW	60	-	ns
Pulse width low for read	tSCLR	230	-	ns
Chip Select setup time	tCSS	20	-	ns
Chip Select hold time	tCSH	60	-	ns
Serial input data setup time	tSIDS	30	-	ns
Serial input data hold time	tSIDH	30	-	ns
Serial output data delay time	tSODD	-	130	ns
Serial output data hold time	tSODH	5	-	ns

Table 53. Reset Timing Characteristics

(VDD = 1.4V to 1.6V, VDD3 = 1.65 to 3.3V, VCI = 2.5V to 3.3VT_A = -40 to +85 °C)

Characteristic	Symbol	Min.	Max.	Unit
Reset low pulse width	tRES	1	-	us

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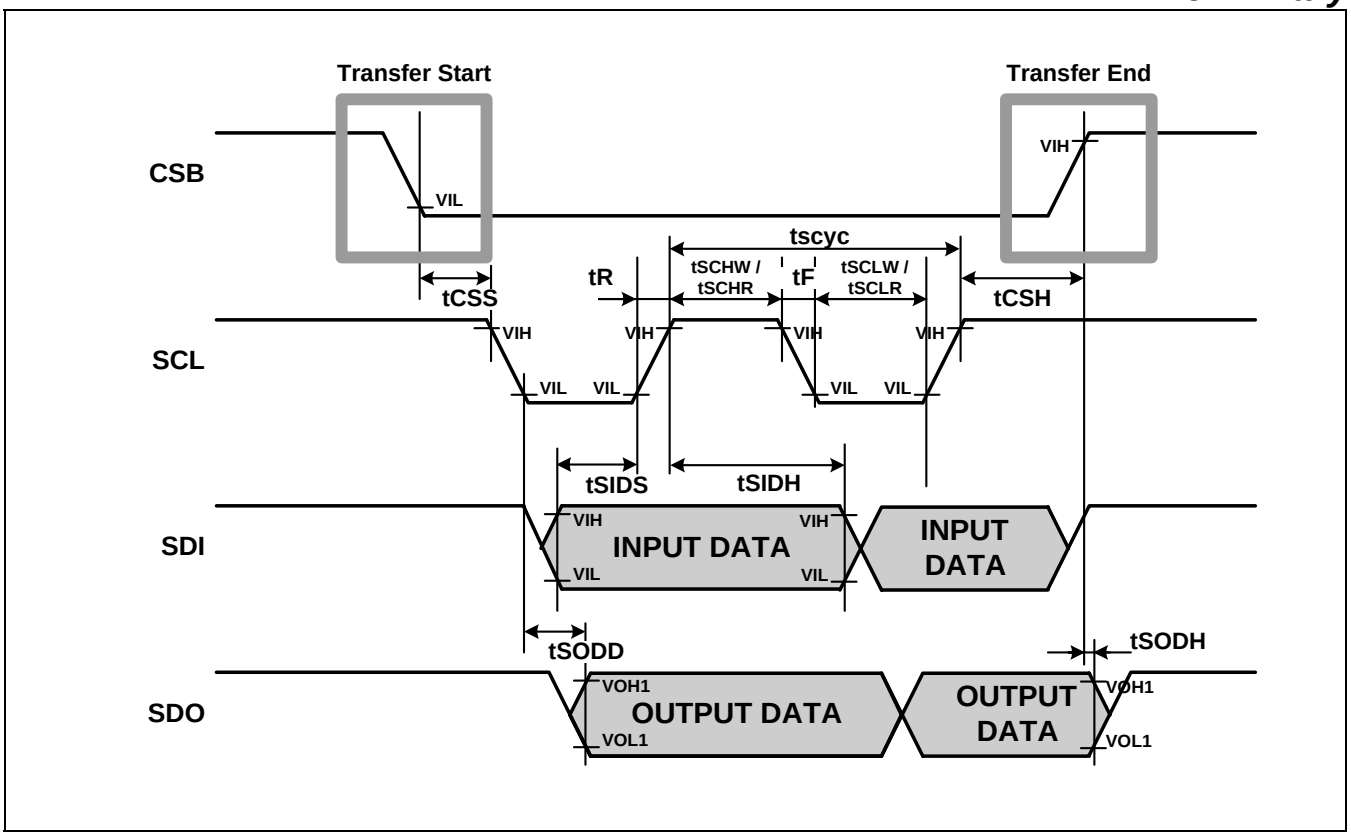

Figure 130. AC characteristics (SPI Mode)

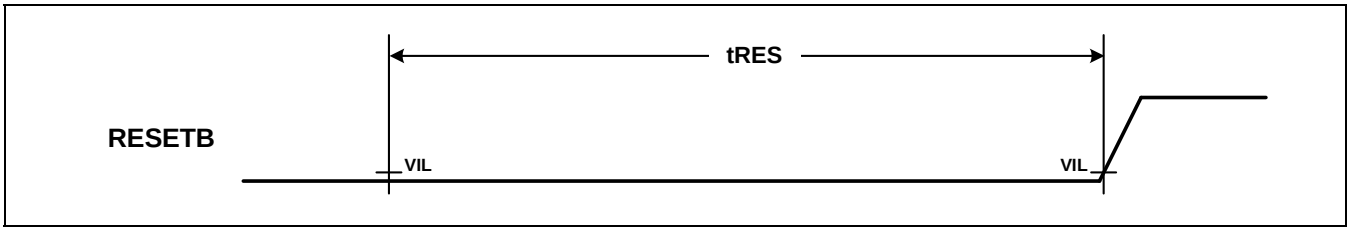

Figure 131. AC characteristics (RESET timing)

Table 54. RGB Data Interface Characteristics

(VDD = 1.4V to 1.6V, VDD3 = 1.65 to 3.3V, VCI = 2.5V to 3.3VT_A = -40 to +85 °C)

Characteristic	Symbol	Normal Mode				Unit
		18/16bit RGB interface		6bit RGB interface		
		Min.	Max.	Min.	Max.	
DOTCLK cycle time	tDCYC	100	-	55	-	ns
DOTCLK rise / fall time	tR, tF	-	2		2	ns
DOTCLK Pulse width high	tDCHW	40	-	27	-	ns
DOTCLK Pulse width low	tDCLW	40	-	27	-	ns
ENABLE setup time	tENS	30	-	15	-	ns
ENABLE hold time	tENH	20	-	7	-	ns
PD data setup time	tPDS	30	-	15	-	ns
PD data hold time	tPDH	20	-	7	-	ns

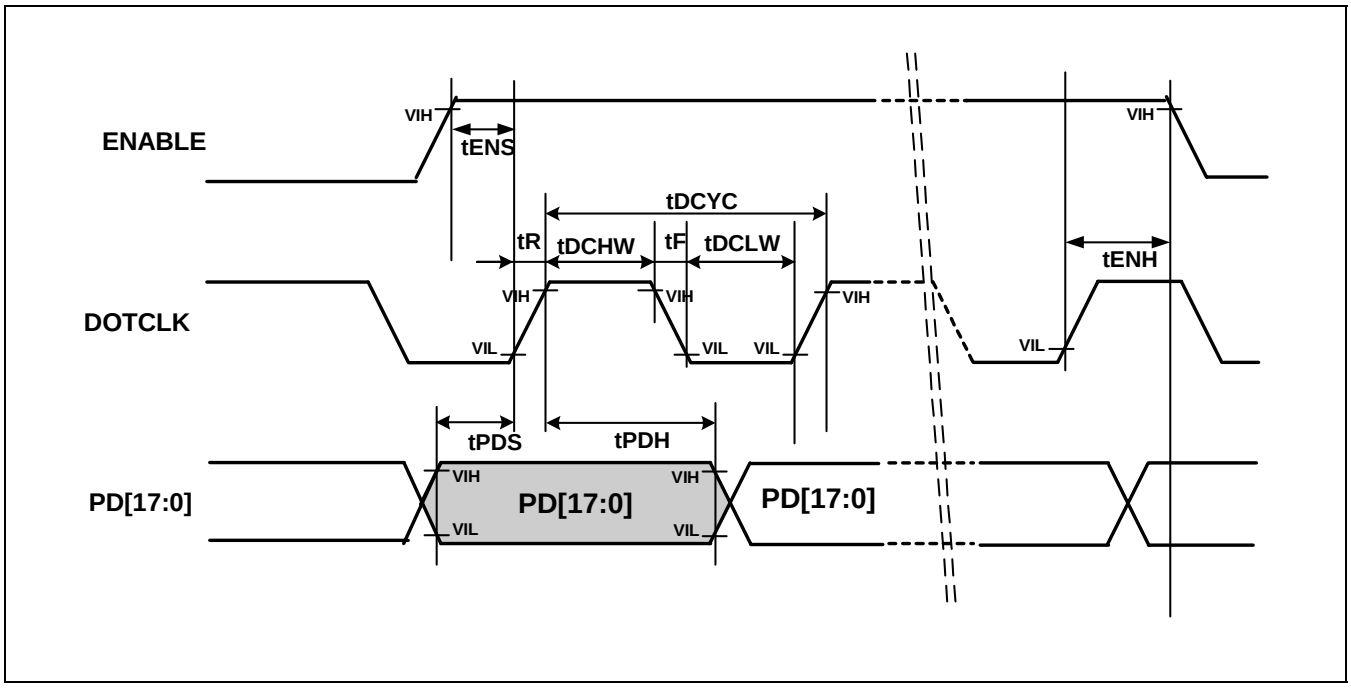

Figure 132. AC characteristics (RGB Mode)

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MDDI IO DC/AC CHARACTERISTICS

Table 45. DC/AC Characteristics

Parameter	Description	CONDITION	MIN	TYP	MAX	Unit	Note
V_{IT+}	Receiver input differential threshold voltage	Vinput_range=0V~1.65V			50	mV	
V_{IT-}	Receiver input differential threshold voltage	Vinput_range=0V~1.65V	-50			mV	
$V_{inp-offset-wakeup}$	Wake-up receiver input offset voltage	Vinput_range=0V~1.65V	75		175	mV	
$V_{inp-range}$	Single-ended receiver input operating range with respect to ground	Under all conditions	0V		1.65V	V	
$I_{bias-failsafe}$	Failsafe receiver bias current for avoiding false transitions	1.25mA typical	0.75		1.75	mA	
$I_{failsafe-off}$	Failsafe receiver bias leakage current when the offset is not enabled				0.5	uA	
$T_{hib-rcv-en}$	Hibernation receiver enable time				100	ns	
$I_{rcv-act}$	Standard receiver average current	Not including bias generation		300		uA	
$I_{rcv-hib}$	Hibernation receiver average current	Not including bias generation		30		uA	
$T_{delay-rcv}$	Propagation delay, standard receiver contribution				4	ns	
$T_{std-rcv-en}$	Standard receiver enable time, both with and without offset				100	ns	
$I_{diffabs}$	Absolute driver differential output current range		2.5		4.5	mA	
$V_{out-rng-int}$	Single-ended driver output voltage range with respect to ground, internal mode	Under all conditions, including double-drive	0.35		1.60	V	
$T_{hib-act-drv}$	Driver output enable time	Not including core to pad delay of enable			40	ns	
$T_{act-hib-drv}$	Driver output disable time	Not including core to pad delay of enable			40	ns	
$I_{drv,act}$	Average current consumption per driver, active mode, maximum speed	Includes pre-driver bias			8	mA	
$I_{drv,tri}$	Current consumption per drive, tri-stated (disabled)	Not including common reference circuitry			10	uA	
$T_{delay-drv}$	Driver propagation delay				3	ns	

Notes : Please refer to VESA specification Ver 1.0

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EXTERNAL POWER ON / OFF SEQUENCE

a) EXTERNAL POWER ON SEQUENCE

VDD3 should reach 90% before VCI does so. When regulator cap is 1μF, RESETB must be applied after VCI have been applied. The applied time gap between VCI and RESETB is minimum 1ms. As regulator cap becomes larger, this time gap must be increased. Otherwise function is not guaranteed.

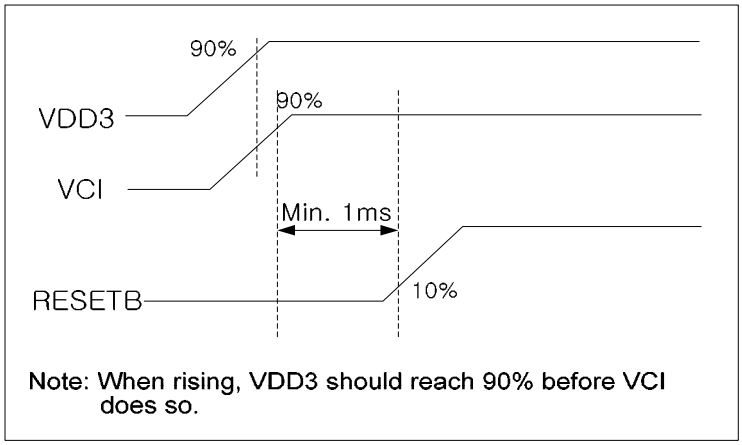

Figure 133. External power on sequence

b) EXTERNAL POWER OFF SEQUENCE

VCI should reach 90% before VDD3 does so. VCI must be powered down after RESETB have been powered down. The time gap of powered down between RESETB and VCI is minimum 1ms. Otherwise function is not guaranteed.

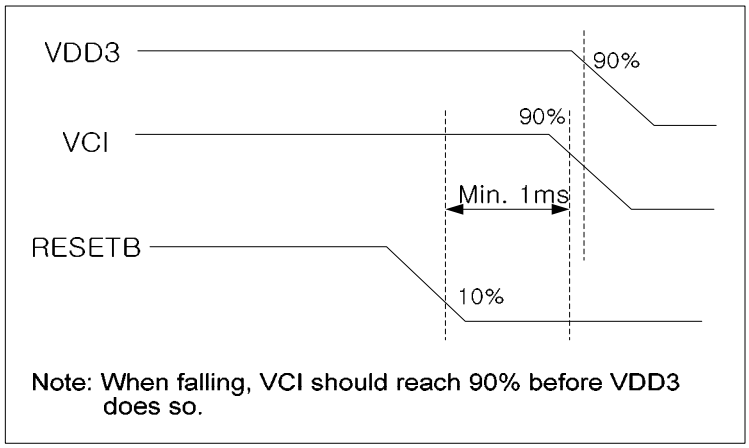

Figure 134. External power off sequence

Preliminary

DEFAULT REGISTER VALUES

	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0	hexadecimal
R00h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0001
R01h	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	0027
R02h	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0400
R03h	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0030
R07h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R08h	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0808
R09h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R0Bh	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R0Ch	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R10h	0	0	0	1	1	0	0	0	0	1	1	0	0	0	0	0	1860
R11h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R13h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R14h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R15h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R30h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R31h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R32h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R33h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R34h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R35h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R36h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R37h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R38h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R39h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R40h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R41h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R42h	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	013F
R43h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R44h	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	013F
R45h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R46h	1	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0	EF00
R47h	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	013F
R48h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R50h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R51h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R60h	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	0	007A
R61h	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0	0022
R73h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R75h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R76h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R77h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R78h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R79h	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	03FF
R90h	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0006
R91h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000
R92h	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0000

Preliminary

REVISION HISTORY

S6D0139 Specification Revision History			
Version	**Content**	**Author**	**Date**
0.0	Original	K. S .Cho	Nov. 21, 2005
0.1	10 page : Revised Figure 10 11 page : PAD configuration corrected 28 page : MISCELLANEOUS PIN added(PREC,EQ) 24 page : External VGL supply(-13.75V) comment removed 55 page : PT1-0 : 11 removed, setting disable changed 178page : Screen-division driving function – description changed VCI_REG -> ECS, VCI descrption changed. 179page : extended table, PT1-0: “11” setting disable 187page : Parallel Write Interface Characteristics (80mode): tcycw80 changed (min 100ns -> min 75ns)	K.S.Cho	Nov 26, 2005
0.2	9 page, Built in GRAM :1,382,000 bit -> 1,382,400 bit 10 page, the description of pad configuration added. 25 page, RESETB pin description corrected. 26 page, GPIO, S_CSB, S_RS, S_WRB pin description corrected. 46 page, MTP Testkey command is changed R94h to R92h 89 page, MTP description added 96 page, setup flow correction (reset and display off -> reset) 108 page, VSYNC interface figure corrected 182 page, numbering corrected. 184 page, table 49 186 page, VCI voltage added. 186 page, pulse width low/high changed (min 40ns -> min 27.5ns) 188 page, AC characteristic corrected. 188 page, VCI voltage added. 190 page, VCI voltage added. 192 page, VCI voltage added. 193 page, default register value added.	K.S.Cho	Feb 22, 2006
0.3	8 page, VGH, VGL updated. 82 page, gamma table updated 90 page, MTP sequence updated. 94 page, BT2-0 -> BT3-0, VGH, VGL updated 152 page, Read Instruction(R91h) addition 165 page, Table 38, updated 167 page, Table 40, updated 184 page, VGH, VGL updated	K.S.Cho	Mar 08, 2006
0.4	82 page, Register gamma table updated 157 page, Grayscale control figure updated. 158 page, Structure of grayscale amplifier figure updated 159 page, Structure of 8 to 1 selector figure updated 160 page, Operation of adjusting registers figure updated 161 page, Ratio adjustment register description added 162 page, Gamma correction register table updated 164 page, Ratio Adjustment table added	Sanjith	APR 04, 2006

Preliminary

0.5	64page, BT table corrected 83 page, NL-SCN figure corrected 187-190 page, CSB Read Setup time addition Chip Select Wait time addition	CKS	Arp 19,2006

Preliminary

NOTICE

Precautions for Light

When S6D0139 is exposed to light, it may cause motion of electrons inside the semiconductors, which might lead to a change in device characteristics. Hence, the users of the packages who may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the penetrating light protection to the IC at substrate (board or glass) or product design stage.

2. Always test and inspect products under the environment with no penetration of light.