TriFlash with MultiMediaCard Interface

Product Manual

Revision 1.2
3/2003

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Lit. No. 80-36-00180 Rev 1.2 3/2003 Printed in U.S.A.

Revision History

- *Revision 0.1—preliminary draft.*
- *Revision 0.5—first edits from marketing and engineering.*
- *Revision 0.6—several minor edits throughout document.*
- *Revision 0.9—addition of MLC and minor edits throughout document.*
- *Revision 1.0—removed Stream Read and Stream Write and minor edits throughout document.*
- *Revision 1.1— Changed power requirements in Section 2.2, Table 2.2; updated addresses in Appendix A*
- *Revision 1.2— Changed entry in Table 3-1 from "pull up to VDD" to "pull down to VSS".*

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1. Introduction to the TriFlash

The SanDisk TriFlash is a very small flash storage device, designed specifically for storage applications that put a premium on small form factor, low power and low cost. Flash is the ideal storage medium for portable, battery-powered devices. It features low power consumption and is non-volatile, requiring no power to maintain the stored data. It also has a wide operating range for temperature, shock and vibration.

TriFlash is well suited to meet the needs of small, low power, electronic devices. With a form factor as small as 10 mm by 12 mm and 1.1 mm thick, TriFlash can be used in a wide variety of portable devices like mobile phones, digital audio players, car navigation devices, and voice recorders.

To support this wide range of applications, the TriFlash is offered with either the MultiMediaCard or Secure Digital (SD) protocol (see *TriFlash with Secure Digital Interface Product Manual*). The MultiMediaCard protocol is a simple 3-pin interface, which can be shared by the TriFlash and MultiMediaCards, providing the most compact memory interface available today. For compatibility with existing controllers, the TriFlash offers, in addition to these interfaces, an alternate communication protocol based on the SPI standard.

These interfaces allow for easy integration into any design, regardless of microprocessor used. All device and interface configuration data (such as maximum frequency, card identification, etc.) are stored on the device.

The TriFlash provides up to 1024 Mbits of memory using SanDisk Flash memory chips, which were designed by SanDisk especially for use in mass storage applications. In addition to the flash memory chip, the TriFlash includes an intelligent controller that manages interface protocols, and data storage and retrieval, as well as Error Correction Code (ECC) algorithms, defect handling and diagnostics, power management and clock control.

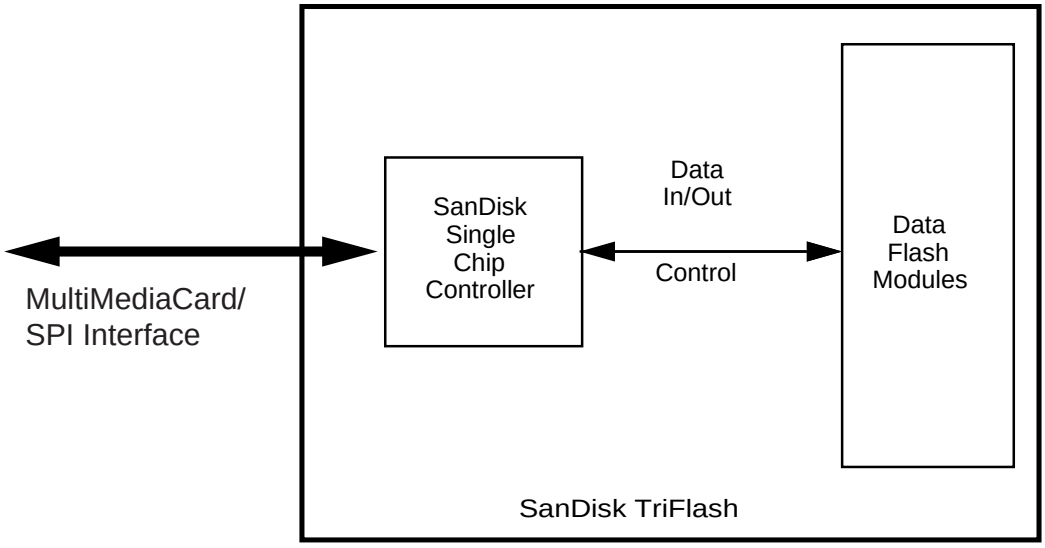

Figure 1-1. TriFlash with MultiMediaCard Interface Block Diagram

1.1. Scope

This document describes the key features and specifications of the TriFlash with the MultiMediaCard interface, as well as the information required to interface this product to a host system.

1.2. Product Models

The TriFlash is available in the capacities shown in Table 1-1.

Table 1-1. TriFlash Capacities

MMC Model No.	Capacities
SDAT1FAH-128	128 Mb
SDBT1FAH-256	256 Mb
SDBT1FCH-512	512 Mb
SDBT1FCH-1024	1024 Mb

1.3. System Features

TriFlash provides the following system features:

- Up to 1024 Mbits of data storage.
- MultiMediaCard protocol compatible.
- Supports SPI Mode.
- Targeted for portable and stationary applications for data storage.
- Voltage range: 2.7-3.6V.
- Variable clock rate 0-20 MHz.
- Maximum data rate with up to 10 devices or cards.
- Correction of memory field errors.
- Built-in write protection features (permanent and temporary).
- Comfortable erase mechanism.
- Standard pinout across all capacities.
- Single 3-wire bus for use with both the TriFlash and card.

The performance of the communication channel is described in Table 1-2.

Table 1-2. MultiMediaCard Bus /SPI Bus Comparison

TriFlash Using MultiMediaCard Bus	TriFlash Using SPI Bus
Three-wire serial data bus (Clock, Command, Data).	Three-wire serial data bus (Clock, DataIn, DataOut) + device specific CS signal (hardwired device selection).
Up to 64k devices addressable by the bus protocol.	Device selection via a hardware CS signal.
Error-protected data transfer.	Optional. A non-protected data transfer mode is available.
Sequential and single/multiple block oriented data transfer.	Single or multiple block oriented data transfer.

1.4. TriFlash with MultiMediaCard Interface Bus Standards

The SanDisk TriFlash is also fully compatible with the MultiMediaCard standard specification listed below:

The MultiMediaCard System Specification, Version 2.2

This specification may be obtained from:

MultiMediaCard Association
19672 Stevens Creek Blvd., Suite 404
Cupertino, CA 95014-2465
USA
Phone: 408-253-0441
Fax: 408-253-8811
Email: prophet2@mmca.org
http://www.mmca.org

1.5. Functional Description

The SanDisk TriFlash contains a high level, intelligent subsystem as shown in the block diagram, Figure 1-1. This intelligent (microprocessor) subsystem provides many capabilities not found in other types of devices. These capabilities include:

- Host independence from details of erasing and programming flash memory.
- Sophisticated system for managing defects (analogous to systems found in magnetic disk drives).
- Sophisticated system for error recovery including a powerful error correction code (ECC).
- Power management for low power operation.

1.5.1. Flash Technology Independence

The 512-byte sector size of the TriFlash is the same as that in an IDE magnetic disk drive. To write or read a sector (or multiple sectors), the host The host software then waits for the command to complete. The host software does not get involved in the details of how the flash memory is erased, programmed or read. This is extremely important as flash devices are expected to get more and more complex in the future. Because the TriFlash uses an intelligent on-board controller, the host system software will not require changing as new flash memory evolves. In other words, systems that support the TriFlash today will be able to access future SanDisk TriFlash devices built with new flash technology without having to update or change host software.

1.5.2. Defect and Error Management

The TriFlash contains a sophisticated defect and error management system. This system is analogous to the systems found in magnetic disk drives and in many cases offers enhancements. For instance, disk drives do not typically perform a read after write to confirm the data is written correctly because of the performance penalty that would be incurred. The TriFlash does a read after write under margin conditions to verify that the data is written correctly. In the rare case that a bit is found to be defective, the TriFlash replaces this bad bit with a spare bit within the sector header. If necessary, the TriFlash will even replace the entire sector with a spare sector. This is completely transparent to the host and does not consume any user data space.

The TriFlash device's soft error rate specification is much better than the magnetic disk drive specification. In the extremely rare case a read error does occur, the TriFlash has innovative algorithms to recover the data. This is similar to using retries on a disk drive but is much more sophisticated. The last line of defense is to employ a powerful ECC to correct the data. If ECC is used to recover data, defective bits are replaced with spare bits to ensure they do not cause any future problems. These defect and error management systems coupled with the solid-state construction give the TriFlash unparalleled reliability.

1.5.3. Endurance

The SanDisk TriFlash has an endurance specification for each sector of 100,000 writes (reading a logical sector is unlimited) under typical conditions. This far exceeds what is needed in nearly all applications of TriFlash devices. Even very heavy use of the TriFlash in cellular phones, personal communicators, pagers and voice recorders will use only a fraction of the total endurance over the typical device's lifetime. For instance, it would take over 34 years to wear out an area on the TriFlash on which a file of any size (from 512 bytes to maximum capacity) was rewritten 3 times per hour, 8 hours a day, 365 days per year. With typical applications, the endurance limit is not of any practical concern to the vast majority of users.

1.5.4. Automatic Sleep Mode

A unique feature of the SanDisk TriFlash (and other SanDisk products) is automatic entrance and exit from sleep mode. Upon completion of an operation, the TriFlash will enter the sleep mode to conserve power if no further commands are received within 5msec. The host does not have to take any action for this to occur. In most systems, the TriFlash is in sleep mode except when the host is accessing it, thus conserving power. When the host is ready to access the TriFlash and it is in sleep mode, any command issued to the TriFlash will cause it to exit sleep and respond.

1.5.5. TriFlash MultiMediaCard Mode

The following sections provide valuable information for TriFlash in MultiMediaCard mode.

1.5.5.1. MultiMediaCard Standard Compliance

The TriFlash with MultiMediaCard interface is fully compliant with MultiMediaCard Standard Specification, version 2.2. The structure of the Card Specific Data (CSD) register is compliant with CSD structure version 1.1.

1.5.5.2. Negotiating Operation Conditions

The TriFlash supports the operation condition verification sequence defined in the MultiMediaCard Standard Specifications. Should the TriFlash host define an operating voltage range, which is not supported by the TriFlash, it will put itself in an inactive state and ignore any bus communication. The only way to get the device out of the inactive state is by powering it down and up again. In addition, the host can explicitly send the device to the inactive state by using the GO_INACTIVE_STATE command.

1.5.5.3. Device Acquisition and Identification

The MultiMediaCard bus is a single master (TriFlash host) and multi-slaves (devices) bus. The host can query the bus and find out how many devices of which type are currently connected. The TriFlash's CID register is pre-programmed with a unique card identification number that is used during the acquisition and identification procedure.

In addition, the TriFlash host can read the device's CID register using the READ_CID command. The CID register is programmed during the TriFlash testing and formatting procedure, on the manufacturing floor. The TriFlash host can only read this register and not write to it.

1.5.5.4. Device Status

TriFlash status is stored in a 32-bit status register which is sent as the data field in the device response to host commands. The Status register provides information about the device's current state and completion codes for the last host command. The device status can be explicitly read (polled) with the SEND_STATUS command.

1.5.5.5. Memory Array Partitioning

Although the TriFlash memory space is byte addressable with addresses ranging from 0 to the last byte, it is not a simple byte array but divided into several structures as follows:

- Memory bytes are grouped into 512 byte blocks called sectors. Every block can be read, written and erased individually.
- Sectors are grouped into erase groups of 16 or 32 sectors depending on device size. Any combination of sectors within one group, or any combination of erase groups can be erased in a single erase command. A write command implicitly erases the memory before writing new data into it. An explicit erase command can be used for pre-erasing memory, which will speed up the next write operation.
- Erase groups are grouped into Write Protect Groups (WPG) of 32 erase groups. The write/erase access to each WPG can be limited individually. A diagram of the memory structure hierarchy is shown in Figure 1-2.

The number of various memory structures for the different TriFlash devices are summarized in Table 1-3. The last (highest in address) WPG will be smaller and contain less than 32 erase groups.

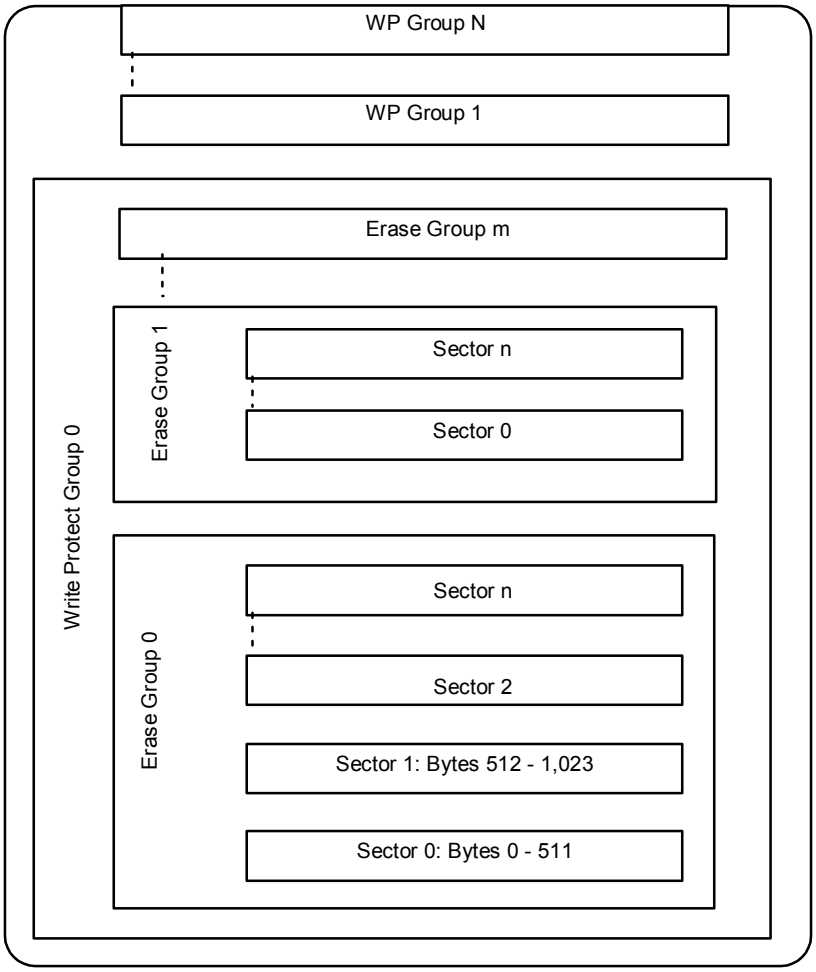

Figure 1-2. Memory Array Partitioning

Table 1-3. TriFlash Memory Array Structures Summary

Part Number	Bits	Sector	Erase Group Size (Sectors)	Number of Erase Groups	Write Protect Group Size (erase groups)	Number of Write Protect Groups
SDBT1FCH-1024	1024Mb	250,880	32	7,840	32	245
SDBT1FCH-512	512Mb	125,440	32	3,920	32	123
SDBT1FAH-256	256Mb	62,720	32	1,960	32	62
SDAT1FAH-128	128Mb	31,360	32	980	32	31

1.5.5.6. Read and Write Operations

The TriFlash supports three read/write modes as shown in Figure 1-3.

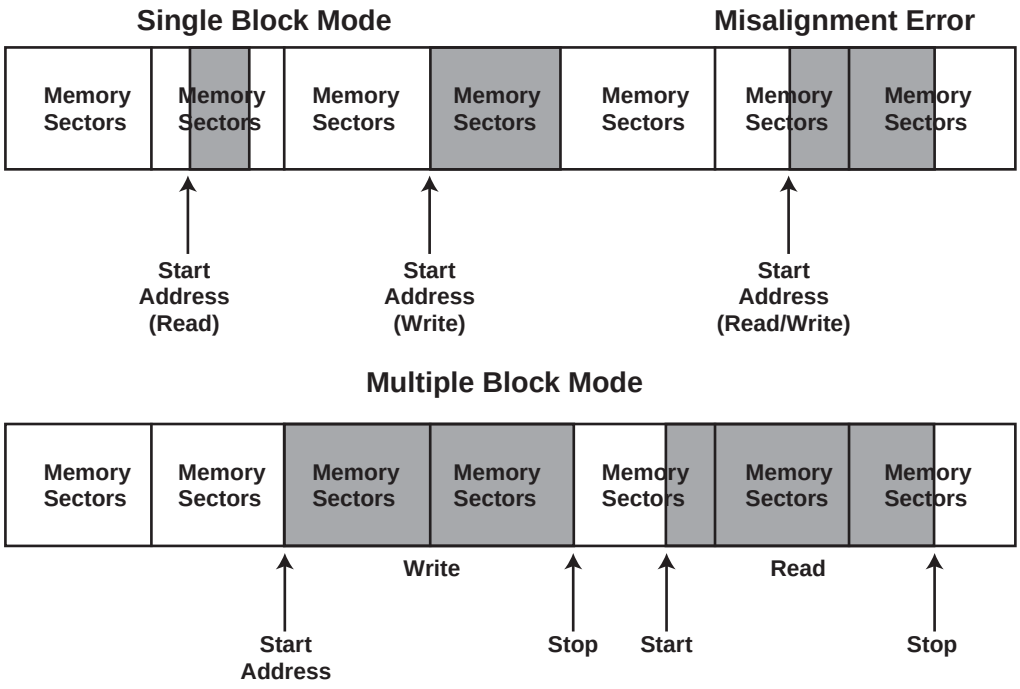

Figure 1-3. Data Transfer Formats

Single Block Mode

In this mode, the host reads or writes one data block in a pre-specified length. The data block transmission is protected with 16-bit CRC, which is generated by the sending unit and checked by the receiving unit.

The block length for read operations is limited by the device sector size (512 bytes), but can be as small as a single byte. Misalignment is not allowed. Every data block must be contained in a single physical sector.

The block length for write operations must be identical to the sector size and the start address aligned to a sector boundary.

Multiple Block Mode

This mode is similar to the single block mode, but the host can read/write multiple data blocks (all have the same length), which will be stored or retrieved from contiguous memory addresses starting at the address specified in the command.

The operation is terminated with a stop transmission command.

Misalignment and block length restrictions apply to multiple blocks as well, and are identical to the single block read/write operations.

1.5.5.7. Data Protection in the TriFlash

Every sector is protected with an Error Correction Code (ECC). The ECC is generated (in the device) when the sectors are written and validated when the data is read. If defects are found, the data is corrected prior to transmission to the host.

1.5.5.8. Erase

The smallest erasable unit in the TriFlash is a sector. In order to speed up the erase procedure, multiple sectors can be erased at the same time. To facilitate selection, a first command with the starting address is followed by a second command with the final address, and all sectors within this range are selected for erase.

1.5.5.9. Write Protection

Two device level write protection options, permanent and temporary, are available. Both can be set using the PROGRAM_CSD command (see Section 4.2.2). The permanent write protect bit, once set, cannot be cleared. This feature is implemented in the TriFlash controller firmware and not with a physical OTP cell.

1.5.5.10. Copy Bit

The content of a TriFlash can be marked as an original or a copy using the copy bit in the CSD register. Once the Copy bit is set (marked as a copy) it cannot be cleared. The Copy bit of the TriFlash is programmed (during test and formatting on the manufacturing floor) as a copy. The TriFlash can be purchased with the copy bit set (copy) or cleared, indicating the device is a master. This feature is implemented in the TriFlash controller firmware and not with a physical OTP cell.

1.5.5.11. The CSD Register

All the configuration information of the TriFlash is stored in the CSD register. The MSB bytes of the register contain manufacturer data. The two least significant bytes contain the host controlled data: the device Copy and write protection, the user file format indication, and the user ECC register.

The host can read the CSD register and alter the host-controlled data bytes using the SEND_CSD and PROGRAM_CSD commands (see Section 4.2.2).

1.5.6. TriFlash—SPI Mode

The SPI mode is a secondary communication protocol for TriFlash devices. This mode is a subset of the MultiMediaCard bus protocol, designed to communicate with an SPI channel, commonly found in Motorola's (and lately a few other vendors') microcontrollers.

1.5.6.1. Negotiating Operating Conditions

The operating condition negotiation function of the MultiMediaCard bus is not supported in SPI mode. The host must work within the valid voltage range (2.7 to 3.6 volts) of the card.

1.5.6.2. Device Acquisition and Identification

The host must know the number of devices currently connected on the bus. Specific device selection is done via the CS signal. The internal pullup resistor on the CD line may be used for device detection (insertion/removal).

1.5.6.3. Device Status

In SPI mode, only 16 bits (containing the errors relevant to SPI mode) can be read out of the 32-bit TriFlash status register.

1.5.6.4. Memory Array Partitioning

Memory partitioning in SPI mode is equivalent to MultiMediaCard Bus mode. All read and write commands are byte addressable with the limitations given in section 1.5.7.5 above.

1.5.6.5. Read and Write Operations

In SPI mode, both single and multiple block data transfer modes are supported.

1.5.6.6. Data Transfer Rate

Same as for the MultiMediaCard mode when the device is operating in single block read/write mode.

1.5.6.7. Data Protection in the TriFlash

Same as for the MultiMediaCard Bus mode.

1.5.6.8. Erase

Same as in MultiMediaCard Bus mode.

1.5.6.9. Write Protection

Same as in MultiMediaCard Bus mode.

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2. Product Specifications

For all the following specifications, values are defined at ambient temperature and nominal supply voltage unless otherwise stated.

2.1. System Environmental Specifications

Table 2-1. System Environmental Specifications

Temperature	Operating: Non-Operating:	-25° C to 85° C -40° C to 85° C
Humidity	Operating: Non-Operating:	8% to 95%, non-condensing 8% to 95%, non-condensing
ESD Protection		± 2kV, Human body model
Vibration	Operating: Non-Operating:	15 G peak to peak max. 15 G peak to peak max.
Shock	Operating: Non-Operating:	1,000 G max. 1,000 G max.
Altitude (relative to sea level)	Operating: Non-Operating:	80,000 feet max. 80,000 feet max.

2.2. Typical Power Requirements

Table 2-2. Power Requirements

VDD (ripple: max, 60 mV peak to peak)	2.7 V–3.6 V

(Ta = -25 – 85C)

	@ VDD = 2.7 V	**@ VDD = 3.6 V**
Operating current (maximum rates). Fclk = 20 MHz, 0.5 MByte/s. Read/Write speed	Read: 30 mA Write: 35 mA	Read: 40 mA Write: 45 mA

(Ta = -25 – 85C)

		Typical	**Maximum**
Sleep Current	@ 2.7 V	40 uA	120 uA
	@3.3 V	50 uA	150 uA

2.3. System Performance

Table 2-3. System Performance[1]

	Typical	Maximum
Block Read Access Time		
Binary Products	1.5msec	15msec
MLC Products	10msec	100msec
Block Write Access Time		
Binary Products	24msec	240msec
MLC Products	40msec	400msec
CMD1 to Ready (after power up)	50msec	500msec
Sleep to Ready	1msec	2msec

2.4. System Reliability and Maintenance

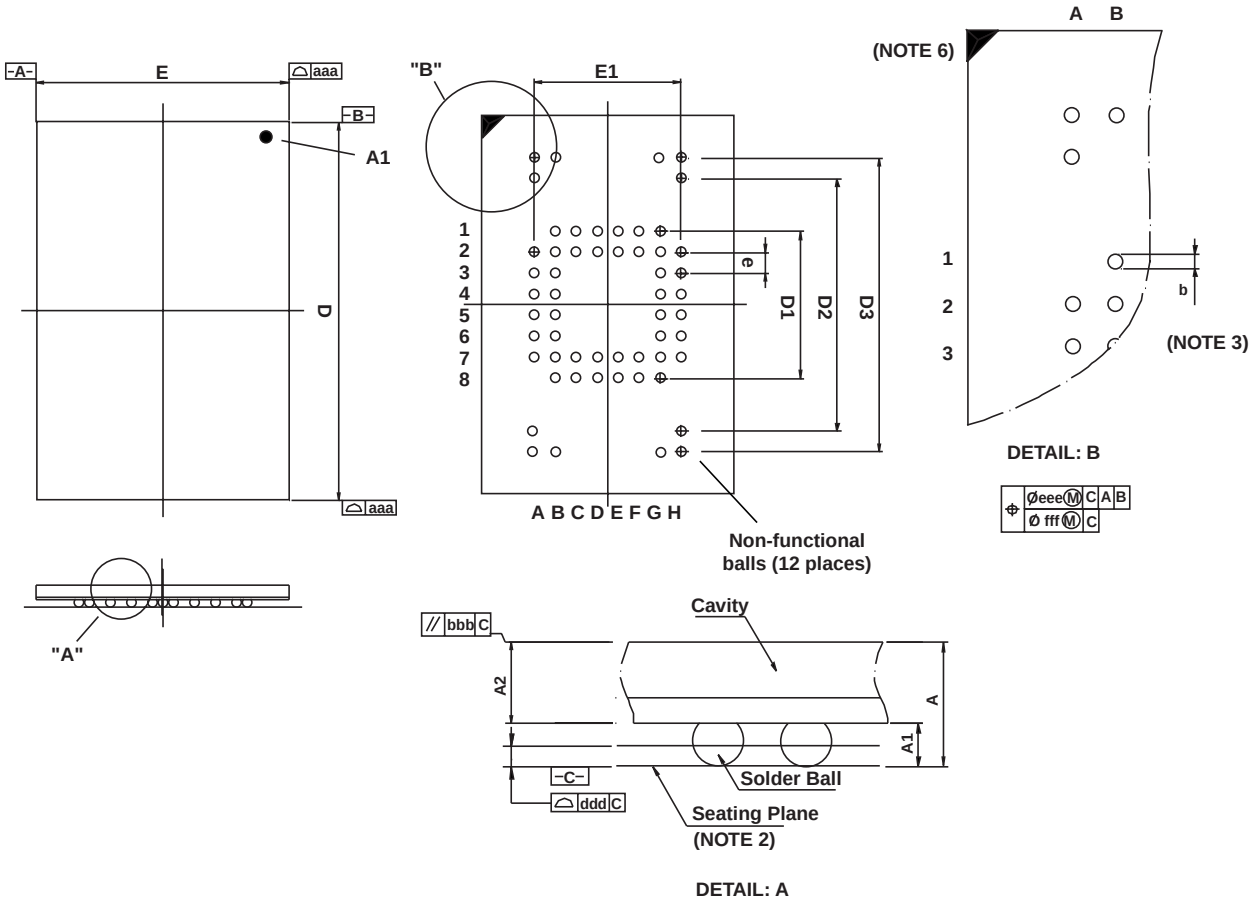
Table 2-4. System Reliability and Maintenance Specifications

MTBF	> 1,000,000 hours
Preventive Maintenance	None
Data Reliability	< 1 non-recoverable error in 10^{14} bits read
Endurance	≥ 100,000 erase/program cycles per block, typical

2.5. Physical Specifications

See Figures 2-1 and 2-2 for the physical specifications and dimensions and Figure 2-3 for pin definitions.

[1] All values quoted are under the following conditions:
a) Voltage range: 2.7 V to 3.6 V.
b) Temperature range: -25° C to 85° C.
c) Are independent of the TriFlash clock frequency.

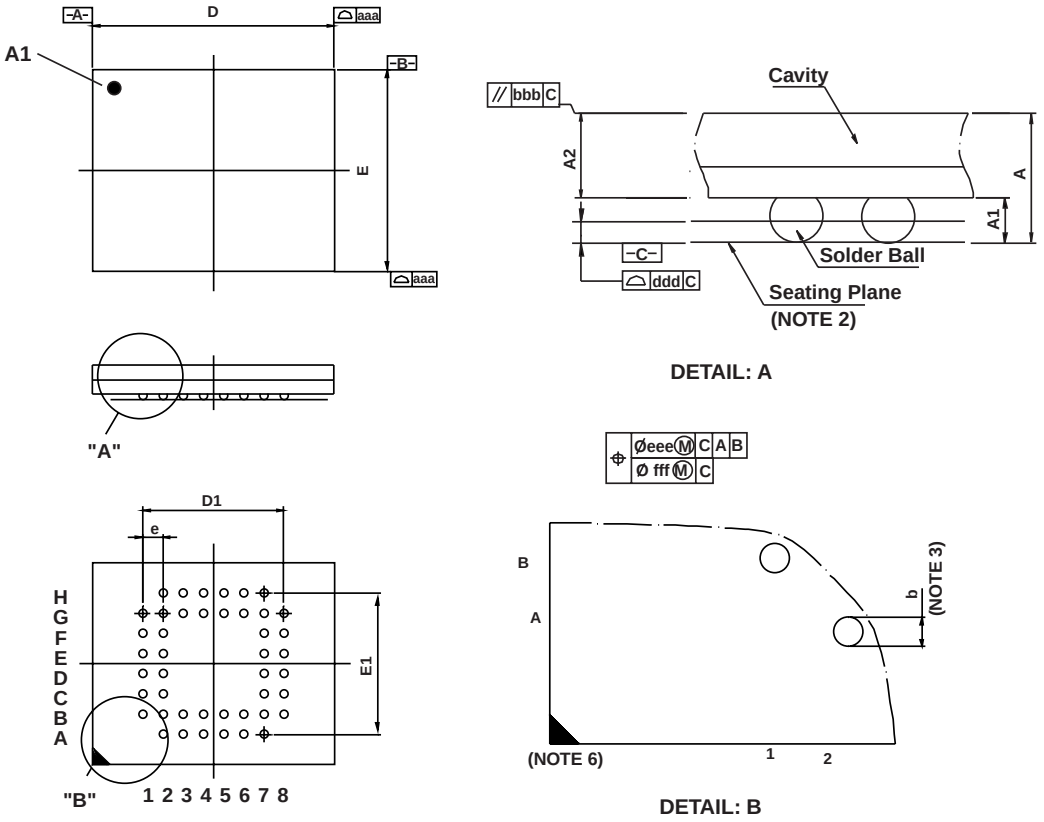


Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	Min	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.32	0.35	0.38	0.013	0.014	0.015
A2	0.62	0.67	0.72	0.024	0.026	0.028
D	17.90	18.00	18.10	0.705	0.709	0.713
E	11.90	12.00	12.10	0.469	0.472	0.476
D1	---	7.00	---	---	0.276	---
D2	---	11.00	---	---	0.433	---
D3	---	13.00	---	---	0.512	---
E1	---	7.00	---	---	0.276	---
e	---	1.00	---	---	0.039	---
b	0.40	0.45	0.50	0.016	0.018	0.020
aaa	0.10			0.004		
bbb	0.10			0.004		
ddd	0.15			0.006		
eee	0.25			0.010		
fff	0.10			0.004		
MD/ME	12/11			12/11		

NOTE:

1. Controlling Dimension: Millimeter.
2. Primary Datum C and seating plane are defined by the spherical crowns of the solder balls.
3. Dimensions b is measured at the maximum solder ball diameter, parallel to Primary Datum C.
4. There shall be a minimum clearance of 0.25mm between the edge of the solder ball and the body edge.
5. Reference document: JEDEC MO-205.
6. The pattern of Pin 1 Fiducial is for reference only.
7. All numbers are in mm.
8. All numbers are typical unless otherwise stated.

Figure 2-1. TriFlash Physical Specifications—18 X 12mm Package



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	Min	NOM	MAX
A	---	---	1.10	---	---	0.043
A1	0.32	0.35	0.38	0.013	0.014	0.015
A2	0.62	0.67	0.72	0.024	0.026	0.028
D	11.90	12.00	12.10	0.469	0.472	0.476
E	9.90	10.00	10.10	0.390	0.394	0.398
D1	---	7.00	---	---	0.276	---
E1	---	7.00	---	---	0.276	---
e	---	1.00	---	---	0.039	---
b	0.40	0.45	0.50	0.016	0.018	0.020
aaa		0.10			0.004	
bbb	0.10			0.004		
ddd	0.15			0.006		
eee	0.25			0.010		
fff	0.10			0.004		
MD/ME	8/8			8/8		

NOTE:

1. Controlling Dimension: Millimeter.
2. Primary Datum C and seating plane are defined by the spherical crowns of the solder balls.
3. Dimensions b is measured at the maximum solder ball diameter, parallel to Primary Datum C.
4. There shall be a minimum clearance of 0.25mm between the edge of the solder ball and the body edge.
5. Reference document: JEDEC MO-205.
6. The pattern of Pin 1 Fiducial is for reference only.

Figure 2-2. TriFlash Physical Specifications—12 X 10mm Package

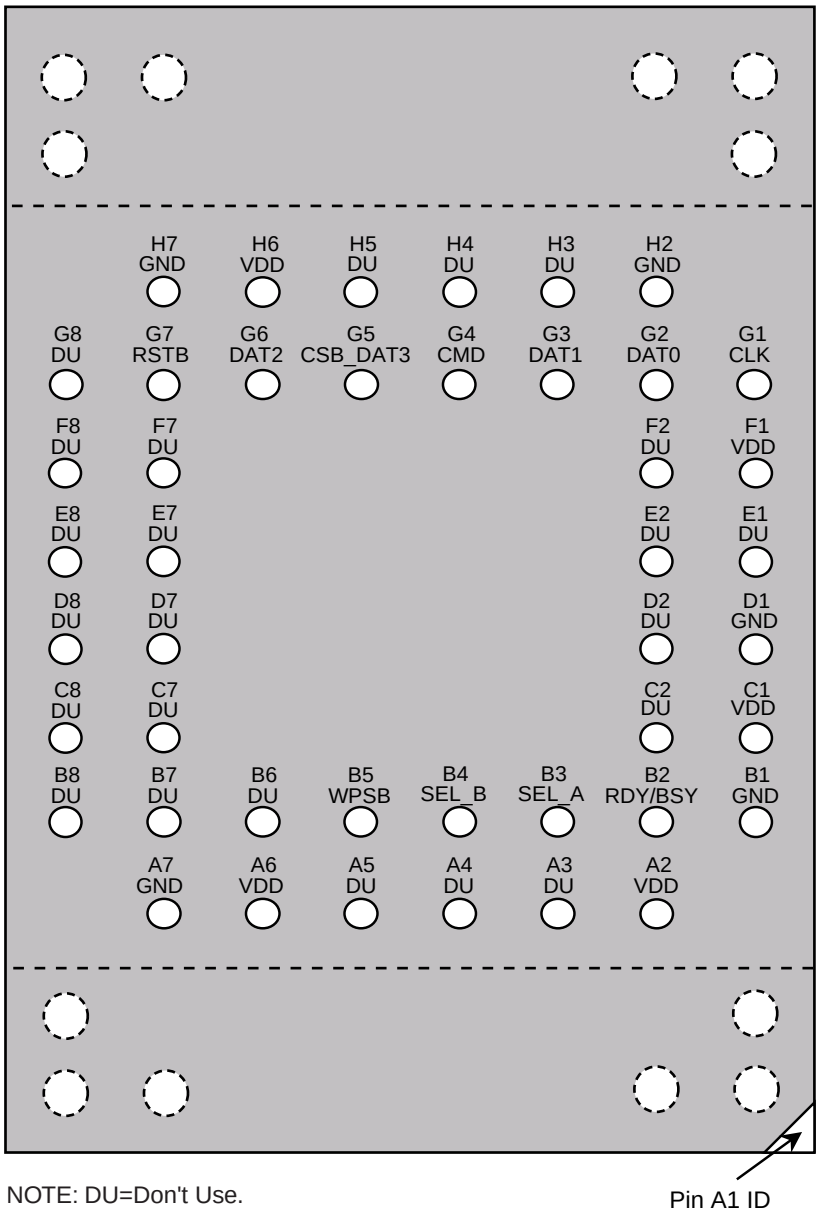


Figure 2-3. TriFlash Pin Definitions (Top View)

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3. TriFlash Interface Description

3.1. General Description of Pins and Registers

The TriFlash is a BGA package with 44 core balls (see Figure 2-3). The host is connected to the TriFlash using the 11 interface connections shown in Tables 3-1 and 3-2, plus power and ground balls.

3.1.1. Pin Assignments in MultiMediaCard Mode

Table 3-1. MultiMediaCard Pin Definition

Pin #	Name	Type[1]	Function	Comment
H6, F1, C1, A2, A6	V_{DD}	S	Supply Voltage	
H7, H2, D1, B1, A7	V_{SS}	S	Supply Voltage Ground	
G2	DAT0	I/O	Data Line	
G3	DAT1	I/O	Unused	Pull up to VDD
G6	DAT2	I/O	Unused	Pull up to VDD
G5	DAT3	I/O	Unused	Pull up to VDD
G1	CLK	I	Clock	
G4	CMD	I/O	Command/Response	
B5	WPSB	I	Write Protect	
G7	RSTB	I	Reset (Active low)	
B2	RDY/BSY	O	Ready/Busy Interrupt	
B3	SEL_A	I	Defines I/F	Pull down to VSS
B4	SEL_B	I	Defines I/F	Pull down to VSS

[1] S=power supply; I=input; O=output using push-pull drivers.

3.1.2. Pin Assignments in SPI Mode

Table 3-2. SPI Bus Mode Pin Definition

Pin #	Name	Type[1]	Function	Comment
H6, F1, C1, A2, A6	V_{DD}	S	Supply Voltage	
H7, H2, D1, B1, A7	V_{SS}	S	Supply Voltage Ground	
G2	DataOut	I/O	Device to Host Data and Status	
G3	DAT1	I/O	Unused	Pull up to VDD
G6	DAT2	I/O	Unused	Pull up to VDD
G5	CS	I	Chip Select (Active low)	
G1	CLK	I	Clock	
G4	DataIn	I	Host to Device Commands and Data	
B5	WPSB	I	Write Protect	
G7	RSTB	I	Reset (Active low)	
B2	RDY/BSY	O	Ready/Busy Interrupt	
B3	SEL_A	I	Defines I/F	Pull down to VSS
B4	SEL_B	I	Defines I/F	Pull down to VSS

3.1.3. Registers

Each device has a set of information registers. A detailed description is given in section 4.5.

Table 3-3. TriFlash with MultiMediaCard Registers

Name	Width	Description
CID	128	Card identification number: individual device number for identification.
RCA[2]	16	Relative card address: local system address of a device, dynamically suggested by the device and approved by the host during initialization.
CSD	128	Card specific data: information about the device operation conditions.
OCR	32	Operation Condition Register.

The host may reset the devices by switching the power supply off and on again. The device has its own power-on detection circuitry that puts the device into an idle state after the power-on. The device can also be reset by sending the GO_IDLE (CMD0) command, or by providing a negative pulse on the RESET pin.

[1] S=power supply; I=input; O=output using push-pull drivers.

[2] The RCA register is not used (available) in SPI Mode.

3.2. MultiMediaCard Bus Topology

The MultiMediaCard Bus has three communication lines and power and ground:

- **CMD**—Command is a bi-directional signal. Host and device drivers are operating in two modes, open drain and push pull.
- **DAT**—Data is a bi-directional signal. Host and device drivers are operating in push pull mode.
- **CLK**—Clock is a host to device signal. CLK operates in push pull mode.
- **VDD**—VDD is the power supply line for all devices.
- **VSS**—VSS are ground lines.

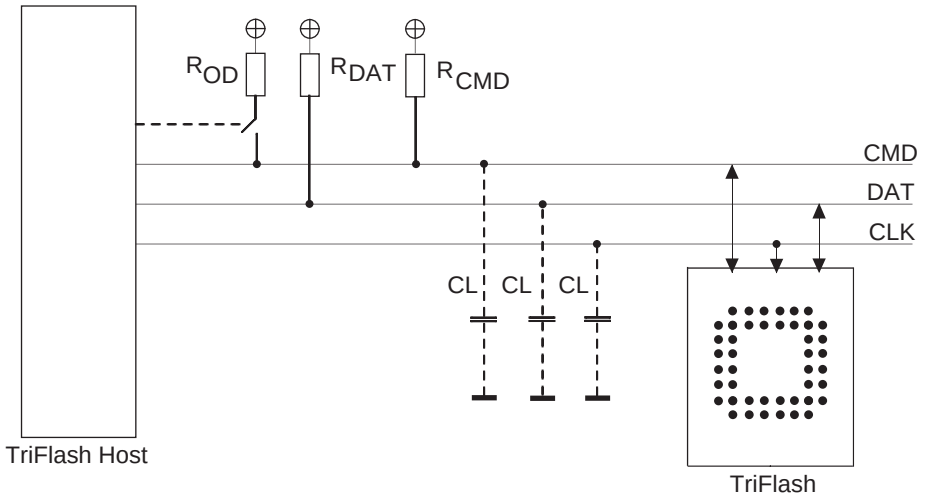

Figure 3-1. MultiMediaCard Bus Circuitry Diagram

The R_{OD} is switched on and off by the host synchronously to the open-drain and push-pull mode transitions. R_{DAT} and R_{CMD} are pull-up resistors protecting the CMD and the DAT line against bus floating when all device drivers are in a hi-impedance mode.

A constant current source can replace the R_{OD} in order to achieve better performance (constant slopes for the signal rising and falling edges). If the host does not allow the switchable R_{OD} implementation, a fix R_{CMD} can be used. Consequently the maximum operating frequency in the open drain mode has to be reduced in this case.

3.3. SPI Bus Topology

The TriFlash SPI interface is compatible with SPI hosts available on the market. As with any other SPI device the TriFlash SPI channel consists of the following four signals:

- **CS**—Host to device Chip Select signal.
- **CLK**—Host to device clock signal
- **DataIn**—Host to device data signal.
- **DataOut**—Device to host data signal.

Another SPI common characteristic, which is implemented in the MultiMediaCard bus as well, is byte transfers. All data tokens are multiples of 8 bit bytes and always byte aligned to the CS signal.

The SPI standard defines the physical link only and not the complete data transfer protocol. In SPI Bus mode, the TriFlash uses a subset of the MultiMediaCard protocol and command set.

The TriFlash identification and addressing algorithms are replaced by a hardware Chip Select (CS) signal. A device (slave) is selected, for every command, by asserting (active low) the CS signal (see Figure 3-2).

The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception is device programming time. At this time the host can de-assert the CS signal without affecting the programming process.

The bi-directional CMD and DAT lines are replaced by unidirectional DataIn and DataOut signals. This eliminates the ability of executing commands while data is being read or written. An exception is the multi read/write operations. The Stop Transmission command can be sent during data read. In the multi block write operation a Stop Transmission token is sent as the first byte of the data block.

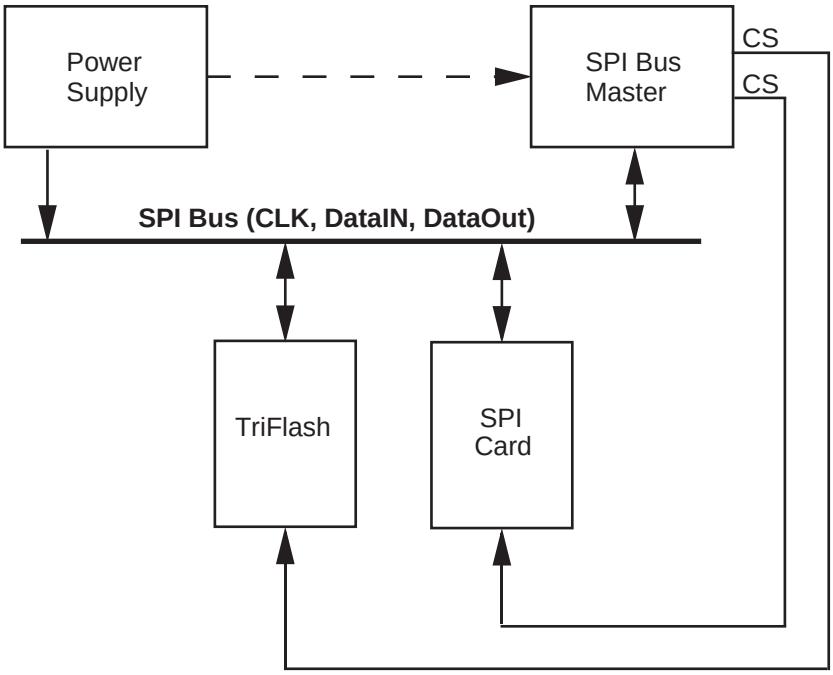

Figure 3-2. SPI Bus System

3.4. Electrical Interface

The following sections provide valuable information for TriFlash's electrical interface.

3.4.1. Power-up

The power up of the bus is handled locally in each TriFlash and in the bus master.

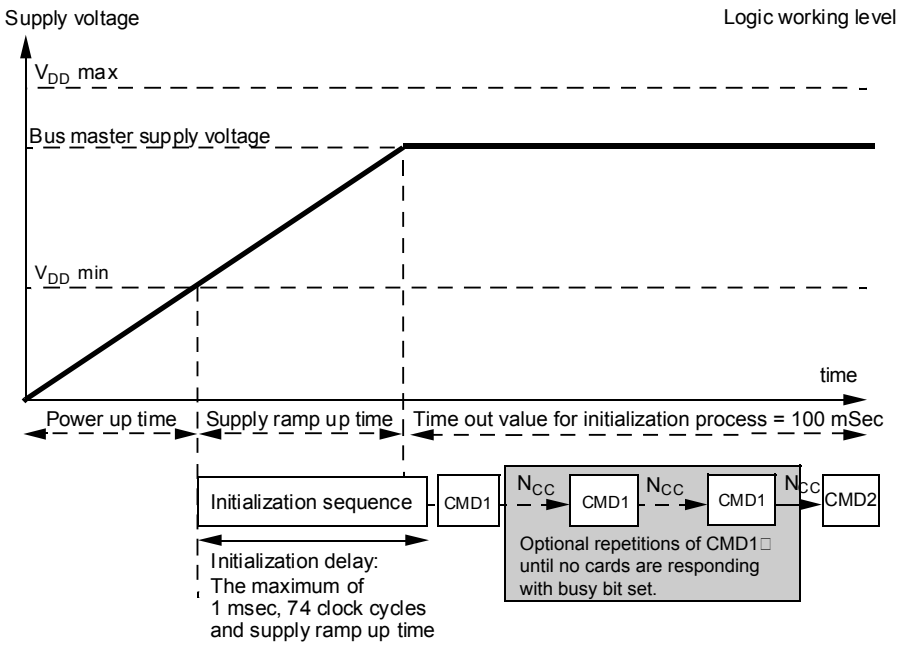

Figure 3-3. Power-up Diagram

After power up the TriFlash enters the *idle state*. During this state the TriFlash ignores all bus transactions until CMD1 is received.

CMD1 is a special synchronization command used to negotiate the operation voltage range and to poll the devices until they are out of their power-up sequence. Besides the operation voltage profile of the devices, the response to CMD1 contains a busy flag, indicating that the device is still working on its power-up procedure and is not ready for identification. This bit informs the host that at least one device is not ready. The host has to wait (and continue to poll the devices) until this bit is cleared. The TriFlash shall complete its initialization procedure within 500msec.

Getting individual devices, as well as the whole TriFlash system, out of *idle state* is the responsibility of the bus master. Since the power up time and the supply ramp up time depend on application parameters such as the maximum number of devices, the bus length and the power supply unit, the host must ensure that the power is built up to the operating level (the same level which will be specified in CMD1) before CMD1 is transmitted.

After power up, the host starts the clock and sends the initialising sequence on the CMD line. This sequence is a contiguous stream of logical ‘1’s. The sequence length is the maximum of 1msec, 74 clocks or the supply ramp-up time. The additional 10 clocks (over the 64 clocks after what the device should be ready for communication) are provided to eliminate power-up synchronization problems.

3.4.2. Bus Operating Conditions

SPI Mode bus operating conditions are identical to MultiMediaCard mode bus operating conditions. The chip select (CS) signal timing is identical to the input signal timing (see Figure 3-5).

Table 3-4. Power Supply Voltage

General					
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**	**Remark**
Peak voltage on all lines		-0.3	VDD+0.3	V	
All Inputs					
Input Leakage Current		-10	10	µA	
All Outputs					
Output Leakage Current		-10	10	µA	
Power Supply Voltage					
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**	**Remark**
Supply Voltage	V_{DD}	2.7	3.6	V	
Supply voltage differentials (V_{SS1}, V_{SS2})		-0.3	0.3	V	
Power up Time			250	mS	From 0V to V_{DD} Min.

Bus Signal Line Load

The total capacitance CL of the CLK line of the bus is the sum of the bus master capacitance CHOST, the bus capacitance CBUS itself and the capacitance C_{DEV} of each device connected to this line:

$$CL = CHOST + CBUS + N*C_{DEV}$$

Where N is the number of connected devices. Requiring the sum of the host and bus capacitances not to exceed 30 pF for up to 10 devices, and 40 pF for up to 30 devices, the values in Table 3-5 must not be exceeded.

Table 3-5. Signal Line's Load

Parameter	Symbol	Min.	Max.	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	kΩ	To prevent bus floating
Bus signal line capacitance	C_L		250	pF	$f_{PP} \leq 5$ MHz, 21 devices
Bus signal line capacitance	C_L		100	pF	$f_{PP} \leq 20$ MHz, 7 devices
Single device capacitance	C_{DEV}		10	pF	
Maximum signal line inductance			16	nH	$f_{PP} \leq 20$ MHz
Pull-up resistance inside device (pin 1)	R_{DAT3}	10	90	kΩ	May be used for device detection.

3.4.3. Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

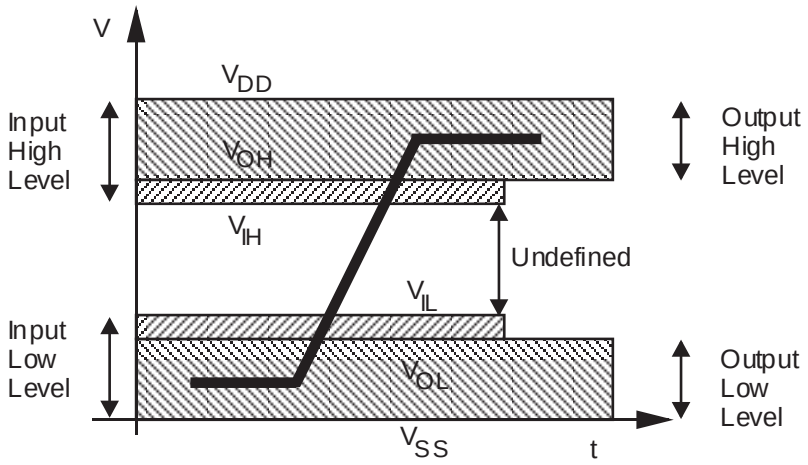

Figure 3-4. Bus Signal Levels

To meet the requirements of the JEDEC specification JESD8-1A, the device input and output voltages shall be within the specified ranges in Table 3-6 for any VDD of the allowed voltage range.

Table 3-6. Input and Output Voltages

Parameter	Symbol	Min.	Max.	Unit	Conditions
Output HIGH voltage	VOH	0.75∗VDD		V	IOH=-100 µA @V_{DD} (min.)
Output LOW voltage	VOL		0.125∗VDD	V	IOL=100 µA @V_{DD} (min.)
Input HIGH voltage	VIH	0.625∗VDD	VDD + 0.3	V	
Input LOW voltage	VIL	VSS-0.3	0.25∗VDD	V	

3.4.4. Bus Timing

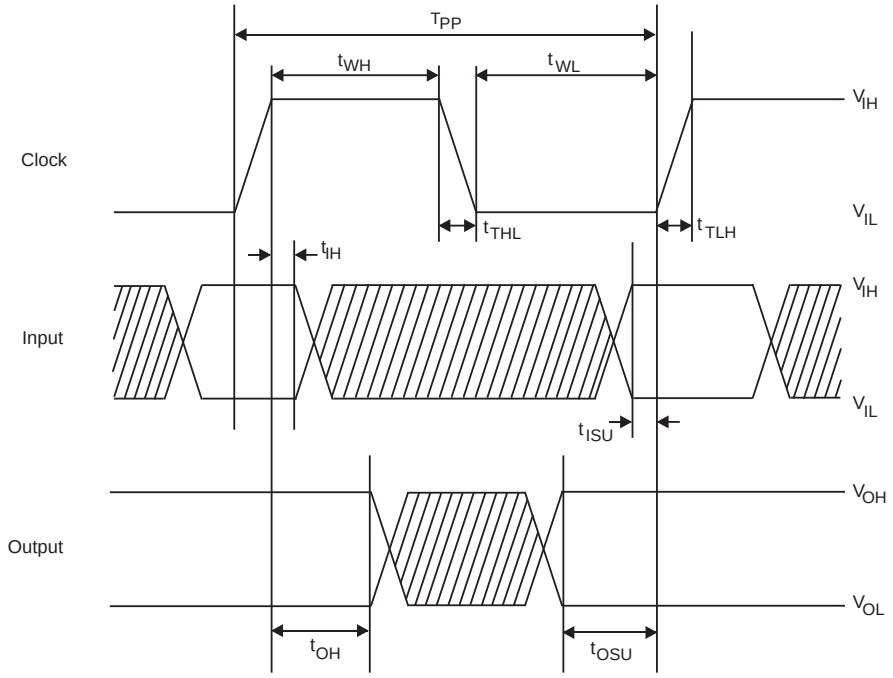

Figure 3-5. Timing Diagram Data Input/Output Referenced to Clock

Table 3-7. Bus Timing

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min. (V_{IH}) and max. (V_{IL})					
Clock Frequency Data Transfer Mode (PP)	f_{PP}	0	20	MHz	$C_L \leq 100$ pF (10 devices)
Clock Frequency Identification Mode (OD)	f_{OD}	0	400	kHz	$C_L \leq 250$ pF (30 devices)
Clock Low Time	t_{WL}	10		ns	$C_L \leq 100$ pF (10 devices)
Clock High Time	t_{WH}	10		ns	$C_L \leq 100$ pF (10 devices)
Clock Rise Time	t_{TLH}		10	ns	$C_L \leq 100$ pF (10 devices)
Clock Fall Time	t_{THL}		10	ns	$C_L \leq 100$ pF (10 devices)
Clock Low Time	t_{WL}	50		ns	$C_L \leq 250$ pF (30 devices)
Clock High Time	t_{WH}	50		ns	$C_L \leq 250$ pF (30 devices)
Clock Rise Time	t_{TLH}		50	ns	$C_L \leq 250$ pF (30 devices)

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock Fall Time	t_{THL}		50	ns	$C_L \leq 250$ pF (30 devices)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	
Input hold time	t_{IH}	3		ns	
Outputs CMD, DAT (referenced to CLK)					
Output set-up time	t_{OSU}	5		ns	
Output hold time	t_{OH}	5		ns	

3.4.5. TriFlash-Specific Functions

The following sections list the TriFlash-specific functions.

3.4.5.1. Ready/Busy Function [Output]

The RDY/BSY pin indicates ”0” if the TriFlash is in “Busy” condition. Busy condition is a period where the data paths of the TriFlash are not ready to get new data. The Busy condition, as defined in the MultiMediaCard Specification, may occur after or within the block transfer of any write or erase operations. After a host command is sent, the host shall expect to get a Busy indication in any case that response of type R1b is expected. The RDY/BSY_B indication is basically the same as the Busy indication that is indicated by DAT0 (as given in the MultiMediaCard Specification).

3.4.5.2. Write Protect Function [Input + Pullup]

This line shall be set to “0” (or maximum 10KOhm pull down resistor) in order to eliminate any write operations to the TriFlash memory. An attempt to write to the TriFlash in that condition will set the WP_VIOLATION status bit (bit [26] in the Card Status).

3.4.5.3. Reset Function [Input + Pullup]

If input is set to “0” (or maximum 10KOhm pull down resistor) it will force a Hardware RESET to the TriFlash.

3.5. TriFlash Registers

The device interface contains a set of four registers. The OCR, CID and CSD registers carry the device configuration information. The RCA register holds the device-relative communication address for the current session.

3.5.1. Operating Conditions Register (OCR)

The 32-bit OCR register stores the V_{DD} voltage profile of the device. The TriFlash is capable of executing the voltage recognition procedure (CMD1) with any standard TriFlash host using operating voltages from 2 to 3.6 Volts. Accessing the data in the memory array, however, requires 2.7 to 3.6 Volts. The OCR shows the voltage range in which the device data can be accessed. The structure of the OCR register is described in Table 3-8.

Table 3-8. OCR Register Definition

OCR Bit	VDD Voltage Window
0-7	Reserved
8	2.0-2.1
9	2.1-2.2
10	2.2-2.3
11	2.3-2.4
12	2.4-2.5
13	2.5-2.6
14	2.6-2.7
15	2.7-2.8
16	2.8-2.9
17	2.9-3.0
18	3.0-3.1
19	3.1-3.2
20	3.2-3.3
21	3.3-3.4
22	3.4-3.5
23	3.5-3.6
24-30	Reserved
31	Device power up status bit (busy)

The level coding of the OCR register is as follows:

- Restricted voltage windows=LOW
- Device busy=LOW (bit 31)

The least significant 31 bits are constant and will be set as described in Figure 3-6. If set, bit 32, the busy bit, informs the host that the device power up procedure is finished.

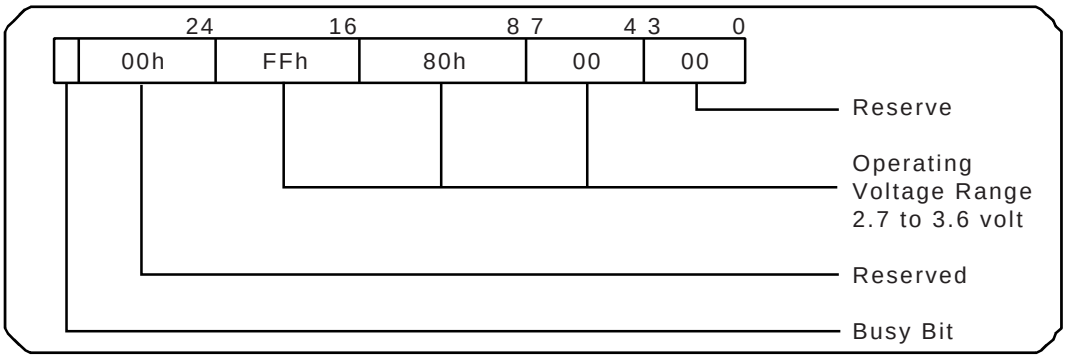

Figure 3-6. OCR Structure

3.5.2. Card Identification (CID) Register

The CID register is 16 bytes long and contains a unique device identification number as shown in Table 3-9. It is programmed during device manufacturing and cannot be changed by TriFlash hosts.

Table 3-9. CID Fields

Name	Type	Width	CID—Slice	CID—Value	Comments
Manufacturer ID (MID)	Binary	8	[127:120]	0x02	The manufacturer IDs are controlled and assigned by the MultiMediaCard Association.
OEM/Application ID (OID)	Binary	16	[119:104]	0x0000	Identifies the device OEM and/or the device contents. The OID is assigned by the MMCA. This field may be specifically configured for OEM customers.
Product Name (PNM)	String	48	[103:56]	See footnote[1]	6 ASCII characters long.
Product Revision (PRV)	BCD	8	[55:48]	See footnote[2]	Two binary coded decimal digits.
Serial Number (PSN)	Binary	32	[47:16]		32 Bits unsigned integer.
Manufacturing Date Code (MDT)	BCD	8	[15:8]	See footnote[3]	Manufacturing date–mm/yy (offset from 1997).
CRC7 checksum (CRC)	Binary	7	[7:1]	See footnote[4]	Calculated.
Not used, always '1'		1	[0:0]		

[1] Model Name — Name in CD Field
SDAT1FAH-128 — STM016
SDBT1FAH-256 — STM032
SDBT1FCH-512 — STM064
SDBT1FCH-1024 — STM128

[2] The product revision is composed of two Binary Coded Decimal (BCD) digits, four bits each, representing an "n.m" revision number. The "n" is the most significant nibble and the "m" is the least significant nibble. Example: The PRV binary value filed for product revision "6.2" will be: 0110 0010.

[3] As an example, this field value for a March 2001 manufacturing date will be: 0011 0100.

[4] The CRC Checksum is computed by the following formula:
CRC Calculation: G(x)=x7+3+1
M(x)=(MID-MSB)*x119+...+(CIN-LSB)*x0
CRC[6...0]=Remainder[(M(x)*x7)/G(x)]

3.5.3. Card Specific Data (CSD) Register

The CSD register contains all the configuration information required in order to access the device data. In Table 3-10, the Cell Type column defines the CSD field as Read only (R), One Time Programmable (R/W) or erasable (R/W/E). This table shows, for each field, the value in "real world" units and coded according to the CSD structure. The Model Dependent column marks (with a check mark—√) the CSD fields that are model dependent.

Table 3-10. CSD Register

Field	Width [bits]	Cell Type	CSD-slice	CSD Value	CSD Code	Model Dep.	Description
CSD_STRUCTURE	2	R	[127:126]	V1.1	1		CSD Structure
SPEC_VERS	4	R	[125:122]	V2.2	2		MultiMediaCard Specification Version
-	2	R	[121:120]	0	0		Reserved
TAAC Binary MLC	 8 8	 R R	 [119:112] [119:112]	 1.5msec 10msec	 0x0F 0x0F		 Data Read Access-Time-1 Data Read Access-Time-1
NSAC	8	R	[111:104]	0	0		Data Read Access-Time-2 in CLK Cycles (NSAC*100)
TRAN_SPEED	8	R	[103:96]	20MHZ	0x2A		Max. Data Transfer Rate
CCC	12	R	[95:84]	See note[1]	0x0F5		Card Command Classes
READ_BL_LEN	4	R	[83:80]	512	9		Max. Read Data Block Length
READ_BL_PARTIAL	1	R	[79:79]	Yes	1		Partial Blocks for Read Allowed
WRITE_BLK_MISALIGN	1	R	[78:78]	No	0		Write Block Misalignment
READ_BLK_MISALIGN	1	R	[77:77]	No	0		Read Block Misalignment
DSR_IMP	1	R	[76:76]	No	0		DSR Implemented
-	2	R	[75:74]	0	0		Reserved
C_SIZE	12	R	[73:62]			√	Device Size (C_SIZE)
VDD_R_CURR_MIN	3	R	[61:59]	60mA	6		Max. Read Current @V_{DD} Min.
VDD_R_CURR_MAX	3	R	[58:56]	80mA	6		Max. Read Current @V_{DD} Max.
VDD_W_CURR_MIN	3	R	[55:53]	60mA	6		Max. Write Current @V_{DD} Min.
VDD_W_CURR_MAX	3	R	[52:50]	80mA	6		Max. Write Current @V_{DD} Max.
C_SIZE_MULT	3	R	[49:47]			√	Device Size Multiplier (C_SIZE_MULT)
SECTOR_SIZE	5	R	[46:42]	1	0		Erase Sector Size
ERASE_GRP_SIZE	5	R	[41:37]			√	Erase Group Size
WP_GRP_SIZE	5	R	[36:32]	32	0x1F		Write Protect Group Size
WP_GRP_ENABLE	1	R	[31:31]	Yes	1		Write Protect Group Enable
DEFAULT_ECC	2	R	[30:29]	None	0		Manufacturer Default ECC

[1] This SanDisk product does not support the following classes: I/O, application specific, stream write, and stream read.

Field	Width [bits]	Cell Type	CSD-slice	CSD Value	CSD Code	Model Dep.	Description
R2W_FACTOR Binary MLC	 3 3	 R R	 [28:26] [28:26]	 1:16 1:4	 2 2		 Read to Write Speed Factor Read to Write Speed Factor
WRITE_BL_LEN	4	R	[25:22]	512	9		Max. Write Data Block Length
WRITE_BL_PARTIAL	1	R	[21:21]	No	0		Partial Blocks for Write Allowed
-	5	R	[20:16]	0	0		Reserved
FILE_FORMAT_GRP	1	R/W	[15:15]	0	0		Indicates File Format of Selected Group
COPY	1	R/W	[14:14]	Copy	1		Copy Flag (OTP)
PERM_WRITE_PROTECT	1	R/W	[13:13]	No	0		Permanent Write Protection
TMP_WRITE_PROTECT	1	R/W/E	[12:12]	No	0		Temporary Write Protection
FILE_FORMAT	2	R/W	[11:10]	0	0		File Format of Card
ECC	2	R/W/E	[9:8]	None	0		ECC Code
CRC	7	R/W/E	[7:1]			√	CRC
-	1	-	[0:0]	1	1		Not Used, Always '1'

The following sections describe the CSD fields and the relevant data types. If not explicitly defined otherwise, all bit strings are interpreted as binary coded numbers starting with the left bit first.

CSD_STRUCTURE—describes the version of the CSD structure.

Table 3-11. CSD Register Structure

CSD_STRUCTURE	CSD Structure Version	Valid for MultiMediaCard Protocol Version
0	CSD version No. 1.0	MultiMediaCard protocol version 1.0–1.2
1	CSD version No. 1.1	MultiMediaCard protocol version 1.4–2.2
2—3	Reserved	Reserved

MMC_PROT—Defines the MultiMediaCard protocol version supported by the device. It includes the definition of the command set and the device responses. The card identification procedure is compatible for all protocol versions.

Table 3-12. MultiMediaCard Protocol Version

SPEC_VERS	MultiMediaCard Protocol Version
0	MultiMediaCard protocol version 1.0–1.2
1	MultiMediaCard protocol version 1.4
2	MultiMediaCard protocol version 2.0–2.2
3-15	Reserved

TAAC—Defines the asynchronous part (relative to the MultiMediaCard bus clock (CLK)) of the read access time.

Table 3-13. TAAC Access Time Definition

TAAC Bit Position	Code
2:0	time exponent 0=1ns, 1=10ns, 2=100ns, 3=1µms, 4=10µms, 5=100µms, 6=1ms, 7=10ms
6:3	time mantissa 0=Reserved, 1=1.0, 2=1.2, 3=1.3, 4=1.5, 5=2.0, 6=2.5, 7=3.0, 8=3.5, 9=4.0, A=4.5, B=5.0, C=5.5, D=6.0, E=7.0, F=8.0
7	Reserved

NSAC—Defines the worst case for the clock dependent factor of the data access time. The unit for NSAC is 100 clock cycles. Therefore, the maximal value for the clock dependent part of the read access time is 25.5k clock cycles.

The total read access time N_{AC} as expressed in the Table 3-14 is the sum of TAAC and NSAC. It has to be computed by the host for the actual clock rate. The read access time should be interpreted as a typical delay for the first data bit of a data block or stream from the end bit on the read commands.

TRAN_SPEED—Table 3-14 defines the maximum data transfer rate TRAN_SPEED.

Table 3-14. Maximum Data Transfer Rate Definition

TRAN_SPEED Bit	Code
2:0	transfer rate exponent 0=100kbit/s, 1=1Mbit/s, 2=10Mbit/s, 3=100Mbit/s, 4... 7=Reserved
6:3	time mantissa 0=Reserved, 1=1.0, 2=1.2, 3=1.3, 4=1.5, 5=2.0, 6=2.5, 7=3.0, 8=3.5, 9=4.0, A=4.5, B=5.0, C=5.5, D=6.0, E=7.0, F=8.0
7	Reserved

CCC—The TriFlash command set is divided into subsets (command classes). The card command class register CCC defines which command classes are supported by this device. A value of '1' in a CCC bit means that the corresponding command class is supported. For an explanation of command classes, see Section 4.6.3.

Table 3-15. Supported Card Command Classes

CCC Bit	Supported Card Command Class
0	class 0
1	class 1
.....	
11	class 11

READ_BL_LEN—The data block length is computed as $2^{READ\_BL\_LEN}$. The block length might therefore be in the range 1, 2, 4...2048 bytes.

Table 3-16. Data Block Length

READ_BL_LEN	Block Length
0	2^0 = 1 Byte
1	2^1 = 2 Bytes
.....	
11	2^{11} = 2048 Bytes
12-15	Reserved

READ_BL_PARTIAL—Defines whether partial block sizes can be used in block read commands.

READ_BL_PARTIAL=0 means that only the READ_BL_LEN block size can be used for block-oriented data transfers.

READ_BL_PARTIAL=1 means that smaller blocks can be used as well. The minimum block size will be equal to minimum addressable unit (one byte).

WRITE_BLK_MISALIGN—Defines if the data block to be written by one command can be spread over more than one physical block of the memory device. The size of the memory block is defined in WRITE_BL_LEN.

WRITE_BLK_MISALIGN=0 signals that crossing physical block boundaries is invalid.

WRITE_BLK_MISALIGN=1 signals that crossing physical block boundaries is allowed.

READ_BLK_MISALIGN—Defines if the data block to be read by one command can be spread over more than one physical block of the memory device. The size of the memory block is defined in READ_BL_LEN.

READ_BLK_MISALIGN=0 signals that crossing physical block boundaries is invalid.

READ_BLK_MISALIGN=1 signals that crossing physical block boundaries is allowed.

DSR_IMP—Defines if the configurable driver stage is integrated on the device. If set, a driver stage register (DSR) must be implemented also.

Table 3-17. DSR Implementation Code Table

DSR_IMP	DSR Type
0	No DSR implemented
1	DSR implemented

C_SIZE (Device Size)—This parameter is used to compute the device capacity. The memory capacity of the device is computed from the entries C_SIZE, C_SIZE_MULT and READ_BL_LEN as follows:

memory capacity = BLOCKNR * BLOCK_LEN

where:

BLOCKNR = (C_SIZE+1) * MULT
MULT = $2^{C\_SIZE\_MULT+2}$ (C_SIZE_MULT < 8)
BLOCK_LEN = $2^{READ\_BL\_LEN}$ (READ_BL_LEN < 12)

Therefore, the maximum capacity that can be coded is 4096*512*2048 = 4GBytes. Example: A four MByte device with BLOCK_LEN = 512 can be coded with C_SIZE_MULT = 0 and C_SIZE = 2047.

VDD_R_CURR_MIN, VDD_W_CURR_MIN—The minimum values for read and write currents on VDD power supply are coded shown in Table 3-18.

Table 3-18. V_{DD} Minimum Current Consumption

VDD_R_CURR_MIN VDD_W_CURR_MIN	Code For Current Consumption @ V_{DD}
2:0	0=0.5mA; 1=1mA; 2=5mA; 3=10mA; 4=25mA; 5=35mA; 6=60mA; 7=100mA

VDD_R_CURR_MAX, VDD_W_CURR_MAX—The maximum values for read and write currents on VDD power supply are coded as shown in Table 3-19.

Table 3-19. V_{DD} Maximum Current Consumption

VDD_R_CURR_MAX VDD_W_CURR_MAX	Code For Current Consumption @ V_{DD}
2:0	0=1mA; 1=5mA; 2=10mA; 3=25mA; 4=35mA; 5=45mA; 6=80mA; 7=200mA

C_SIZE_MULT (Device Size Multiplier)—This parameter is used for coding a factor MULT for computing the total device size (see 'C_SIZE'). The factor MULT is defined as $2^{C\_SIZE\_MULT+2}$.

Table 3-20. Multiply for the Device Size

C_SIZE_MULT	MULT
0	$2^2 = 4$
1	$2^3 = 8$
2	$2^4 = 16$
3	$2^5 = 32$
4	$2^6 = 64$
5	$2^7 = 128$
6	$2^8 = 256$
7	$2^9 = 512$

SECTOR_SIZE—The size of an erasable sector. The content of this register is a 5-bit binary coded value, defining the number of write blocks (see WRITE_BL_LEN). The actual size is computed by increasing this number by one. A value of zero means 1 write block, 31 means 32 blocks.

ERASE_GRP_SIZE—The size of an erasable group. The content of this register is a 5-bit binary coded value, defining the number of sectors (see SECTOR_SIZE). The actual size is computed by increasing this number by one. A value of zero means 1 sector, 31 means 32 sectors.

WP_GRP_SIZE—The size of a write protected group. The content of this register is a 5-bit binary coded value, defining the number of Erase Groups (see ERASE_GRP_SIZE). The actual size is computed by increasing this number by one. A value of zero means 1 erase group, 31 means 32 erase groups.

WP_GRP_ENABLE—A value of '0' means no group write protection possible.

DEFAULT_ECC—Set by the device manufacturer. It defines the ECC code that is recommended for use. The field definition is the same as for the ECC field described later.

R2W_FACTOR—Defines the typical block program time as a multiple of the read access time. Table 3-21 defines the field format.

Table 3-21. R2W_FACTOR

R2W_FACTOR	Multiples of Read Access Time
0	1
1	2 (write half as fast as read)
2	4
3	8
4	16
5	32
6,7	Reserved

WRITE_BL_LEN—Block length for write operations. See READ_BL_LEN for field coding.

WRITE_BL_PARTIAL—Defines whether partial block sizes can be used in block write commands.

WRITE_BL_PARTIAL='0' means that only the WRITE_BL_LEN block size can be used for block oriented data write.

WRITE_BL_PARTIAL='1' means that smaller blocks can be used as well. The minimum block size is one byte.

FILE_FORMAT_GROUP—Indicates the selected group of file formats. This field is read-only for ROM. The usage of this field is shown in Table 3-22.

Table 3-22. FILE_FORMAT

FILE_FORMAT_GRP	FILE_FORMAT	Type
0	0	Hard disk-like file system with partition table
0	1	DOS FAT (floppy-like) with boot sector only (no partition table)
0	2	Universal File Format
0	3	Others/Unknown
1	0, 1, 2, 3	Reserved

COPY—This bit marks the device as an original (‘0’) or a copy (‘1’). Once set to copy, this bit cannot be reset to original. The definition of “original” and “copy” is application dependent and changes no device characteristics.

PERM_WRITE_PROTECT—Permanently protects the whole device content against overwriting or erasing (all write and erase commands for this device are permanently disabled). The default value is ‘0’, i.e., not permanently write protected.

TMP_WRITE_PROTECT—Temporarily protects the whole device content from being overwritten or erased (all write and erase commands for this device are temporarily disabled). This bit can be set and reset. The default value is ‘0’, i.e., not write protected.

FILE_FORMAT—Indicates the file format on the device. This field is read-only for ROM. The following formats are defined.

ECC—Defines the ECC code that was used for storing data on the device. This field is used by the host (or application) to decode the user data. Table 3-22 defines the field format.

Table 3-23. ECC Type

ECC	ECC Type	Maximum Number Of Correctable Bits Per Block
0	none (default)	none
1	BCH (542,512)	3
2-3	Reserved	-

CRC—The CRC field carries the checksum for the CSD contents. The checksum has to be recalculated by the host for any CSD modification. The default corresponds to the initial CSD contents.

3.5.4. Status Register

The TriFlash Status register structure is defined in the following table. The Type and Clear-Condition fields in the table are coded as follows:

Type:

- **E**—Error bit.
- **S**—Status bit.
- **R**—Detected and set for the actual command response.
- **X**—Detected and set during command execution. The host must poll the device by sending status command in order to read these bits.

Clear Condition:

- **A**—According to the device current state.
- **B**—Always related to the previous command. Reception of a valid command will clear it (with a delay of one command).
- **C**—Clear by read.

Table 3-24. Status Register

Bits	Identifier	Type	Value	Description	Clear Condition
31	OUT_OF_RANGE	E R	'0'= no error '1'= error	The commands argument was out of allowed range for this device.	C
30	ADDRESS_ERROR	E R X	'0'= no error '1'= error	A misaligned address, which did not match the block length was used in the command.	C
29	BLOCK_LEN_ERROR	E R	'0'= no error '1'= error	The transferred block length is not valid.	C
28	ERASE_SEQ_ERROR	E R	'0'= no error '1'= error	An error in the sequence of erase commands occurred.	C
27	ERASE_PARAM	E X	'0'= no error '1'= error	An invalid selection, sectors or groups, for erase.	C
26	WP_VIOLATION	E R X	'0'= not protected '1'= protected	The command tried to write a write-protected block.	C
25-24	Not applicable. This bit is always set to '0'.				
23	COM_CRC_ERROR	E R	'0'= no error '1'= error	The CRC check of the previous command failed.	B
22	ILLEGAL_COMMAND	E R	'0'= no error '1'= error	Command not legal for the current state	B
21-20	Not applicable. This bit is always set to '0'.				
19	ERROR	E R X	'0'= no error '1'= error	A general or an unknown error occurred during the operation.	C
18	Not applicable. This bit is always set to '0'.				
17	Not applicable. This bit is always set to '0'.				
16	CID/CSD_OVERWRITE	E R X	'0'= no error '1'= error	Can be one of the following errors: - The CID register has been already written and cannot be overwritten. - The read only section of the CSD does not match the device content. - An attempt to reverse the copy (set as original) or permanent WP (unprotect) bits was made.	C
15	WP_ERASE_SKIP	S X	'0'= not protected '1'= protected	Only partial address space was erased due to existing WP blocks.	C
14	Not applicable. This bit is always set to '0'.				
13	ERASE_RESET	S R	'0'= cleared '1'= set	An erase sequence was cleared before executing because an out of erase sequence command was received	C

Bits	Identifier	Type	Value	Description	Clear Condition
12-9	CURRENT_STATE	S X	0 = idle 1 = ready 2 = ident 3 = stby 4 = tran 5 = data 6 = rcv 7 = prg 8 = dis 9-15 = Reserved	The state of the device when the command was received. If the command execution causes a state change, it will be visible to the host in the response to the next command. The four bits are interpreted as a binary coded number between 0 and 15.	B
8	READY_FOR_DATA	S X	'0'= not ready '1'= ready	Corresponds to buffer empty signaling on the bus. (RDY/BSY)	A
7-0	Reserved. Always set to '0'.				

3.5.5. Relative Card Address (RCA) Register

The 16-bit RCA register carries the device address assigned by the host during the card identification. This address is used for the addressed host-device communication after the card identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all devices in Stand-by State with CMD7.

3.5.6. TriFlash Registers in SPI Mode

In SPI mode, only the CSD and CID registers are accessible. Their format is identical to the format in the MultiMediaCard mode; however, a few fields are irrelevant in SPI mode (refer to Table 3-25).

In SPI mode, the device status register has a different, shorter format as well. Refer to the SPI Protocol section for more details.

Table 3-25. TriFlash Registers in SPI Mode

Name	Available in SPI Mode	Width (Bytes)	Description
CID	Yes	16	Card identification data (serial number, manufacturer ID etc.)
RCA	No		
DSR	No		
CSD	Yes	16	Card specific data, information about the device operation conditions.
OCR	No		

3.6. File System Format

The TriFlash devices with MultiMediaCard Interface are formatted with a "hard disk-like" partitioned DOS FAT file system. Similar to hard disks in PCs, the first data block of the memory consists of a partition table. Thus, using the same notation as for hard disks (i.e., partitioning the memory field into logical sectors of 512 bytes each), the first sector is reserved for this partition table. Table 3-26 shows how the data in this sector is structured.

Table 3-26. Partition Table for Hard Disk-like File System

Byte Position	Length (bytes)	Entry Description	Value/Range
0x0	446	Consistency Check Routine	
0x1be	16	Partition Table Entry	(See below.)
0x1ce	16	Partition Table Entry	(See below.)
0x1de	16	Partition Table Entry	(See below.)
0x1ee	16	Partition Table Entry	(See below.)
0x1fe	1	Signature	'0x55'
0x1ff	1	Signature	'0xaa'

Every partition entry consists of the fields shown in Table 3-27.

Table 3-27. Partition Entry Description

Byte Position	Length (Bytes)	Entry Description	Value/Range
0x0	1	Boot Descriptor	0x00 (Unbootable Device), 0x80 (Bootable Device)
0x1	3	First Partition Sector	Address of First Sector
0x4	1	File System Descriptor	0 = Empty 1 = DOS 12-bit FAT < 16 MB 4 = DOS 16-bit FAT < 32 MB 5 = Extended DOS 6 = DOS 16-bit FAT >= 32 MB 0x10-0xff = Free for other File Systems*
0x5	3	Last Partition Sector	Address of Last Sector
0x8	4	First Sector Position Relative to Beginning of Device	Number of First Sector (Linear Address)
0xc	4	Number of Sectors in Partition	Between one and Maximum Number of Sectors on Device

The descriptors marked by an asterisk are not used in DOS systems. Every DOS partition is based on a 12-bit, 16-bit FAT or VFAT respectively. All sector numbers are stored in Little-Endian format (least significant byte first). The start and end addresses of the partition are given in terms of heads, tracks and sectors, and can therefore be ignored for the TriFlash, since the position of the partition can be determined by the last two entries.

The boot sector is described in Table 3-28.

Table 3-28. Boot Sector Configuration

Byte Position	Length (Bytes)	Entry Description	Value/Range
0x0	3	Jump Command	0xeb 0xXX 0x90
0x3	8	OEM Name	XXX
0xb	2	Bytes/Sector	512
0xd	1	Sectors/Cluster	XXX (range: 1—64)
0xe	2	Reserved Sectors (Number of reserved sectors at the beginning of the media including the boot	1

Byte Position	Length (Bytes)	Entry Description	Value/Range
		sector.)	
0x10	1	Number of FATs	2
0x11	2	Number of Root Directory Entries	512
0x13	2	Number of Sectors on Media	XXX (Depends on card capacity, if the media has more than 65535 sectors, this field is zero and the 'number of total sectors' is set.)
0x15	1	Media Descriptor	0xf8 (Hard Disk)
0x16	2	Sectors/FAT	XXX
0x18	2	Sectors/Track	32 (No Meaning)
0x1a	2	Number of Heads	2 (No Meaning)
0x1c	4	Number of Hidden Sectors	0
0x20	4	Number of Total Sectors	XXX (Depends on Capacity)
0x24	1	Drive Number	0x80
0x25	1	Reserved	0
0x26	1	Extended Boot Signature	0x29
0x27	4	Volume ID or Serial Number	XXX
0x2b	11	Volume Label	XXX (ASCII characters padded with blanks if less than 11 characters.)
0x36	8	File System Type	XXX (ASCII characters identifying the file system type FAT12 or FAT16.)
0x3e	448	Load Program Code	XXX
0x1fe	1	Signature	0x55
0x1ff	1	Signature	0xaa

All 'X' entries are denoting card dependent or unfixed values. The number of sectors per track and the number of heads are meaningless for the TriFlash and can be ignored.

4. MultiMediaCard Protocol Description

All communication between the host and TriFlash devices is controlled by the host (master). The host sends commands of two types: broadcast and addressed (point-to-point) commands.

- Broadcast Commands.
- Broadcast commands are intended for all TriFlash devices and MultiMediaCards. Some of these commands require a response.
- Addressed (Point-to-Point) Commands
- The addressed commands are sent to the addressed TriFlash and cause a response from this device.

A general overview of the command flow is shown in Figure 4-1 for the Device Identification Mode and in Figure 4-2 for the Data Transfer Mode. The commands are listed in the command tables (Table 4-3 to Table 4-11). The dependencies between the current TriFlash state, received command and following state are listed in Table 4-12. In the following sections, the different device operation modes will be described first. Thereafter, the restrictions for controlling the clock signal are defined. All MultiMediaCard bus commands together with the corresponding responses, state transitions, error conditions and timings are presented in the following sections.

Three operation modes are defined for TriFlash devices using the MultiMediaCard bus:

- **Card Identification Mode**—The host will be in card identification mode after reset and while it is looking for new devices on the bus. TriFlash devices will be in this mode after reset until the SET_RCA command (CMD3) is received.
- **Interrupt Mode**—The Interrupt Mode option defined in the MultiMediaCard Standard is not implemented on the SanDisk TriFlash.
- **Data Transfer Mode**—TriFlash devices will enter data transfer mode once an RCA is assigned to them. The host will enter data transfer mode after identifying all the TriFlash devices on the bus.

Table 4-1 shows the dependencies between bus modes, operation modes and device states. Each state in the TriFlash state diagrams (Figure 4-1 and Figure 4-2) is associated with one bus mode and one operation mode.

Table 4-1. Bus Modes Overview

Device State	Operation Mode	Bus Mode
Inactive State	Inactive	
Idle State		
Ready State	Card Identification Mode	Open-Drain
Identification State		
Stand-by State		
Transfer State		
Sending-data State	Data Transfer Mode	Push-Pull
Receive-data State		
Programming State		
Disconnect State		

If a command with improper CRC was received, it is ignored. If there was a command execution (e.g., continuous data read) the device continues in the operation until it gets a correct host command.

4.1. Device Identification Mode

All the data communication in the Device Identification Mode uses only the command line (CMD).

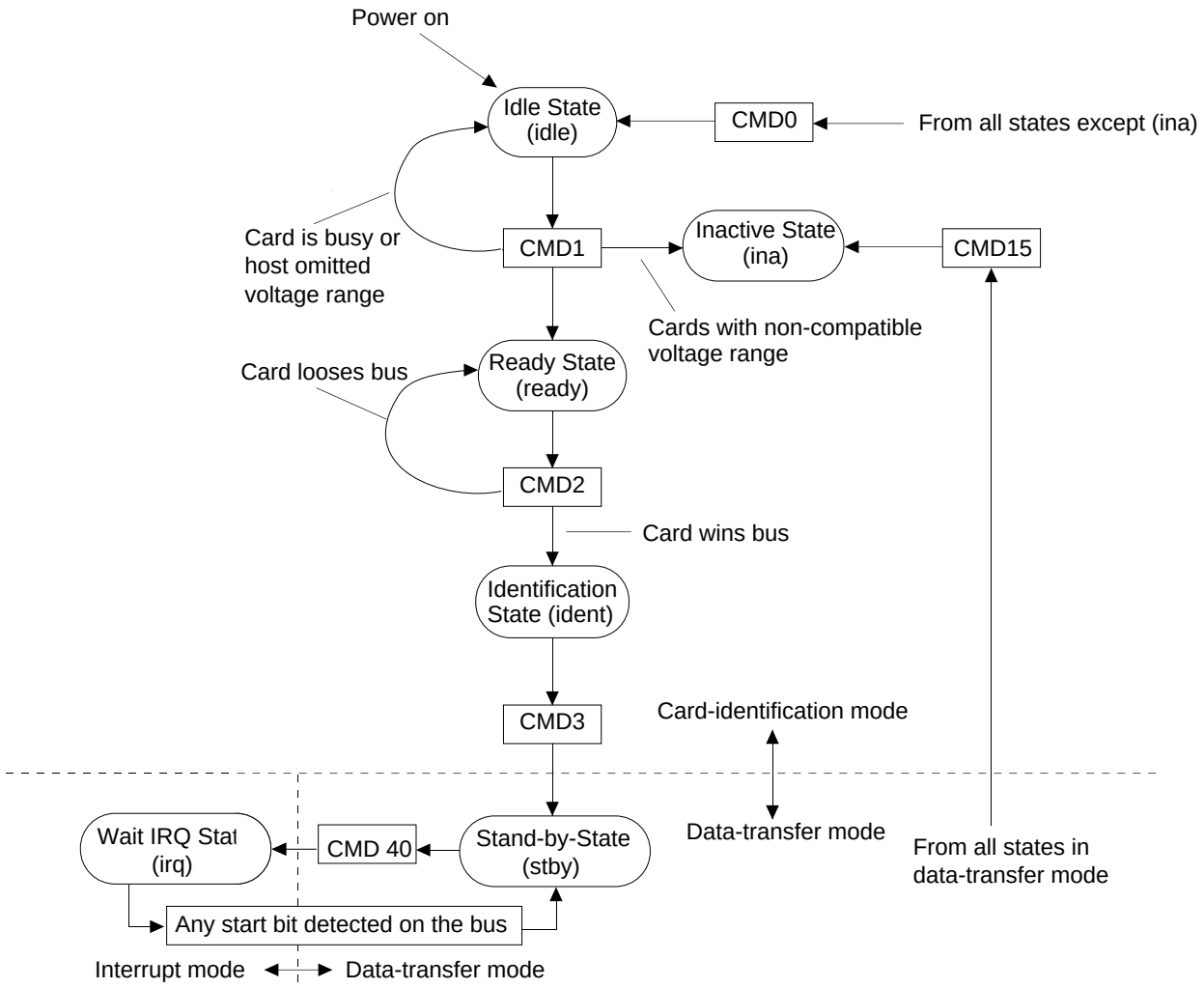

Figure 4-1. TriFlash State Diagram (Device Identification Mode)

4.1.1. Reset

GO_IDLE_STATE (CMD0) is the software reset command and sets all TriFlash devices to Idle State regardless of the current device state. Devices in Inactive State are not affected by this command.

After power-on by the host, all TriFlash devices are in Idle State, including the devices that were in Inactive State. Note that at least 74 clock cycles are required prior to starting bus communication.

After power-on or CMD0, all TriFlash devices' output bus drivers are in a high-impedance state. The host drives the bus at the identification clock rate f_{OD} (generated by a push-pull driver stage).

4.1.2. Operating Voltage Range Validation

Although not required, the TriFlash is compatible with the Operating Voltage Range Validation procedure used for the MultiMediaCard and will respond in the same way as the cards. The host must send CMD1 using the OCR value for the TriFlash defined in this manual. The busy bit in the CMD1 response can be used by a device to tell the host that it is still working on its power-up/reset procedure (e.g., downloading the register information from memory field) and is not ready yet for communication. In this case the host must repeat CMD1 until the busy bit is cleared.

During the initialization procedure, the host is not allowed to change the OCR values. Changes in the OCR content will be ignored by the TriFlash. If there is a real change in the operating conditions the host must reset the card stack (using CMD0) and begin the initialization procedure once more.

GO_INACTIVE_STATE (CMD15) can also be used to send an addressed TriFlash into the Inactive State. This command is used when the host explicitly wants to deactivate a device (e.g., host is changing V_{DD} into a range which is known to be not supported by this device).

4.1.3. Device Identification Process

The host starts the device identification process in open-drain mode with the identification clock rate f_{OD}. The open drain driver stages on the CMD line allow parallel device operation during card identification.

After the bus is activated and a valid operation condition is obtained, the host then asks all devices for their unique card identification (CID) number with the broadcast command ALL_SEND_CID (CMD2). All remaining unidentified devices (i.e., those which are in Ready State) simultaneously start sending their CID numbers serially, while bit-wise monitoring their outgoing bit stream. Those devices, whose outgoing CID bits do not match the corresponding bits on the command line in any one of the bit periods, stop sending their CID immediately and must wait for the next identification cycle (devices stay in the Ready State). Since CID numbers are unique for each TriFlash, there should be only one device that successfully sends its full CID-number to the host. This device then goes into Identification State. The host issues CMD3, (SET_RELATIVE_ADDR) to assign this device a relative address (RCA), which is shorter than CID and which will be used to address the device in future data transfer mode communication (typically with a higher clock rate than f_{OD}). Once the RCA is received the device transfers to the Stand-by State and does not react to further identification cycles. The TriFlash also switches its output drivers from open-drain to push-pull.

The host repeats the identification process as long as it receives a response (CID) to its identification command (CMD2). When no device responds to this command, all devices have been identified. The time-out condition to recognize completion is the absence of a start bit for more than 5 clock periods after sending CMD2.

4.2. Data Transfer Mode

When all devices are in Stand-by State, communication over the CMD and DAT lines will be in push-pull mode. Until the content of all CSD registers is known by the host, the f_{PP} clock rate must remain at f_{OD} because some devices may have operating frequency restrictions. The host issues SEND_CSD (CMD9) to obtain the CSD register, e.g., ECC type, block length, device storage capacity, maximum clock rate.

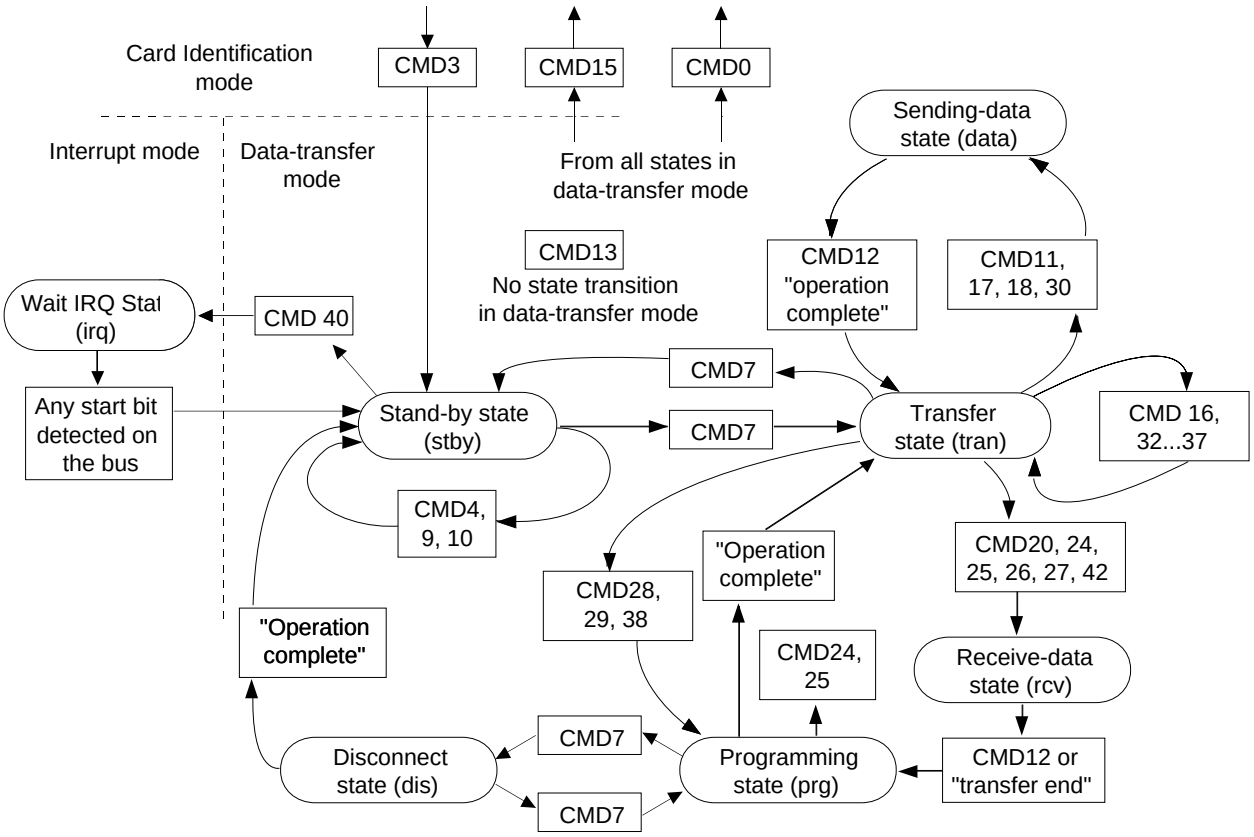

Figure 4-2. TriFlash State Diagram (Data Transfer Mode)

CMD7 is used to select one device and place it in the Transfer State. Only one TriFlash can be in the Transfer State at a given time. If a previously selected TriFlash or card is in the Transfer State, its connection with the host is released and it will move back to the Stand-by State. When CMD7 is issued with the reserved relative card address "0x0000," all devices transfer back to Stand-by State. This command is used to identify new devices without resetting other already acquired devices. TriFlash devices that already have an RCA do not respond to the identification command flow in this state.

All data communication in the Data Transfer Mode is point-to point between the host and the selected TriFlash (using addressed commands). All addressed commands are acknowledged with a response on the CMD line.

The relationship between the various data transfer modes is summarized in the state diagram Figure 4-2, and in the following paragraphs:

- All data read commands can be aborted any time by the stop command (CMD12). The data transfer will terminate and the TriFlash will return to the Transfer State. The read commands are: block read (CMD17), multiple block read (CMD18) and send write protect (CMD30).
- All data write commands can be aborted any time by the stop command (CMD12). The write commands must be stopped prior to deselecting the TriFlash by CMD7. The write commands are: block write (CMD24 and CMD25), write CID (CMD26), and write CSD (CMD27).
- As soon as the data transfer is completed, the TriFlash will exit the data write state and move either to the Programming State (transfer is successful) or Transfer State (transfer failed).
- If a block write operation is stopped and the block length and CRC of the last block are valid, the data will be programmed.

- There is no buffering option for write CSD, write CID, write protection and erase. This means that while the TriFlash is busy servicing any one of these commands, no other data transfer commands will be accepted. DAT line will be kept low as long as the TriFlash is busy and in the Programming State.
- Parameter set commands are *not* allowed while the TriFlash is programming. Parameter set commands are: set block length (CMD16), and erase tagging/untagging (CMD32-37).
- Read commands are *not* allowed while the TriFlash is programming.
- Moving another TriFlash from Stand-by to Transfer State (using CMD7) will not terminate a programming operation. The TriFlash will switch to the Disconnect State and will release the DAT line.
- A TriFlash can be reselected while in the Disconnect State, using CMD7. In this case the TriFlash will move to the Programming State and reactivate the busy indication.
- Resetting a TriFlash (using CMD0 or CMD15) will terminate any pending or active programming operation. This may destroy the data contents on the TriFlash. It is up to the host's responsibility to prevent this.

4.2.1. Data Read Format

The DAT bus line is high when no data is transmitted. A transmitted data block consists of a start bit (LOW), followed by a continuous data stream. The data stream contains the net payload data (and error correction bits if an off-card ECC is used). The data stream ends with an end bit (HIGH). The data transmission is synchronous to the clock signal.

The payload for block oriented data transfer is preserved by a CRC checksum. The generator polynomial is a standard CCITT polynomial:

$$x^{16}+x^{12}+x^{5}+1$$

The code is a shortened BCH code with d=4 and is used for payload length of up to 2048 Bytes.

Block read

The basic unit of data transfer is a block whose maximum size is defined in the CSD (READ_BL_LEN). Smaller blocks whose starting and ending address are wholly contained within one physical block (as defined by READ_BL_LEN) may also be transmitted. A CRC is appended to the end of each block ensuring data transfer integrity. CMD17 (READ_SINGLE_BLOCK) starts a block read and after a complete transfer the device goes back to Transfer State. CMD18 (READ_MULTIPLE_BLOCK) starts a transfer of several consecutive blocks. Blocks will be continuously transferred until a stop command is issued.

If the host uses partial blocks whose accumulated length is not block aligned, the device will, at the beginning of the first misaligned block, detect a block misalignment error, set the ADDRESS_ERROR error bit in the status register, abort transmission and wait (in the *Data State*) for a stop command.

4.2.2. Data Write Format

The data transfer format is similar to the data read format. For block-oriented write data transfer, the CRC check bits are added to each data block. The device performs a CRC check for each such received data block prior to a write operation. (The polynomial is the same one used for a read operation.) By this mechanism, writing of erroneously transferred data can be prevented.

Block write

Block write (CMD24—27) means that one or more blocks of data are transferred from the host to the device with a CRC appended to the end of each block by the host. If the CRC fails, the device will indicate the failure on the DAT line (see below); the transferred data will be discarded and not written, and all further transmitted blocks (in multiple block write mode) will be ignored.

If the host uses partial blocks whose accumulated length is not block aligned, the device will detect the block misalignment error and abort programming before the beginning of the first misaligned block. The device will set the ADDRESS_ERROR error bit in the status register, and while ignoring all further data transfer, wait (in the *Receive-Data-State*) for a stop command.

The write operation will also be aborted if the host tries to write over a write protected area. In this case, however, the device will set the WP_VIOLATION bit.

After receiving a block of data and completing the CRC check, the device will begin programming and hold the DAT line low if its write buffer is full and unable to accept new data from a new WRITE_BLOCK command. The host may poll the status of the device with a SEND_STATUS command at any time, and the device will respond with its status. The status bit READY_FOR_DATA indicates whether the TriFlash can accept new data or whether the write process is still in progress. The host may deselect the device by issuing CMD7 (to select a different device), which will place the device in the Disconnect State and release the DAT line without interrupting the write operation. When reselecting the device, it will reactivate busy indication by pulling DAT to low if programming is still in progress and write buffer is unavailable.

4.2.3. CSD Programming

Programming of the CSD register does not require a previous block length setting. After sending CMD27 and getting the R1 response, send the start bit=0, the modified CSD register = 16Bytes, the CRC16 = 2Bytes, and the end bit = 1. Only the least significant 16 bits [15:0] of the CSD can be changed by the host. The rest of the CSD register content must match the card CSD. If the device detects a content inconsistency between the old and new CSD register, it will not reprogram the CSD. This is done to ensure validity of the CRC field of the CSD register.

Bits [7:1] are the CRC7 of bits [127:8] of the CSD register, which should be recalculated once the CSD register is changed. After calculating CRC7, the CRC16 should also be calculated for all of the CSD register, [127:0].

4.2.4. Erase

It is desirable to erase many sectors simultaneously in order to enhance the data throughput. Identification of these sectors is accomplished with the TAG_* commands. Either an arbitrary set of sectors within a single erase group or an arbitrary selection of erase groups may be erased at one time, but not both together. That is, the unit of measure for determining an erase is either a sector or an erase group, but if a sector, all selected sectors must lie within the same erase group. To facilitate selection, a first command with the starting address is followed by a second command with the final address, and all sectors within this range will be selected for erase. After a range is selected, an individual sector (or group) within that range can be removed using the UNTAG command.

The host must adhere to the following command sequence: TAG_SECTOR_START, TAG_SECTOR_END, UNTAG_SECTOR (up to 16 untag sector commands can be sent for one erase cycle) and ERASE (or the same sequence for group tagging).

The following exception conditions are detected by the TriFlash:

- An erase or tag/untag command is received out of sequence. The device will set the ERASE_SEQ_ERROR error bit in the status register and reset the whole sequence.
- An out of sequence command (except SEND_STATUS) is received. The device will set the ERASE_RESET status bit in the status register, reset the erase sequence and execute the last command.

If the erase range includes write protected sectors, they will be left intact and only the unprotected sectors will be erased. The WP_ERASE_SKIP status bit in the status register will be set.

The address field in the tag commands is a sector or a group address in byte units. The device will ignore all LSBs below the group or sector size.

The number of untag commands (CMD34 and CMD37) which are used in a sequence is limited up to 16.

As described above for block write, the TriFlash will indicate that an erase is in progress by holding DAT low.

4.2.5. Write Protect Management

Device data may be protected against either erase or write by the write protection features. The entire device may be permanently write protected by the manufacturer or content provider by setting the permanent or temporary write protect bits in the CSD. Portions of the data may also be protected (in units of WP_GRP_SIZE sectors as specified in the CSD). The SET_WRITE_PROT command sets the write protection of the addressed write-protect group, and the CLR_WRITE_PROT command clears the write protection of the addressed write-protect group.

The SEND_WRITE_PROT command is similar to a single block read command. The device will send a data block containing 32 write protection bits (representing 32 write protect groups starting at the specified address) followed by 16 CRC bits. The address field in the write protect commands is a group address in byte units. The device will ignore all LSBs below the group size.

4.2.6. Card Lock/Unlock

The Card Lock and Unlock features of the MultiMediaCard have been implemented in the TriFlash. Details on how to use this feature are given in section 4.4.5 of the *MultiMediaCard System Specification*, version 2.2.

4.3. Clock Control

The MultiMediaCard bus clock signal can be used by the TriFlash host to set the devices to energy saving mode or to control the data flow (to avoid under-run or over-run conditions) on the bus. The host is allowed to lower the clock frequency or shut it down.

There are a few restrictions the TriFlash host must follow:

- The bus frequency can be changed at any time (under the restrictions of maximum data transfer frequency, defined by the TriFlash and the identification frequency).
- It is an obvious requirement that the clock must be running for the TriFlash to output data or response tokens. After the last TriFlash bus transaction, the host is required, to provide **eight (8)** clock cycles for the device to complete the operation before shutting down the clock. Following is a list of various MultiMediaCard bus transactions:
  - A command with no response—eight clocks after the host command end bit.
  - A command with response—eight clocks after the device response end bit.
  - A read data transaction—eight clocks after the end bit of the last data block.
  - A write data transaction—eight clocks after the CRC status token.
- The host is allowed to shut down the clock of a "busy" device. The TriFlash will complete the programming operation regardless of the host clock. However, the host must provide a clock edge for the device to turn off its busy signal. Without a clock edge the TriFlash (unless previously disconnected by a deselect command -CMD7) will force the DAT line down, permanently.

4.4. Cyclic Redundancy Codes (CRC)

The CRC is intended for protecting TriFlash commands, responses and data transfer against transmission errors on the MultiMediaCard bus. One CRC is generated for every command and checked for every response on the CMD line. For data blocks, one CRC per transferred block is generated. The CRC is generated and checked as described in the following.

CRC7—The CRC7 check is used for all commands, for all responses except type R3, and for the CSD and CID registers. The CRC7 is a 7-bit value and is computed as follows:

generator polynomial: $G(x) = x^7 + x^3 + 1$.

$M(x) = (\text{first bit}) * x^n + (\text{second bit}) * x^{n-1} + ... + (\text{last bit}) * x^0$

$CRC[6...0] = \text{Remainder } [(M(x) * x^7)/G(x)]$

All CRC registers are initialized to zero. The first bit is the most significant bit of the corresponding bit string (of the command, response, CID or CSD). The degree *n* of the polynomial is the number of CRC protected bits decreased by one. The number of bits to be protected is 40 for commands and responses (n = 39), and 120 for the CSD and CID (n = 119).

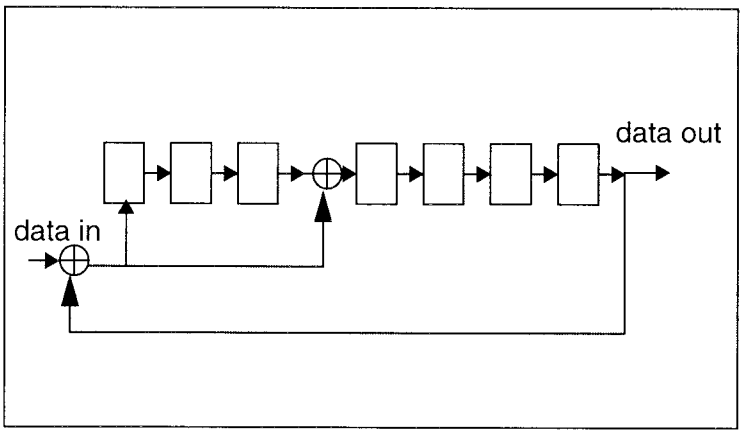

Figure 4-3. CRC7 Generator/Checker

CRC16—The CRC16 is used for payload protection in block transfer mode. The CRC checksum is a 16 bit value and is computed as follows:

generator polynomial G(x) = x16 + x12 +x5 +1
M(x) = (first bit) * xn + (second bit)* xn-1 +...+ (last bit) * x0
CRC[15...0] = Remainder [(M(x) * x16)/G(x)]

All CRC registers are initialized to zero. The first bit is the first data bit of the corresponding block. The degree n of the polynomial denotes the number of bits of the data block decreased by one. For example, n = 4,095 for a block length of 512 bytes. The generator polynomial G(x) is a standard CCITT polynomial. The code has a minimal distance d=4 and is used for a payload length of up to 2,048 bytes ($n \leq 16,383$).

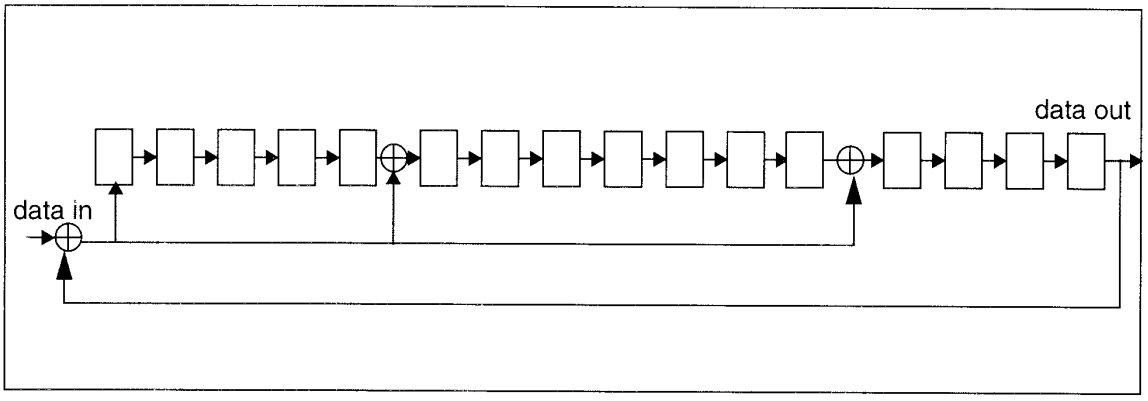

Figure 4-4. CRC16 Generator/Checker

4.5. Error Conditions

The following sections provide valuable information for TriFlash error conditions.

4.5.1. CRC and Illegal Command

All commands are protected by CRC (cyclic redundancy check) bits. If the addressed TriFlash's CRC check fails, the device does not respond and the command is not executed. The TriFlash does not change its state, and COM_CRC_ERROR bit is set in the status register.

Similarly, if an illegal command has been received, a TriFlash shall not change its state, shall not respond and shall set the ILLEGAL_COMMAND error bit in the status register. Only the branches that do not give errors are shown in the state diagrams (Figure 4-1 and Figure 4-2). Table 4-12 contains a complete state transition description.

There are different kinds of illegal commands:

- Commands that belong to classes not supported by the TriFlash (e.g., I/O command CMD39).
- Commands not allowed in the current state (e.g., CMD2 in Transfer State).
- Commands that are not defined (e.g., CMD6).

4.5.2. Read, Write and Erase Time-out Conditions

The times after which a time-out condition for read/write/erase operations occurs are (device independent) **100 times longer** than the typical access/program times for these operations given below. A device shall complete the command within this time period, or give up and return an error message. If the host does not get a response within the defined time-out it should assume the device is not going to respond any more and try to recover (e.g., reset the device, power cycle, reject, etc.). The typical access and program times are defined as follows:

- **Read**—The read access time is defined as the sum of the two times given by the CSD parameters TAAC and NSAC. These device parameters define the typical delay between the end bit of the read command and the start bit of the data block.
- **Write**—The R2W_FACTOR field in the CSD is used to calculate the typical block program time obtained by multiplying the read access time by this factor. It applies to all write/erase commands (e.g., SET(CLEAR)_WRITE_PROTECT, PROGRAM_CSD(CID) and the block write commands).
- **Erase**—The duration of an erase command will be (order of magnitude) the number of sectors to be erased multiplied by the block write delay.

4.6. Commands

The following sections provide valuable information for TriFlash commands.

4.6.1. Command Types

There are four kinds of commands defined on the MultiMediaCard bus:

- **Broadcast commands (bc)**—sent on CMD, no response.
- **Broadcast commands with response (bcr)**—sent on CMD, response (all devices simultaneously) on CMD.
- **Addressed (point-to-point) commands (ac)**—sent on CMD, response on CMD.
- **Addressed (point-to-point) data transfer commands (adtc)**—sent on CMD, response on CMD, data transfer on DAT.

The command transmission always starts with the MSB.

4.6.2. Command Format

All commands have a length of 48 bits, and require 2.4 µs @ 20 MHz. The structure of each command is given in Table 4-2. Commands and arguments are listed in Table 4-3 to Table 4-11.

Table 4-2. MultiMediaCard Bus Command Format

0	1	bit 5...bit 0	bit 31...bit 0	bit 6...bit 0	1
start bit	host	command	argument	CRC7[1]	end bit

7-bit CRC Calculation: $G(x) = x^7 + x^3 + 1$
$M(x) = (\text{start bit}) * x^{39} + (\text{host bit}) * x^{38} + ... + (\text{last bit before CRC}) * x^0$
$CRC[6...0] = \text{Remainder}[(M(x) * x^7)/G(x)]$

4.6.3. Command Classes

The command set of the TriFlash is divided into several classes (See Table 4-3). Each class supports a set of MultiMediaCard bus functions. The supported Card Command Classes (CCC) are coded as a parameter in the card specific data (CSD) register of each device, providing the host with information on how to access the device.

Table 4-3. Card Command Classes (CCCs)

Card Command Class (CCC)	Class Description	Supported Commands															
		0	1	2	3	4	7	9	10	11	12	13	15	16	17	18	20
Class 0	Basic	+	+	+	+	+	+	+	+		+	+	+				
Class 2	Block Read													+	+	+	
Class 4	Block Write													+			
Class 5	Erase																
Class 6	Write-Protection																
Class 7	Lock Card																
Class 8	Application Specific[2]																
Class 9	I/O Mode[2]																
Class 10-11	Reserved																

[1] 7-bit Cyclic Redundancy Check.

[2] Application specific and I/O mode classes are not supported by the SanDisk TriFlash.

Table 4-4. Card Command Classes (CCCs)

Card Command Class (CCC)	Class Description	Supported Commands																		
		24	25	26	27	28	29	30	32	33	34	35	36	37	38	39	40	42	55	56
Class 0	Basic																			
Class 2	Block Read																			
Class 4	Block Write	+	+	+	+															
Class 5	Erase								+	+	+	+	+	+	+					
Class 6	Write-Protection					+	+	+												
Class 7	Lock Card																	+		
Class 8	Application Specific																		+	+
Class 9	I/O Mode															+	+			
Class 10-11	Reserved																			

4.6.4. Detailed Command Description

All future reserved commands have to be 48 bits long, their responses have to be also 48 bits long or they might also have no response. Tables 4-5 through 4-13 define in detail the MultiMediaCard bus commands.

Table 4-5. Basic Commands (Class 0)

Cmd Index	Type	Argument	Resp	Abbreviation	Command Description
CMD0	bc	[31:0] do not care[1]	-	GO_IDLE_STATE	Resets all devices to Idle State.
CMD1	bcr	[31:0] OCR without busy	R3	SEND_OP_COND	Asks all devices in idle state to send their operation conditions register content in the response on the CMD line.
CMD2	bcr	[31:0] do not care	R2	ALL_SEND_CID	Asks all devices to send their CID numbers on the CMD line.
CMD3	ac	[31:16] RCA [15:0] do not care	R1	SET_RELATIVE_ ADDR	Assigns relative address to the device.
CMD4[2]	Not Supported				
CMD5	Reserved				
CMD6	Reserved				
CMD7	ac	[31:16] RCA [15:0] do not care	R1 (only from the selected device)	SELECT/DESELECT_ CARD	Command toggles a device between the Stand-by and Transfer states or between the Programming and Disconnect state. In both cases the device is selected by its own relative address and deselected by any other address; address 0 deselects all.
CMD8	Reserved				
CMD9	ac	[31:16] RCA [15:0] do not care	R2	SEND_CSD	Addressed device sends its card-specific data (CSD) on the CMD line.

[1] Do not care = the bit places must be filled but the value is irrelevant.

[2] The DSR option (as well as the SET_DSR command) is not supported by the SanDisk TriFlash.

Cmd Index	Type	Argument	Resp	Abbreviation	Command Description
CMD10	ac	[31:16] RCA [15:0] do not care	R2	SEND_CID	Addressed device sends its card identification (CID) on the CMD line.
CMD11	Not supported				
CMD12	ac	[31:0] do not care	R1b[1]	STOP_ TRANSMISSION	Terminates a multiple block read/write operation.
CMD13	ac	[31:16] RCA [15:0] do not care	R1	SEND_STATUS	Addressed device sends its status register.
CMD14	Reserved				
CMD15	ac	[31:16] RCA [15:0] do not care	-	GO_INACTIVE_ STATE	Sets the device to inactive state.

Table 4-6. Block Read Commands (Class 2)

Cmd Index	Type	Argument	Resp	Abbreviation	Command Description
CMD16	ac	[31:0] block length	R1	SET_BLOCKLEN	Selects a block length (in bytes) for all following block commands (read and write).[2]
CMD17	adtc	[31:0] data address	R1	READ_SINGLE_ BLOCK	Reads a block of the size selected by the SET_BLOCKLEN command.[3]
CMD18	adtc	[31:0] data address	R1	READ_MULTIPLE_BLOCK	Continuously send blocks of data until interrupted by a stop or a new read command.
CMD19	Reserved				

Table 4-7. Block Write Commands (Class 4)

Cmd Index	Type	Argument	Resp	Abbreviation	Command Description
CMD24	Adtc	[31:0] data address	R1	WRITE_BLOCK	Writes a block of the size selected by the SET_BLOCKLEN command.[4]
CMD25	Adtc	[31:0] data address	R1	WRITE_MULTIPLE_ BLOCK	Continuously writes blocks of data until a STOP_TRANSMISSION follows.
CMD26	Not Applicable				
CMD27	Adtc	[31:0] do not care[5]	R1	PROGRAM_CSD	Programming of the programmable bits of the CSD.

[1] The device may become busy after this command. Refer to Figure 5-18 for more details.

[2] The default block length is as specified in the CSD (512 bytes). A set block length of less than 512 bytes will cause a write error. The only valid write set block length is 512 bytes. CMD16 is not mandatory if the default is accepted.

[3] The data transferred must not cross a physical block boundary.

[4] All data blocks are responded to with a data response token followed by a busy signal. The data transferred must not cross a physical block boundary.

[5] The bit places must be filled but the value is irrelevant.

Table 4-8. Write Protection (Class 6)

Cmd Index	Type	Argument	Resp	Abbreviation	Command Description
CMD28	ac	[31:0] data address	R1b	SET_WRITE_PROT	Sets the write protection bit of the addressed group. The properties of write protection are coded in the card specific data (WP_GRP_SIZE)
CMD27	ac	[31:0] data address	R1b	CLR_WRITE_PROT	Clears the write protection bit of the addressed group.
CMD27	adtc	[31:0] write protect data address	R1	SEND_WRITE_PROT	Asks the device to send the status of the write protection bits.[1]
CMD31	Reserved				

Table 4-9. Erase Commands (Class 5)

Cmd Index	Type	Argument	Resp	Abbreviation	Command Description
CMD32	ac	[31:0] data address	R1	TAG_SECTOR_START	Sets the address of the first sector of the erase group.
CMD33	ac	[31:0] data address	R1	TAG_SECTOR_END	Sets the address of the last sector in a continuous range within the selected erase group, or the address of a single sector to be selected for erase.
CMD34	ac	[31:0] data address	R1	UNTAG_SECTOR	Removes one previously selected sector from the erase selection.
CMD35	ac	[31:0] data address	R1	TAG_ERASE_GROUP_ START	Sets the address of the first erase group within a range to be selected for erase.
CMD36	ac	[31:0] data address	R1	TAG_ERASE_GROUP_ END	Sets the address of the last erase group within a continuous range to be selected for erase.
CMD37	ac	[31:0] data address	R1	UNTAG_ERASE_ GROUP	Removes one previously selected erase group from the erase selection.
CMD38	ac	[31:0] do not care[2]*	R1b	ERASE	Erases all previously selected sectors or erase groups.

Table 4-10. I/O Mode Commands (Class 9)

Cmd Index	Type	Argument	Resp	Abbreviation	Command Description
CMD39 CMD40	MMCA Optional Command, currently not supported.				
CMD41	Reserved				

[1] 32 write protection bits (representing 32 write protect groups starting at the specified address) followed by 16 CRC bits are transferred in a payload format via the data line. The last (least significant) bit of the protection bits corresponds to the first addressed group. If the addresses of the last group are outside the valid range, then the corresponding write protection bits shall be set to zero.

[2] The bit places must be filled but the value is irrelevant.

Table 4-11. Lock Card Commands (Class 7)

Cmd Index	Type	Argument	Resp	Abbreviation	Command Description
CMD42	adtc	[31:0] stuff bits	R1b	LOCK_UNLOCK	Used to set/reset the password or lock/unlock the card. The size of the data block is set by the SET_BLOCK_LEN command.
CMD43 to CMD54	Reserved				

Table 4-12. Application Specific Commands (Class 8)

Cmd Index	Type	Argument	Resp	Abbreviation	Command Description
CMD55 CMD56	MMCA Optional Command, currently not supported.				

4.7. Device State Transition Table

Table 4-13 defines the TriFlash state transitions in dependency of the received command.

Table 4-13. Device State Transition Table

	Current State										
	idle	ready	ident	stby	tran	data	rcv	prg	dis	ina	irq
Command	Changes to										
class independent											
CRC error	-	-	-	-	-	-	-	-	-	-	stby
command not supported	-	-	-	-	-	-	-	-	-	-	stby
Class 0											
CMD0	idle	idle	idle	idle	idle	idle	idle	idle	idle	-	stby
CMD1, device VDD range compatible	ready	-	-	-	-	-	-	-	-	-	stby
CMD1, device is busy	idle	-	-	-	-	-	-	-	-	-	stby
CMD1, device VDD range not compatible	ina	-	-	-	-	-	-	-	-	-	stby
CMD2, device wins bus	-	ident	-	-	-	-	-	-	-	-	stby
CMD2, device loses bus	-	ready	-	-	-	-	-	-	-	-	stby
CMD3	-	-	stby	-	-	-	-	-	-	-	stby
CMD4	Not supported										
CMD7, device is addressed	-	-	-	tran	-	-	-	-	prg	-	stby
CMD7, device is not addressed	-	-	-	-	stby	stby	-	dis	-	-	stby

	Current State										
	idle	**ready**	**ident**	**stby**	**tran**	**data**	**rcv**	**prg**	**dis**	**ina**	**irq**
Command	**Changes to**										
CMD9	-	-	-	stby	-	-	-	-	-	-	stby
CMD10	-	-	-	stby	-	-	-	-	-	-	stby
CMD12	-	-	-	-	-	tran	prg	-	-	-	stby
CMD13	-	-	-	stby	tran	data	rcv	prg	dis	-	stby
CMD15	-	-	-	ina	ina	ina	ina	ina	ina	-	stby
Class 1											
CMD11	Not supported										
Class 2											
CMD16	-	-	-	-	tran	-	-	-	-	-	stby
CMD17	-	-	-	-	data	-	-	-	-	-	stby
CMD18	-	-	-	-	data	-	-	-	-	-	stby
Class 3											
CMD20	Not supported										
Class 4											
CMD16	See class 2										
CMD24	-	-	-	-	rcv	-	-	rcv	-	-	stby
CMD25	-	-	-	-	rcv	-	-	rcv	-	-	stby
CMD26	-	-	-	-	rcv	-	-	-	-	-	stby
CMD27	-	-	-	-	rcv	-	-	-	-	-	stby
Class 6											
CMD28	-	-	-	-	prg	-	-	-	-	-	stby
CMD29	-	-	-	-	prg	-	-	-	-	-	stby
CMD30	-	-	-	-	data	-	-	-	-	-	stby
Class 5											
CMD32	-	-	-	-	tran	-	-	-	-	-	stby
CMD33	-	-	-	-	tran	-	-	-	-	-	stby
CMD34	-	-	-	-	tran	-	-	-	-	-	stby
CMD35	-	-	-	-	tran	-	-	-	-	-	stby
CMD36	-	-	-	-	tran	-	-	-	-	-	stby
CMD37	-	-	-	-	tran	-	-	-	-	-	stby
CMD38	-	-	-	-	prg	-	-	-	-	-	stby
Class 7											
CMD42	-	-	-	-	rcv	-	-	-	-	-	stby
Class 8											

	Current State										
	idle	**ready**	**ident**	**stby**	**tran**	**data**	**rcv**	**prg**	**dis**	**ina**	**irq**
Command	**Changes to**										
CMD-55	MMCA Optional Command, currently not supported										
CMC-56; RD/WR = 0	MMCA Optional Command, currently not supported										
CMD-56; RD/WR = 1	MMCA Optional Command, currently not supported										
Class 9											
CMD39, CMD40	MMCA Optional Command, currently not supported										
Class 10—11											
CMD41...CMD59	Reserved										
CMD60...CMD63	Reserved for manufacturer										

4.8. Responses

All responses are sent via the CMD line. The response transmission always starts with the MSB. The response length depends on the response type.

A response always starts with a start bit (always '0'), followed by the bit indicating the direction of transmission (device = '0'). A value denoted by 'x' in the tables below indicates a variable entry. All responses except for the type R3 (see below) are protected by a CRC. Every response is terminated by the end bit (always '1').

There are five types of responses. Their formats are defined as follows:

R1 (standard response)—response length 48 bits.
Bits 45:40 indicate the index of the command that is responded to. The status of the device is coded in 32 bits.

Bit Position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'0'	x	x	x	'1'
Description	start bit	transmission bit	command index	device status	CRC7	end bit

R1b is identical to R1 with the additional busy signaling via the data.

R2 (CID, CSD register)—response length 136 bits.
The content of the CID register is sent as a response to CMD2 and CMD10. The content of the CSD register is sent as a response to CMD9. Only bits [127...1] of the CID and CSD are transferred, bit [0] of these registers is replaced by the end bit of the response.

Bit Position	135	134	[133:128]	[127:1]	0
Width (bits)	1	1	6	127	1
Value	'0'	'0'	'111111'	x	'1'
Description	start bit	transmission bit	Reserved	CID or CSD register incl. internal CRC7	end bit

R3 (OCR register)—response length 48 bits.

The contents of the OCR register are sent as a response to CMD1.

Bit Position	47	46	[45:40]	[39:8]	[7:1]	0
Width (bits)	1	1	6	32	7	1
Value	'0'	'0'	'111111'	x	'1111111'	'1'
Description	start bit	transmission bit	Reserved	OCR register	Reserved	end bit

NOTE: Responses R4 and R5 are not supported.

4.8.1. Data Response

When a data block or the CSD register is written to the device, it will be acknowledged by a CRC Status response. CRC Status response is 5 bits long and has the following format:

[Start bit = 0 | CRC Status 3 bits | End bit = 1]

The CRC Status bits may be:

'010' or '00101 including the Start and End bits'—Data accepted.
'101' or '01011 including the Start and End bits'—Data rejected due to a CRC error.

4.9. Timings

All timing diagrams use the schematics and abbreviations listed in Table 4-14.

Table 4-14. Timing Diagram Symbols

S	Start Bit (= 0)
T	Transmitter Bit (Host = 1, Device = 0)
P	One-cycle Pull-up (= 1)
E	End Bit (=1)
Z	High Impedance State (-> = 1)
D	Data Bits
*	Repeater
CRC	Cyclic Redundancy Check Bits (7 Bits)
	Device Active
	Host Active

4.9.1. Command and Response

Card Identification and Card Operation Conditions Timing—The card identification (CMD2) and card operation conditions (CMD1) timing are processed in the open-drain mode. The device response to the host command starts after exactly N_{ID} clock cycles.

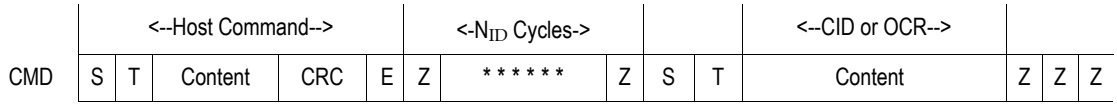

Figure 4-5. Identification Timing (Card Identification Mode)

The minimum delay between the host command and device response is N_{CR} clock cycles. This timing diagram is relevant for host command CMD3.

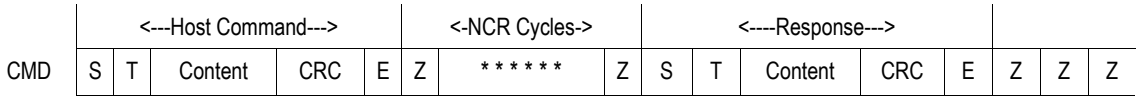

Figure 4-6. Command Response Timing (Identification Mode)

There is just one Z bit period followed by P bits pushed up by the responding device. This timing diagram is relevant for all responded host commands except CMD1, 2, 3.

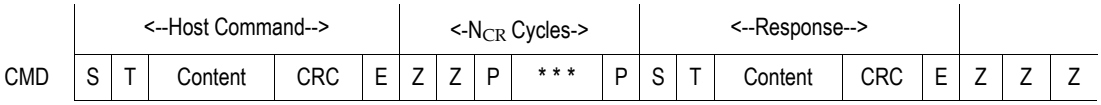

Figure 4-7. Command Response Timing (Data Transfer Mode)

Last Card Response—Next Host Command Timing—After receiving the last card response, the host can start the next command transmission after at least N_{RC} clock cycles. This timing is relevant for any host command.

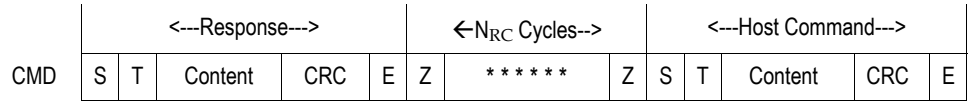

Figure 4-8. Timing Response End to Next CMD Start (Data Transfer Mode)

Last Host Command—Next Host Command Timing Diagram—After the last command has been sent, the host can continue sending the next command after at least N_{CC} clock periods. This timing is relevant for any host command that does not have a response.

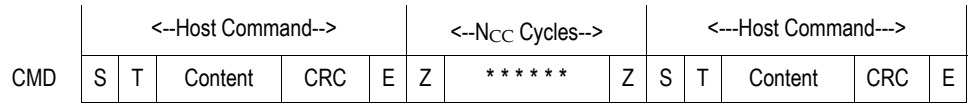

Figure 4-9. Timing CMD_n End to CMD_{n+1} Start (All Modes)

In the case where the $\mathbf{CMD}_n$ command was a last acquisition command with no further response by any device, then the next $\mathbf{CMD}_{n+1}$ command is allowed to follow after at least N_{CC} +136 (the length of the R2 response) clock periods.

4.9.2. Data Read

Single Block Read—The host selects one device for data read operation by CMD7, and sets the valid block length for block oriented data transfer by CMD16. The basic bus timing for a read operation is given in Figure 4-10. The sequence starts with a single block read command (CMD17), which specifies the start address in the argument field. The response is sent on the CMD line as usual.

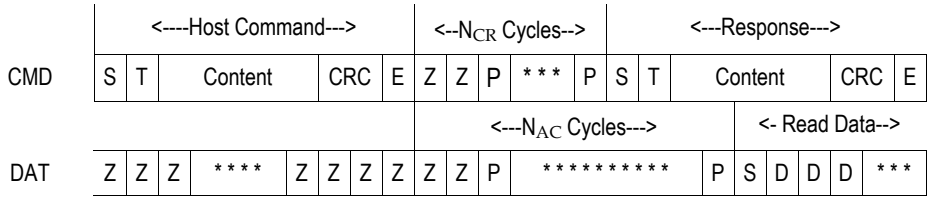

Figure 4-10. Transfer of Single Block Read

Data transmission from the device starts after the access time delay NAC beginning from the end bit of the read command. After the last data bit, the CRC check bits are suffixed to allow the host to check for transmission errors.

Multiple Block Read—In multiple block read mode, the device sends a continuous flow of data blocks following the initial host read command. The data flow is terminated by a stop transmission command (CMD12). Figure 4-11 describes the timing of the data blocks and Figure 4-12 the response to a stop command. The data transmission stops two clock cycles after the end bit of the stop command.

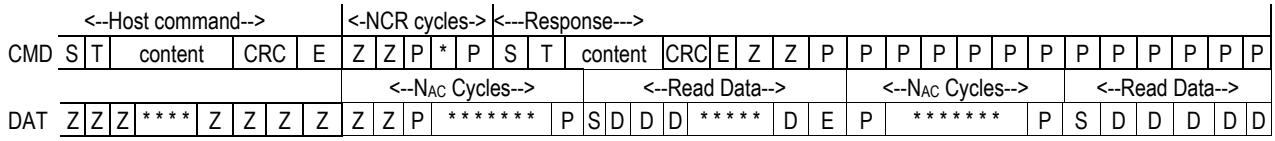

Figure 4-11. Timing of Multiple Block Read Command

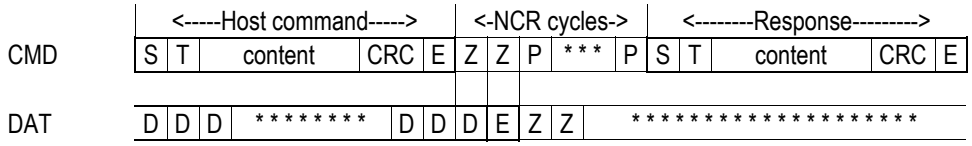

Figure 4-12. Timing of Stop Command (CMD12, Data Transfer Mode)

4.9.3. Data Write

Single Block Write—The host selects one device for a data write operation by CMD7.

The host sets the valid block length for block-oriented data transfer by CMD16.

The basic bus timing for a write operation is given in Figure 4-13. The sequence starts with a single block write command (CMD24), which determines (in the argument field) the start address. It is responded to by the device on the CMD line as usual. The data transfer from the host starts N_{WR} clock cycles after the device response was received.

The data is suffixed with CRC check bits to allow the device to check it for transmission errors. The device sends back the CRC check result as a CRC status token on the data line. In the case of transmission error, the device sends a negative CRC status (‘101’). In the case of a successful transmission, the device sends a positive CRC status (‘010’) and starts the data programming procedure.

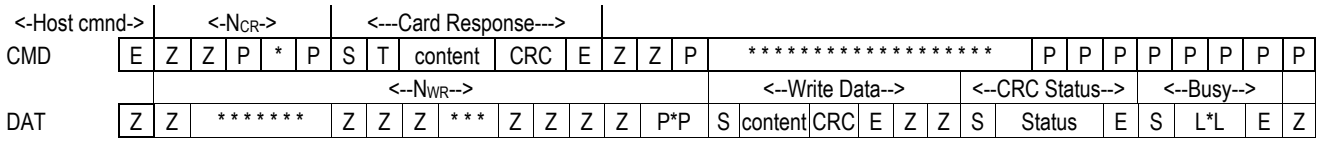

Figure 4-13. Timing of Block Write Command

If the TriFlash does not have a free data receive buffer, the device indicates this condition by pulling down the data line to LOW. The device stops pulling down the data line as soon as at least one receive buffer for the defined data transfer block length becomes free. This signaling does not give any information about the data write status, which must be polled by the host.

Multiple Block Write—In multiple block write mode, the device expects continuous flow of data blocks following the initial host write command. The data flow is terminated by a stop transmission command (CMD12). Figure 4-14 describes the timing of the data blocks with and without device busy signal.

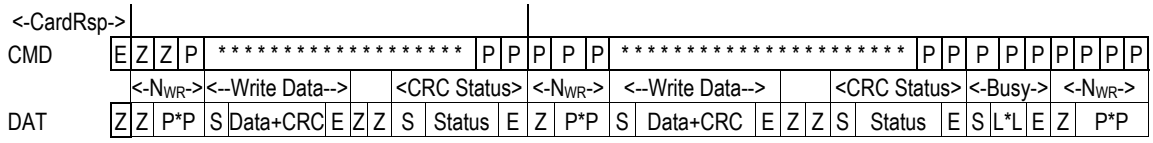

Figure 4-14. Timing of Multiple Block Write Command

In write mode, the stop transmission command works similarly to the stop transmission command in the read mode. Figures 4-15 to 4-18 describe the timing of the stop command in different device states.

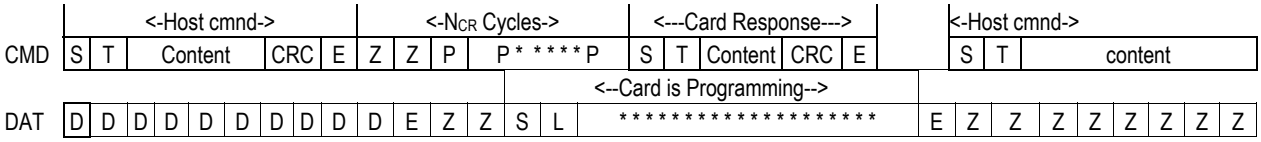

Figure 4-15. Stop Transmission During Data Transfer from the Host

The device will treat a data block as successfully received and ready for programming only if the CRC data of the block was validated and the CRC status token sent back to the host. Figure 4-16 is an example of an interrupted (by a host stop command) attempt to transmit the CRC status block. The sequence is identical to all other stop transmission examples. The end bit of the host command is followed, on the data line, with one more data bit, end bit and two Z clock for switching the bus direction. The received data block, in this case is considered incomplete and will not be programmed.

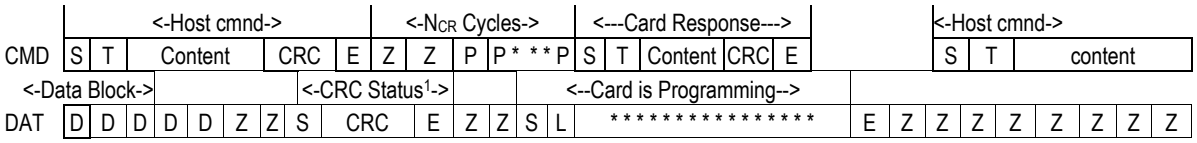

Figure 4-16. Stop Transmission During CRC Status Transfer from the Device

All previous examples dealt with the scenario of the host stopping the data transmission during an active data transfer. The following two diagrams describe a scenario of receiving the stop transmission between data blocks. In the first example the device is busy programming the last block while in the second the device is idle. However, there are still unprogrammed data blocks in the input buffers. These blocks are being programmed as soon as the stop transmission command is received and the device activates the busy signal.

[1] The card CRC status response was interrupted by the host.

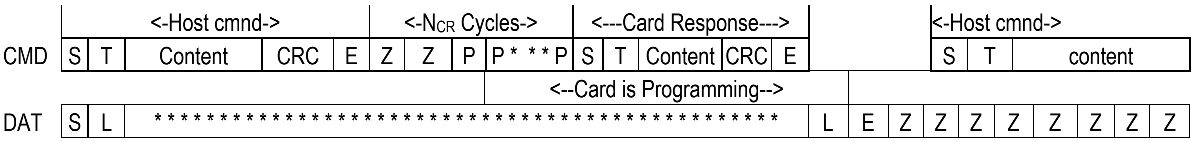

Figure 4-17. Stop Transmission Received After Last Data Block, Device is Busy Programming

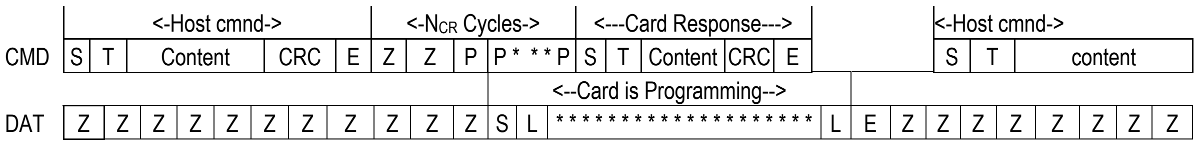

Figure 4-18. Stop Transmission Received After Last Data Block, Device Becomes Busy

Erase, Set and Clear Write Protect Timing—The host must first tag the sectors to erase using the tag commands (CMD32—CMD37). The erase command (CMD38), once issued, will erase all tagged sectors. Similarly, set and clear write protect commands start a programming operation as well. The device will signal "busy" (by pulling the DAT line low) for the duration of the erase or programming operation. The bus transaction timings are described in Figure 4-18.

4.9.4. Timing Values

Table 4-15 defines all timing values.

Table 4-15. Timing Values

	Min	Max	Unit
N_{CR}	2	64	Clock Cycles
N_{ID}	5	5	Clock Cycles
N_{AC}	2	[100 * ((TAAC*f) + (100*NSAC))][1]	Clock Cycles
N_{RC}	8	-	Clock Cycles
N_{CC}	8	-	Clock Cycles
N_{WR}	2	-	Clock Cycles

[1] Where f is the clock frequency.

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5. SPI Protocol Definition

5.1. SPI Bus Protocol

While the MultiMediaCard channel is based on command and data bit-streams, which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of eight bit bytes and is byte aligned (multiples of eight clocks) to the CS signal.

Similar to the MultiMediaCard Bus protocol, the SPI messages are built from command, response and data-block tokens. All communication between host and devices is controlled by the host (master). The host starts every bus transaction by asserting the CS signal low.

The response behavior in SPI Bus mode differs from the MultiMediaCard Bus mode in the following three ways:

- The selected device always responds to the command.
- An 8- or 16-bit response structure is used.
- When the device encounters a data retrieval problem, it will respond with an error response (which replaces the expected data block) rather than time-out as in the MultiMediaCard Bus mode.

In addition to the command response, every data block sent to the device during write operations will be responded with a special data response token. A data block may be as big as one device write block (WRITE_BL_LEN) and as small as a single byte[1].

5.1.1. Mode Selection

The TriFlash wakes up in the MultiMediaCard Bus mode. It will enter SPI mode if the CS signal is asserted (negative) during the reception of the reset command (CMD0). If the device recognizes that the MultiMediaCard Bus mode is required it will not respond to the command and remain in the MultiMediaCard Bus mode. If SPI mode is required, the device will switch to SPI mode and respond with the SPI mode R1 response.

The only way to return to the MultiMediaCard Bus mode is by power cycling the device. In SPI mode, the MultiMediaCard Bus protocol state machine is not observed. All the MultiMediaCard bus commands supported in SPI mode are always available.

The default command structure/protocol for SPI mode is that CRC checking is disabled. Since the device powers up in MultiMediaCard Bus mode, CMD0 must be followed by a valid CRC byte (even though the command is sent using the SPI structure). Once in SPI mode, CRCs are disabled by default.

CMD0 is a static command and always generates the same 7-bit CRC of 4Ah. Adding the "1," end bit (bit 0) to the CRC creates a CRC byte of 95h. The following hexadecimal sequence can be used to send CMD0 in all situations for SPI mode, since the CRC byte (although required) is ignored once in SPI mode. The entire CMD0 sequence appears as 40 00 00 00 00 95 (hexadecimal).

[1] The default block length is as specified in the CSD (512 bytes). A set block length of less than 512 bytes will cause a write error. The only valid write set block length is 512 bytes. CMD16 is not mandatory if the default is accepted.

5.1.2. Bus Transfer Protection

Every TriFlash token transferred on the bus is protected by CRC bits. In SPI mode, the TriFlash offers an unprotected mode, which enables systems built with reliable data links to exclude the hardware or firmware required for implementing the CRC generation and verification functions.

In the unprotected mode the CRC bits of the command, response and data tokens are still required in the tokens however, they are defined as “do not care” for the transmitters and ignored by the receivers.

The SPI interface is initialized in the unprotected mode. The host can turn this option on and off using CRC_ON_OFF command (CMD59).

The CRC7/CRC16 polynomials are identical to that used in MultiMediaCard Bus mode. Refer to Section 5.5 in the MultiMediaCard Bus mode chapter.

5.1.3. Data Read

SPI mode supports single block and multiple block read operations (CMD17 or CMD18). Upon reception of a valid read command the device will respond with a response token followed by a data token in the length defined in a previous SET_BLOCK_LENGTH (CMD16) command (refer to Figure 5-1).

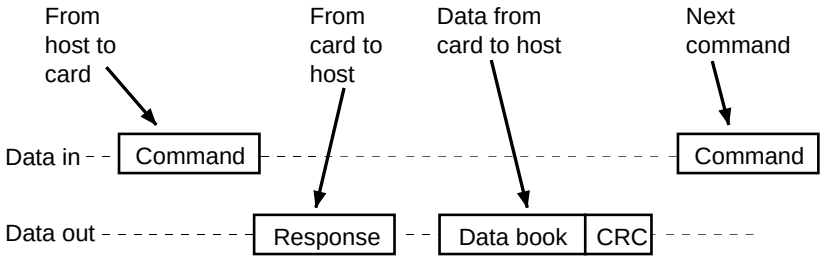


Figure 5-1. Single Block Read Operation

A valid data block is suffixed with a 16 bit CRC generated by the standard CCITT polynomial:

$$x^{16}+x^{12}+x^{5}+1$$

The maximum block length is 512 bytes as defined by READ_BL_LEN (CSD parameter). Block lengths can be any number between 1 and READ_BL_LEN.

The start address can be any byte address in the valid address range of the device. Every block, however, must be contained in a single physical device sector.

In case of data retrieval error, the device will not transmit any data. Instead, a special data error token will be sent to the host. Figure 5-2 shows a data read operation that terminated with an error token rather than a data block.

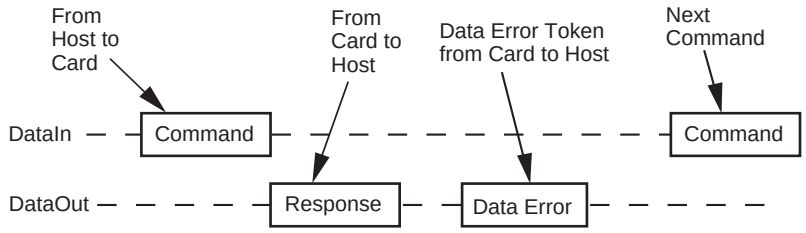


Figure 5-2. Read Operation—Data Error

In the case of a Multiple Block Read operation, every transferred block has a 16-bit CRC suffix. The Stop Transmission command (CMD12) will actually stop the data transfer operation (the same as in MultiMediaCard Bus mode).

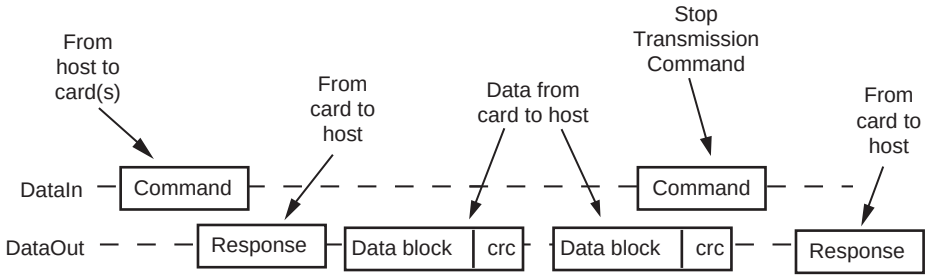


Figure 5-3. Multiple Block Read Operation

5.1.4. Data Write

In SPI mode, the TriFlash supports single block or multiple block write operations. Upon reception of a valid write command (CMD24 or CMD25), the device will respond with a response token and will wait for a data block to be sent from the host. CRC suffix and start address restrictions are identical to the read operation (see Figure 5-4). The only valid block length, however, is 512 bytes. Setting a smaller block length will cause a write error on the next write command.

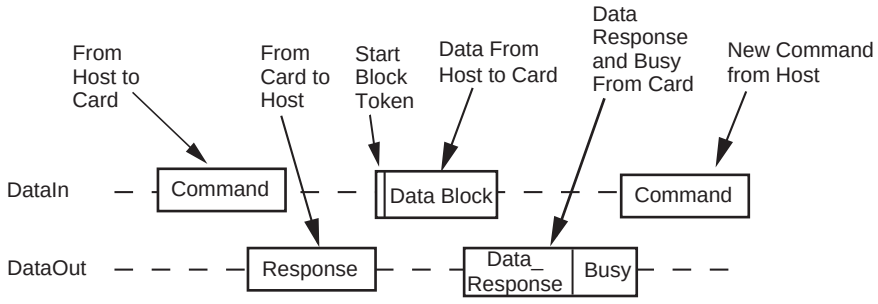


Figure 5-4. Single Block Write Operation

Every data block has a prefix or ‘start block’ token (one byte). After a data block is received the device will respond with a data-response token, and if the data block is received with no errors, it will be programmed. As long as the device is busy programming, a continuous stream of busy tokens will be sent to the host (effectively holding the DataOut line low).

Once the programming operation is completed, the host must check the results of the programming using the SEND_STATUS command (CMD13). Some errors (e.g., address out of range, write protect violation) are detected during programming only. The only validation check performed on the data block and communicated to the host via the data-response token is CRC and general Write Error indication.

In Multiple Block write operation the stop transmission will be done by sending 'Stop Tran' token instead of 'Start Block' token at the beginning of the next block. In case of Write Error indication (on the data response) the host shall use SEND_NUM_WR_BLOCKS (ACMD22) in order to get the number of well written write blocks. The data token's description is given in Section 5.2.4.

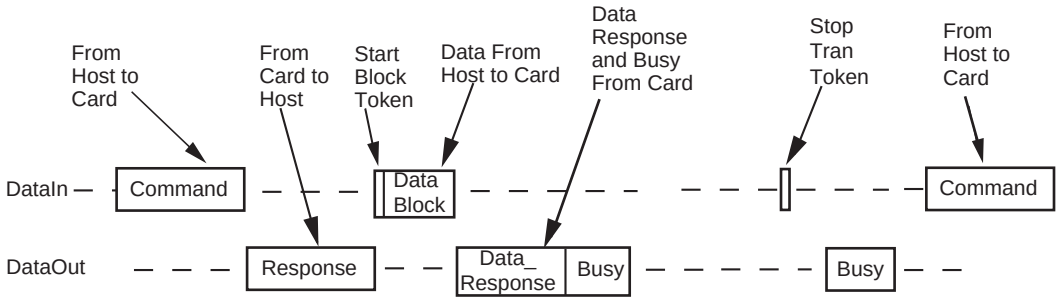


Figure 5-5. Multiple Block Write Operation

Resetting the CS signal while the device is busy, will not terminate the programming process. The device will release the DataOut line (tristate) and continue to program. If the device is reselected before the programming is done, the DataOut line will be forced back to low and all commands will be rejected.

Resetting a device (using CMD0) will terminate any pending or active programming operation. This may destroy the data formats on the device. It is the host's responsibility to prevent it.

5.1.5. Erase and Write Protect Management

The erase and write protect management procedures in the SPI mode are identical to the MultiMediaCard Bus mode. While the device is erasing or changing the write protection bits of the predefined sector list it will be in a busy state and will hold the DataOut line low. Figure 5-6 illustrates a "no data" bus transaction with and without busy signaling.

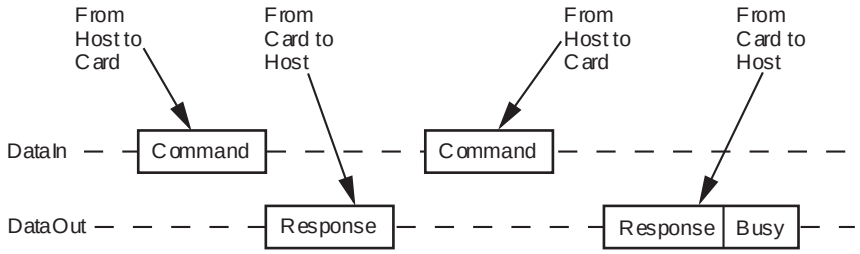


Figure 5-6. "No Data" Operations

5.1.6. Read CID/CSD Registers

Unlike the MultiMediaCard Bus protocol (where the register contents are sent as a command response), reading the contents of the CSD and CID registers in SPI mode is a simple read-block transaction. The device will respond with a standard response token followed by a data block of 16 bytes suffixed with a 16-bit CRC.

The data time out for the CSD command cannot be set to the device TAAC since this value is stored in the CSD. Therefore, the standard response time-out value(N_{CR}) is used for read latency of the CSD register.

5.1.7. Reset Sequence

The TriFlash requires a defined reset sequence. After power on reset or CMD0 (software reset), the device enters an idle state. At this state, the only legal host commands are CMD1 (SEND_OP_COND), CMD1 (SD_SEND_OP_COND), CMD59 (CRC_ON_OFF) and CMD58 (READ_OCR).

The host must poll the device (by repeatedly sending CMD1) until the 'in-idle-state' bit in the device response indicates (by being set to 0) that the device completed its initialization processes and is ready for the next command.

In SPI mode, however, CMD1 has no operands and does not return the contents of the OCR register. Instead, the host can use CMD58 (SPI Mode Only) to read the OCR register. It is the responsibility of the host to refrain from accessing devices that do not support its voltage range.

The use of CMD58 is not restricted to the initialization phase only, but can be issued at any time. The host must poll the device (by repeatedly sending CMD1) until the 'in-idle-state' bit in the device response indicates (by being set to 0) that the device has completed its initialization process and is ready for the next command.

5.1.8. Clock Control

The SPI bus clock signal can be used by the SPI host to set the devices to energy-saving mode or to control the data flow (to avoid under-run or over-run conditions) on the bus. The host is allowed to change the clock frequency or shut it down. There are a few restrictions the SPI host must follow:

- The bus frequency can be changed at any time (under the restrictions of maximum data transfer frequency, defined by the TriFlash devices).
- It is an obvious requirement that the clock must be running for the TriFlash to output data or response tokens. After the last SPI bus transaction, the host is required to provide 8 (eight) clock cycles for the device to complete the operation before shutting down the clock. Throughout this 8 clock period, the state of the CS signal is irrelevant. It can be asserted or de-asserted. Following is a list of the various SPI bus transactions:
  - A command/response sequence. Eight clocks after the device response end bit. The CS signal can be asserted or de-asserted during these 8 clocks.
  - A read data transaction. Eight clocks after the end bit of the last data block.
  - A write data transaction. Eight clocks after the CRC status token.
- The host is allowed to shut down the clock of a "busy" device. The TriFlash will complete the programming operation regardless of the host clock. However, the host must provide a clock edge for the device to turn off its busy signal. Without a clock edge, the TriFlash (unless previously disconnected by de-asserting the CS signal) will force the DataOut line down, permanently.

5.1.9. Error Conditions

The following sections provide valuable information for TriFlash error conditions.

5.1.9.1. CRC and Illegal Commands

Unlike the MultiMediaCard Bus protocol, in SPI mode the device will always respond to a command. The response indicates acceptance or rejection of the command. A command may be rejected in any one of the following cases:

- It is sent while the device is in read operation (except CMD12 which is legal).
- It is sent while the device is in Busy.
- Device is locked and it is other than Class 0 or 7 commands.
- It is not supported (illegal opcode).
- CRC check failed.
- It contains an illegal operand.
- It was out of sequence during an erase sequence.

NOTE: In case the host sends command while the device sends data in read operation then the response with an illegal command indication may disturb the data transfer.

5.1.9.2. Read, Write and Erase Time-out Conditions

The times after which a time-out condition for read operations occur are (device independent**) either 100 times longer** than the typical access times for these operations given below **or 100ms**. The times after which a time-out condition for Write/Erase operations occur are (device independent**) either 100 times longer** than the typical program times for these operations given below **or 250ms**. A device shall complete the command within this time period, or give up and return an error message. If the host does not get any response with the given time out it should assume the device is not going to respond anymore and try to recover (e.g., reset the device, power cycle, reject). The typical access and program times are defined as follows:

- **Read**—The read access time is defined as the sum of the two times given by the CSD parameters TAAC and NSAC. These device parameters define the typical delay between the end bit of the read command and the start bit of the data block.
- **Write**—The R2W_FACTOR field in the CSD is used to calculate the typical block program time obtained by multiplying the read access time by this factor. It applies to all write/erase commands (e.g., SET (CLEAR)_WRITE_PROTECT, PROGRAM_CSD (CID) and the block write commands).
- **Erase**—The duration of an erase command will be (order of magnitude) the number of write blocks (WRITE_BL) to be erased multiplied by the block write delay.

5.1.10. Memory Array Partitioning

Same as for MultiMediaCard Bus mode.

5.1.11. Card Lock/Unlock

Same as for MultiMediaCard Bus mode.

5.2. SPI Command Set

The following sections provide valuable information for the SPI Command Set.

5.2.1. Command Format

All the TriFlash commands are 6 bytes long and transmitted MSB first.

Byte 1				Bytes 2—5		Byte 6	
7	6	5	0	31	0	7	0
0	1	Command		Command Argument		CRC	1

Figure 5-7. SPI Command Format

Commands and arguments are listed in Table 5-2.

7-bit CRC Calculation: $G(x) = x^7 + x^3 + 1$
$M(x) = (\text{start bit}) * x^{39} + (\text{host bit}) * x^{38} + ... + (\text{last bit before CRC}) * x^0$
$CRC[6...0] = \text{Remainder}[(M(x) * x^7)/G(x)]$

5.2.2. Command Classes

As in MultiMediaCard Bus mode, the SPI commands are divided into several classes (See Table 5-1). Each class supports a set of device functions. A TriFlash device will support the same set of optional command classes in both communication modes (there is only one command class table in the CSD register). The available command classes, and the supported commands for a specific class, however, are different in the MultiMediaCard Bus and the SPI communication mode.

NOTE: Except the classes that are not supported in SPI mode (class 1, 3 and 9), the mandatory required classes for the MultiMediaCard Bus mode are the same for the SPI mode.

Table 5-1. Command Classes in SPI Mode

Card CMD Class (CCC)	Class Description	Supported Commands																						
		0	1	9	10	12	13	16	17	18	24	25	27	28	29	30	32	33	38	42	55	56	58	59
class 0	Basic	+	+	+	+	+	+																+	+
class 1	Not supported in SPI																							
class 2	Block read							+	+	+														
class 3	Not supported in SPI																							
class 4	Block write										+	+	+											
class 5	Erase																+	+	+					
class 6	Write-protection (Optional)													+	+	+								
class 7	Lock Card (Optional)																			+				
class 8	Application specific[1]																				+	+		
class 9	Not supported in SPI																							
class 10-11	Reserved																							

5.2.2.1. Detailed Command Description

Table 5-2 provides a detailed description of the SPI bus commands. The responses are defined in section 6.2.3. The table below lists all TriFlash commands. A "yes" in the SPI mode column indicates that the command is supported in SPI mode. With these restrictions, the command class description in the CSD is still valid. If a command does not require an argument, the value of this field should be set to zero. The reserved commands are reserved in MultiMediaCard Bus mode as well.

The command number is the base-10 equivalent of the binary code of the command. As an example, the content of the **Command** field for CMD0 is (binary) '000000' and for CMD39 is (binary) '100111.'

Table 5-2. Description of SPI Bus Commands

CMD INDEX	SPI Mode	Argument	Resp	Abbreviation	Command Description
CMD0	Yes	None	R1	GO_IDLE_STATE	Resets the TriFlash
CMD1	Yes	None	R1	SEND_OP_COND	Activates the device's initialization process.
CMD2	No				
CMD3	No				
CMD4	No				
CMD5	Reserved				
CMD6	Reserved				
CMD7	No				
CMD8	Reserved				

[1] The application specific command is currently not supported in the TriFlash.

CMD INDEX	SPI Mode	Argument	Resp	Abbreviation	Command Description
CMD9	Yes	None	R1	SEND_CSD	Asks the selected device to send its card-specific data (CSD).
CMD10	Yes	None	R1	SEND_CID	Asks the selected device to send its card identification (CID).
CMD11	No				
CMD12	Yes	None	R1b	STOP_ TRANSMISSION	Forces the device to stop transmission during a multiple block read operation.
CMD13	Yes	None	R2	SEND_STATUS	Asks the selected device to send its status register.
CMD14	No				
CMD15	No				
CMD16	Yes	[31:0] block length	R1	SET_BLOCKLEN	Selects a block length (in bytes) for all following block commands (read and write).[1]
CMD17	Yes	[31:0] data address	R1	READ_SINGLE_ BLOCK	Reads a block of the size selected by the SET_BLOCKLEN command.[2]
CMD18	Yes	[31:0] data address	R1	READ_MULTIPLE_ BLOCK	Continuously transfers data blocks from device to host until interrupted by a STOP_ TRANSMISSION command.
CMD19	Reserved				
CMD20	No				
CMD21 to CMD23	Reserved				
CMD24	Yes	[31:0] data address	R1[3]	WRITE_BLOCK	Writes a block of the size selected by the SET_BLOCKLEN command.[4]
CMD25	Yes	[31:0] data address	R1	WRITE_MULTIPLE_BLOCK	Continuously writes blocks of data until a stop transmission token is sent (instead of 'start block').
CMD26	No				
CMD27	Yes	None	R1	PROGRAM_CSD	Programming of the programmable bits of the CSD.
CMD28	Yes	[31:0] data address	R1b	SET_WRITE_PROT	If the device has write protection features, this command sets the write protection bit of the addressed group. The properties of write protection are coded in the card specific data (WP_GRP_SIZE).
CMD29	Yes	[31:0] data address	R1b	CLR_WRITE_PROT	If the device has write protection features, this command clears the write protection bit of the

[1] The only valid block length for write is 512 bytes. The valid block length for read is 1 to 512 bytes. A set block length of less than 512 bytes will cause a write error. The device has a default block length of 512 bytes. CMD16 is not mandatory if the default is accepted.

[2] The start address and block length must be set so that the data transferred will not cross a physical block boundary.

[3] Data followed by data response plus busy.

[4] The start address must be aligned on a sector boundary. The block length is always 512 bytes.

CMD INDEX	SPI Mode	Argument	Resp	Abbreviation	Command Description
					addressed group.
CMD30	Yes	[31:0] write protect data address	R1	SEND_WRITE_ PROT	If the device has write protection features, this command asks the device to send the status of the write protection bits.[1]
CMD31	Reserved				
CMD32	Yes	[31:0] data address	R1	ERASE_WR_BLK_START_ ADDR	Sets the address of the first write block to be erased.
CMD33	Yes	[31:0] data address	R1	ERASE_WR_BLK_END_AD DR	Sets the address of the last write block in a continuous range to be erased.
CMD34 to CMD37	Reserved				
CMD38	Yes	[31:0] do not care[2]	R1b	ERASE	Erases all previously selected write blocks.
CMD39	No				
CMD40	No				
CMD41	Reserved				
CMD42	Yes	[31:0] stuff bits	R1b	LOCK_UNLOCK	Set/reset the password or lock/unlock the card. The size of the data block is defined by the SET_BLOCK_LEN command.
CMD43 to CMD54	Reserved				
CMD55	Yes	[31:0] stuff bits	R1	APP_CMD	Notifies the device that the next command is an application specific command rather than a standard command.
CMD56	Yes	[31:0] stuff bits [0]: RD/WR.[3]	R1	GEN_CMD	Used either to transfer a Data Block to the device or to get a Data Block from the device for general purpose/application specific commands. The size of the Data Block is defined with SET_BLOCK_LEN command.
CMD57	Reserved				
CMD58	Yes	None	R3	READ_OCR	Reads the OCR register of a device.
CMD59	Yes	[31:1] do not care [0:0] CRC option	R1	CRC_ON_OFF	Turns the CRC option on or off. A '1' in the CRC option bit will turn the option on, a '0' will turn it off
CMD60-63	No				

5.2.3. Responses

Several types of response tokens exist. As in the MultiMediaCard Bus mode, all are transmitted MSB first.

[1] 32 write protection bits (representing 32 write protect groups starting at the specified address) followed by 16 CRC bits are transferred in a payload format via the data line.

[2] Do not care = the bit places must be filled but the value is irrelevant.

[3] RD/WR_: "1"=the host will get a block of data from the device. "0"=the host sends a block of data to the device.

5.2.3.1. Format R1

This response token is sent by the device after every command with the exception of SEND_STATUS commands. It is 1 byte long, the MSB is always set to zero and the other bits are error indications. A '1' signals error.

The structure of the R1 format is given in Figure 5-8.

- In idle state: The device is in idle state and running initializing process.
- Erase reset: An erase sequence was cleared before executing because an out of erase sequence command was received.
- Illegal command: An illegal command code was detected.
- Communication CRC error: The CRC check of the last command failed.
- Erase sequence error: An error in the sequence of erase commands occurred.
- Address error: A misaligned address, which did not match the block length was used in the command.
- Parameter error: The command's argument (e.g., address, block length) was out of the allowed range for this device.

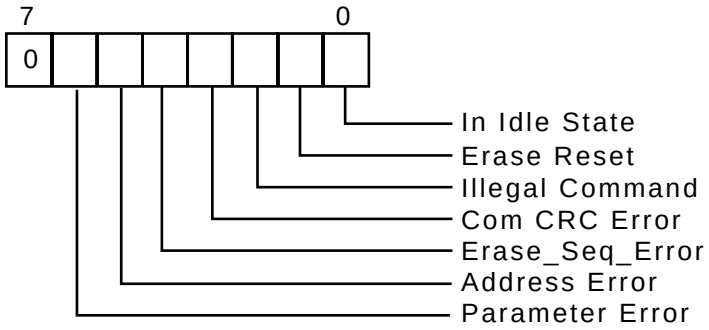


Figure 5-8. R1 Response Format

5.2.3.2. Format R1b

This response token is identical to R1 format with the optional addition of the busy signal. The busy signal token can be any number of bytes. A zero value indicates device is busy. A non-zero value indicates device is ready for the next command.

5.2.3.3. Format R2

This 2-bytes long response token is sent by the device as a response to the SEND_STATUS command. The format of the R2 status is shown in Figure 5-9.

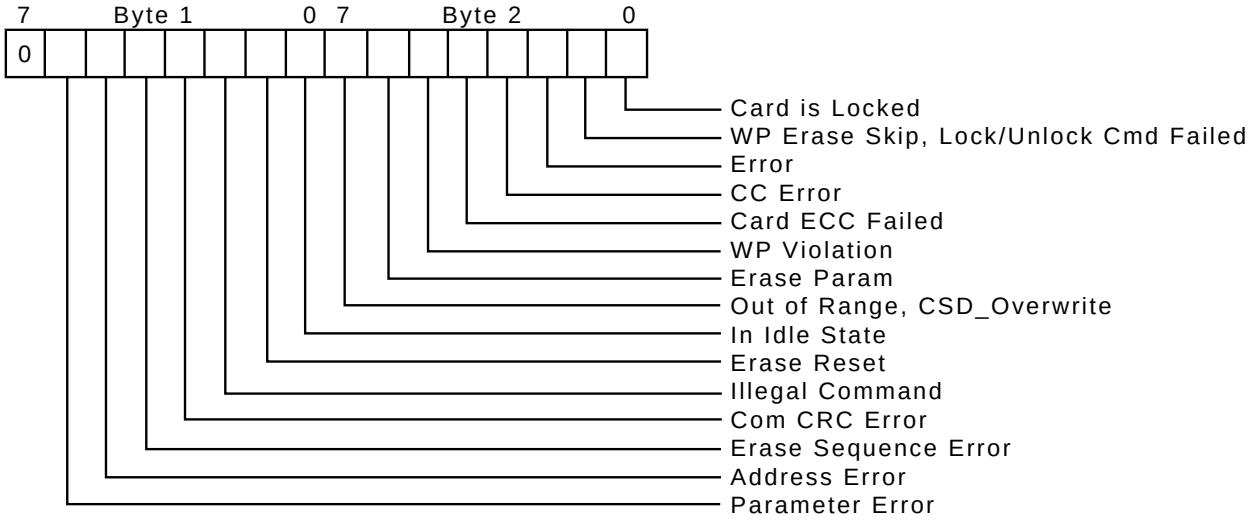


Figure 5-9. R2 Response Format

The first byte is identical to response R1. The content of the second byte is described below:

- **Erase param**—An invalid selection, sectors for erase.
- **Write protect violation**—The command tried to write a write-protected block.
- **Device ECC failed**—Device internal ECC was applied but failed to correct the data.
- **CC error**—Internal device controller error.
- **Error**—A general or an unknown error occurred during the operation.
- **Write protect erase skip**—Only partial address space was erased due to existing WP blocks.
- **Card is locked**—not supported by the SanDisk TriFlash.

5.2.3.4. Format R3

This response token is sent by the device when a READ_OCR command is received. The response length is 5 bytes. The structure of the first (MSB) byte is identical to response type R1. The other four bytes contain the OCR register.

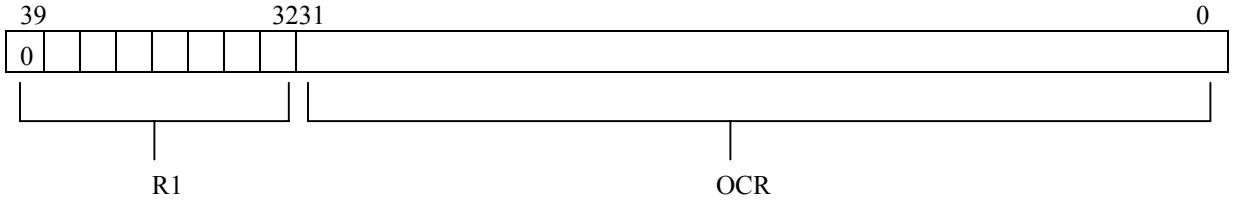
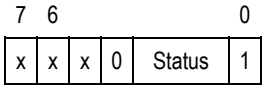


Figure 5-10. R3 Response Format

5.2.3.5. Data Response

Every data block written to the device will be acknowledged by a data response token. It is one byte long and has the following format:



The meaning of the status bits is defined as follows:

- '010'—Data accepted.
- '101'—Data rejected due to a CRC error.
- '110'—Data Rejected due to a Write Error

In case of any error (CRC or Write Error) during Write Multiple Block operation, the host shall stop the data transmission using CMD12. In case of Write Error (response '110') the host may send CMD13 (SEND_STATUS) in order to get the cause of the write problem. ACMD22 can be used to find the number of well written write blocks.

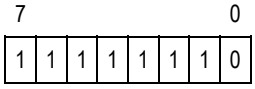
5.2.4. Data Tokens

Read and write commands have data transfers associated with them. Data is being transmitted or received via data tokens. All data bytes are transmitted MSB.

Data tokens are 4 to 515 bytes long and have the following format:

For Single Block Read, Single Block Write and Multiple Block Read:

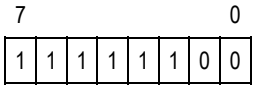
- First byte: Start Block.



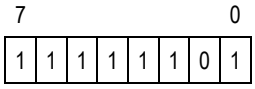
- Bytes 2-513 (depends on the data block length): User data.
- Last two bytes: 16 bit CRC.

For Multiple Block Write Operation:

- First byte of each block.
- If data is to be transferred then—Start Block.



- If Stop transmission is requested—Stop Tran.



NOTE: This format is used only for Multiple Block Write. In case of Multiple Block Read the stop transmission is done using STOP_TRAN Command (CMD12).

5.2.5. Data Error Token

If a read operation fails and the device cannot provide the required data it will send a data error token, instead. The four least significant bits (LSB) are the same error bits as in response format R2. This token is one byte long and has the format shown in Figure 5-11.

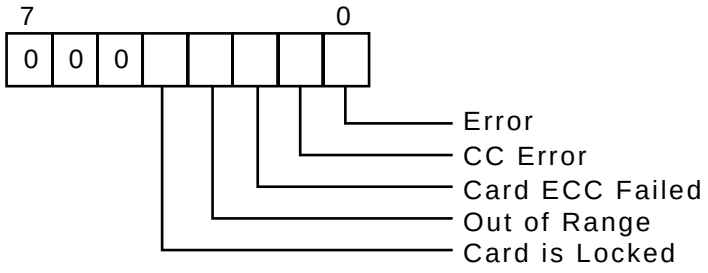


Figure 5-11. Data Error Token

5.2.6. Clearing Status Bits

As described in the previous paragraphs, in SPI mode, status bits are reported to the host in three different formats: response R1, response R2 and data error token (the same bits may exist in multiple response types—e.g., Device ECC failed). As in the MultiMediaCard Bus mode, error bits are cleared when read by the host, regardless of the response format.

5.3. Device Registers

In SPI Mode, only the OCR, CSD and CID registers are accessible. Their format is identical to their format in the MultiMediaCard Bus mode. However, a few fields are irrelevant in SPI mode.

5.4. SPI Bus Timing Diagrams

All timing diagrams use the schematics and abbreviations listed in Table 5-3.

Table 5-3. Timing Diagram Signals

H	Signal is high (logical ‘1’)
L	Signal is low (logical ‘0’)
X	Do not care
Z	high impedance state (-> = 1)
*	repeater
Busy	Busy Token
Command	Command token
Response	Response token
Data block	Data token

All timing values are defined in Table 5-4. The host must keep the clock running for at least NCR clock cycles after the device response is received. This restriction is applied to command and data response tokens.

5.4.1. Command/Response

Host Command to Device Response—Device is Ready

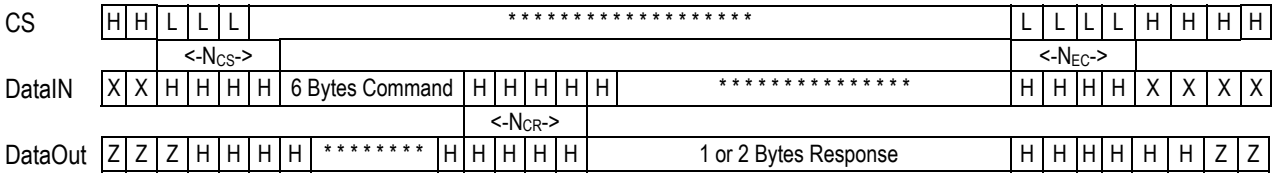


Figure 5-12. Device is Ready Timing

Host Command to Device Response—Device is Busy

The following timing diagram describes the command response transaction for commands when the device responds with the R1b response type (e.g., SET_WRITE_PROT and ERASE). When the device is signaling busy, the host may deselect it (by raising the CS) at any time. The device will release the DataOut line one clock after the CS going high. To check if the device is still busy it needs to be reselected by asserting (set to low) the CS signal. The device will resume busy signal (pulling DataOut low) one clock after the falling edge of CS.

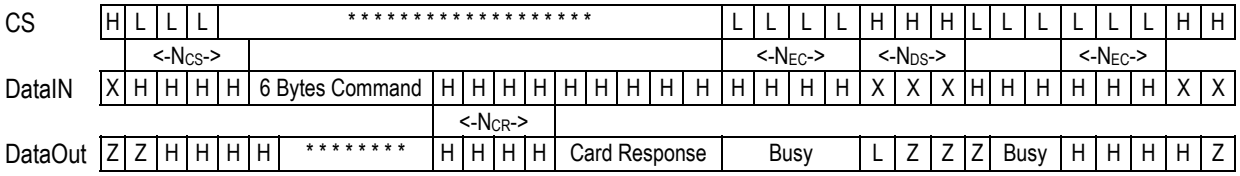


Figure 5-13. Device is Busy Timing

Device Response to Host Command

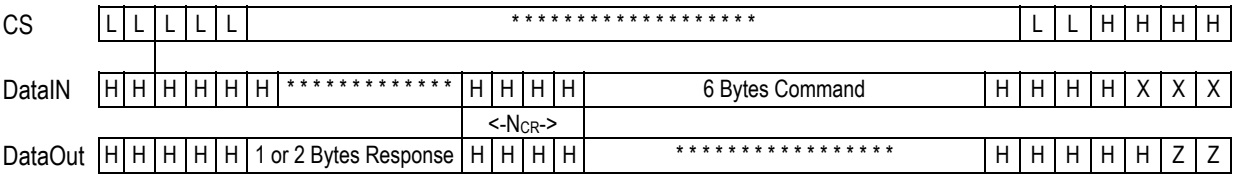


Figure 5-14. Timing of Device Response to Host Command

5.4.2. Data Read

The following timing diagram describes all single block read operations with the exception of SEND_CSD command.

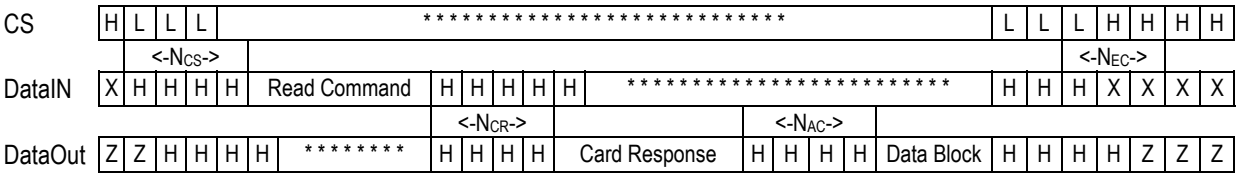


Figure 5-15. Single Block Read Timing

Figure 5-16 describes Stop transmission operation in case of Multiple Block Read.

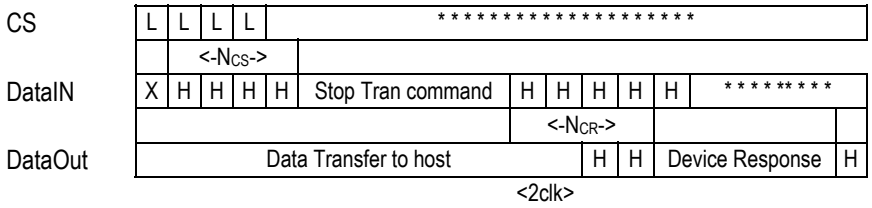


Figure 5-16. Stop Transmission Operation in Multiple Block Read

Reading the CSD Register

Figure 5-17 shows the SEND_CSD command bus transaction. The timeout values for the response and the data block are N_{CR} (Since the N_{AC} is still unknown).

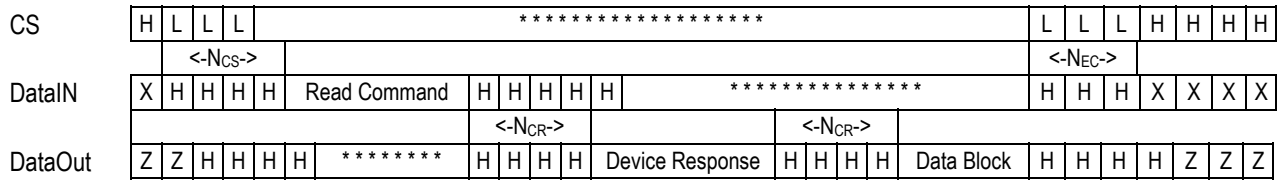


Figure 5-17. Timing of the SEND_CSD Command

5.4.3. Data Write

The host may deselect a device (by raising the CS) at any time during the device busy period (refer to the given timing diagram). The device will release the DataOut line one clock after the CS going high. To check if the device is still busy it needs to be re-selected by asserting (set to low) the CS signal.

The device will resume busy signal (pulling DataOut low) one clock after the falling edge of CS.

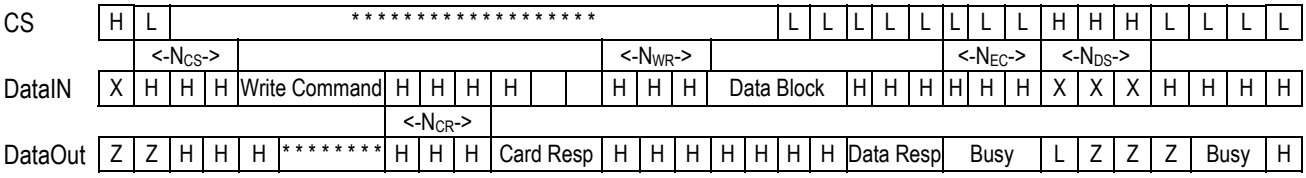


Figure 5-18. Device Write Timing

Figure 5-19 shows the stop transmission operation in Multiple Block Write transfer.

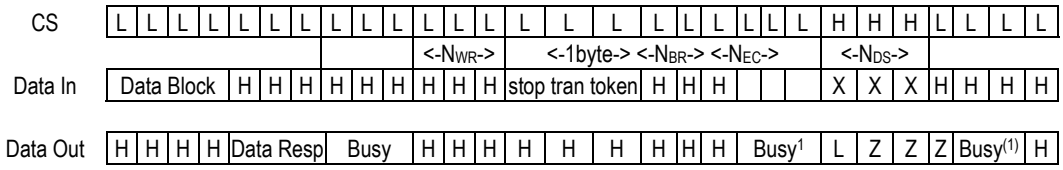


Figure 5-19. Stop Transmission Timing—Multiple Block Write

5.4.4. Timing Values

Table 5-4. Timing Constants Definitions

	Min	Max	Unit
N_{CS}	0	-	8 Clock Cycles
N_{CR}	0	8	8 Clock Cycles
N_{RC}	1	-	8 Clock Cycles
N_{AC}	1	[10*((TAAC*f)+(100*NSAC))]*1/8[2]	8 Clock Cycles
N_{WR}	1	-	8 Clock Cycles
N_{EC}	0	-	8 Clock Cycles
N_{DS}	0	-	8 Clock Cycles
N_{BR}	0	1	8 Clock Cycles

5.5. SPI Electrical Interface

The SPI Mode electrical interface is identical to that of the MultiMediaCard Bus mode.

5.6. SPI Bus Operating Conditions

Identical to MultiMediaCard Bus mode.

5.7. Bus Timing

Identical to MultiMediaCard Bus mode. The timing of the CS signal is the same as any other device input.

[1] The Busy may appear within N_{BR} clocks after Stop Tran Token. If there is no Busy the host may continue to the next command.

[2] Where f is the clock frequency.

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Appendix A. Ordering Information

To order SanDisk products directly from SanDisk, call 408-542-0595.

TriFlash Devices

MMC Model No.	Capacities
SDAT1FAH-128	128 Mb
SDBT1FAH-256	256 Mb
SDBT1FCH-512	512 Mb
SDBT1FCH-1024	1024 Mb

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Appendix B. Technical Support Services

Direct SanDisk Technical Support

Call SanDisk Applications Engineering at 408-542-0405 for technical support.

SanDisk Worldwide Web Site

Internet users can obtain technical support and product information along with SanDisk news and much more from the SanDisk Worldwide Web Site, 24 hours a day, seven days a week. The SanDisk Worldwide Web Site is frequently updated. Visit this site often to obtain the most up-to-date information on SanDisk products and applications. The SanDisk Web Site URL is http://www.sandisk.com.

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Appendix C. SanDisk Worldwide Sales Offices

To order SanDisk products directly from SanDisk, call 408-542-0595.

SanDisk Corporate Headquarters

140 Caspian Court
Sunnyvale, CA 94089
Tel: 408-542-0500
Fax: 408-542-0503
http://www.sandisk.com

U.S. Industrial/OEM Sales Offices

Northwest USA
2241 Fremont Dr., Suite B
Havasu City, AZ 86406
Tel: 928-505-4258
Fax: 928-505-4259

Southwest USA & Mexico
140 Caspian Court
Sunnyvale, CA 94089
Tel: 408-542-0730
Fax: 408-542-0410

North Central USA & South America
134 Cherry creek Circle, Suite 150
Winter Springs, FL 32708
Tel: 407-366-6490
Fax: 407-366-5945

Northeastern USA & Canada
620 Herndon Pkwy. Suite 200
Herndon, VA 22070
Tel: 703-481-9828
Fax: 703-437-9215

U.S. Retail Sales Offices

Americas
10 Flagstone
Trabuco Canyon, CA 92679
Tel: 949-589-8351
Fax: 949-589-8364

Retail Account Sales
32500 Mills Rd.
Avon, OH 44011
Tel: 440-327-0490
Fax: 440-327-0295

International Retail Sales Offices

European Retail Sales
Wilhelminastraat 10
2011 VM Haarlem
The Netherlands
Tel: 31-23-5514226
Fax: 31-23-5348625

Southern European Retail Sales
Centre Hoche Condorcet
3 Rue Condorcet—B.P. 9
91263 Juvisy Sur Orge Cedex
France
Tel: 33-169-12-16-04
Fax: 33-169-12-16-24

Japan Retail Sales
Umeda-Shinmichi Bldg. 10F
1-1-5 Dojima, Kita-ku
Osaka 530-0003
Tel: 81-6-6343-6480
Fax: 81-6-6343-6481

International Industrial/OEM Sales Offices

Europe
SanDisk GmbH
Karlsruher Str. 2C
D-30519 Hannover, Germany
Tel: 49-511-875-9131
Fax: 49-511-875-9187

Northern Europe
Videroegatan 3 B
S-16440 Kista, Sweden
Tel: 46-08-75084-63
Fax: 46-08-75084-26

Central and Southern Europe
Rudolf-Diesel-Str. 3
40822 Mettmann, Germany
Tel: 49-210-495-3433
Fax: 49-210-495-3434

Japan
8F Nisso Bldg. 15
2-17-19 Shin-Yokohama,
Kohoku-ku
Yokohama 222-0033,
Japan
Tel: 81-45-474-0181
Fax: 81-45-474-0371

Asia/Pacific Rim
89 Queensway, Lippo Center
Tower I, Suite 3402
Admiralty, Hong Kong
Tel: 852-2712-0501
Fax: 852-2712-9385

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Appendix D. Limited Warranty

I. WARRANTY STATEMENT

SanDisk warrants its products to be free of any defects in materials or workmanship that would prevent them from functioning properly for one year from the date of purchase. This express warranty is extended by SanDisk Corporation.

II. GENERAL PROVISIONS

This warranty sets forth the full extent of SanDisk's responsibilities regarding the SanDisk TriFlash. In satisfaction of its obligations hereunder, SanDisk, at its sole option, will either repair, replace or refund the purchase price of the product.

NOTWITHSTANDING ANYTHING ELSE IN THIS LIMITED WARRANTY OR OTHERWISE, THE EXPRESS WARRANTIES AND OBLIGATIONS OF SELLER AS SET FORTH IN THIS LIMITED WARRANTY, ARE IN LIEU OF, AND BUYER EXPRESSLY WAIVES ALL OTHER OBLIGATIONS, GUARANTIES AND WARRANTIES OF ANY KIND, WHETHER EXPRESS OR IMPLIED, INCLUDING WITHOUT LIMITATION, ANY IMPLIED WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR INFRINGEMENT, TOGETHER WITH ANY LIABILITY OF SELLER UNDER ANY CONTRACT, NEGLIGENCE, STRICT LIABILITY OR OTHER LEGAL OR EQUITABLE THEORY FOR LOSS OF USE, REVENUE, OR PROFIT OR OTHER INCIDENTAL OR CONSEQUENTIAL DAMAGES, INCLUDING WITHOUT LIMITATION PHYSICAL INJURY OR DEATH, PROPERTY DAMAGE, LOST DATA, OR COSTS OF PROCUREMENT OF SUBSTITUTE GOODS, TECHNOLOGY OR SERVICES. IN NO EVENT SHALL THE SELLER BE LIABLE FOR DAMAGES IN EXCESS OF THE PURCHASE PRICE OF THE PRODUCT, ARISING OUT OF THE USE OR INABILITY TO USE SUCH PRODUCT, TO THE FULL EXTENT SUCH MAY BE DISCLAIMED BY LAW.

SanDisk's products are not warranted to operate without failure. Accordingly, in any use of products in life support systems or other applications where failure could cause injury or loss of life, the products should only be incorporated in systems designed with appropriate redundancy, fault tolerant or back-up features.

III. WHAT THIS WARRANTY COVERS

For products found to be defective within one year of purchase, SanDisk will have the option of repairing or replacing the defective product, if the following conditions are met:

A. The defective product is returned to SanDisk for failure analysis as soon as possible after the failure occurs.
B. An incident card filled out by the user, explaining the conditions of usage and the nature of the failure, accompanies each returned defective product.
C. No evidence is found of abuse or operation of products not in accordance with the published specifications, or of exceeding storage or maximum ratings or operating conditions.

All failing products returned to SanDisk under the provisions of this limited warranty shall be tested to the product's functional and performance specifications. Upon confirmation of failure, each product will be analyzed, by whatever means necessary, to determine the root cause of failure. If the root cause of failure is found to be not covered by the above provisions, then the product will be returned to the customer with a report indicating why the failure was not covered under the warranty.

This warranty does not cover defects, malfunctions, performance failures or damages to the unit resulting from use in other than its normal and customary manner, misuse, accident or neglect; or improper alterations or repairs.

SanDisk reserves the right to repair or replace, at its discretion, any product returned by its customers, even if such product is not covered under warranty, but is under no obligation to do so.

SanDisk may, at its discretion, ship repaired or rebuilt products identified in the same way as new products, provided such cards meet or exceed the same published specifications as new products. Concurrently, SanDisk also reserves the right to market any products, whether new, repaired, or rebuilt, under different specifications and product designations if such products do not meet the original product's specifications.

IV. RECEIVING WARRANTY SERVICE

According to SanDisk's warranty procedure, defective product should be returned only with prior authorization from SanDisk Corporation. Please contact SanDisk's Customer Service department at 408-542-0595 with the following information: product model number and description, nature of defect, conditions of use, proof of purchase and purchase date. If approved, SanDisk will issue a Return Material Authorization or Product Repair Authorization number. Ship the defective product to:

SanDisk Corporation
Attn: RMA Returns
(Reference RMA or PRA #)
140 Caspian Court
Sunnyvale, CA 94089

V. STATE LAW RIGHTS

SOME STATES DO NOT ALLOW THE EXCLUSION OR LIMITATION OF INCIDENTAL OR CONSEQUENTIAL DAMAGES, OR LIMITATION ON HOW LONG AN IMPLIED WARRANTY LASTS, SO THE ABOVE LIMITATIONS OR EXCLUSIONS MAY NOT APPLY TO YOU. This warranty gives you specific rights and you may also have other rights that vary from state to state.