INTEGRATED CIRCUITS

DATA SHEET

TEA5767HN
Low-power FM stereo radio for handheld applications

Preliminary specification
Supersedes data of 2002 Sep 13

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Philips
Semiconductors

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CONTENTS

1 FEATURES

- High sensitivity due to integrated low-noise RF input amplifier
- FM mixer for conversion to IF of the US/Europe (87.5 to 108 MHz) and Japanese (76 to 91MHz) FM band
- Preset tuning to receive Japanese TV audio up to 108 MHz
- RF Automatic Gain Control (AGC) circuit
- LC tuner oscillator operating with low cost fixed chip inductors
- FM IF selectivity performed internally
- No external discriminator needed due to fully integrated FM demodulator
- Crystal reference frequency oscillator; the oscillator operates with a 32.768 kHz clock crystal or with a 13 MHz crystal and with an externally applied 6.5 MHz reference frequency
- PLL synthesizer tuning system
- I^2C-bus and 3-wire bus, selectable via pin BUSMODE
- 7-bit IF counter output via the bus
- 4-bit level information output via the bus
- Soft mute
- Signal dependent mono to stereo blend [Stereo Noise Cancelling (SNC)]
- Signal dependent High Cut Control (HCC)
- Soft mute, SNC and HCC can be switched off via the bus
- Adjustment-free stereo decoder
- Autonomous search tuning function
- Standby mode
- Two software programmable ports
- Bus enable line to switch the bus input and output lines into 3-state mode.

2 GENERAL DESCRIPTION

The TEA5767HN is a single-chip electronically tuned FM stereo radio for low-voltage application with fully integrated IF selectivity and demodulation. The radio is completely adjustment-free and only requires a minimum of small and low cost external components. The radio can be tuned to the European, US and Japanese FM bands.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TEA5767HN	HVQFN40	plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 × 6 × 0.85 mm	SOT618-1

4 QUICK REFERENCE DATA

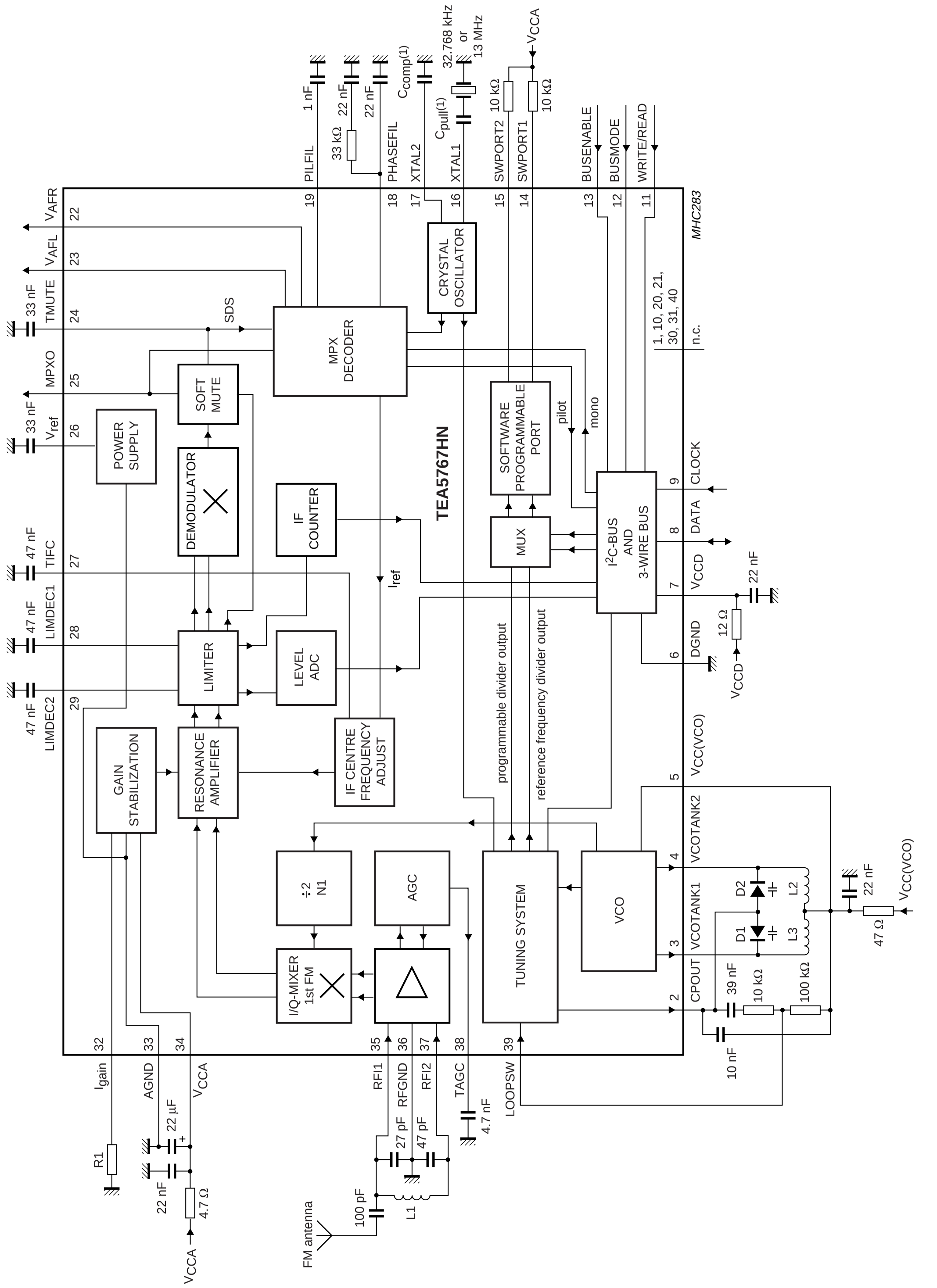
$V_{CCA} = V_{CC(VCO)} = V_{CCD}$.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		2.5	3.0	5.0	V
$V_{CC(VCO)}$	voltage controlled oscillator supply voltage		2.5	3.0	5.0	V
V_{CCD}	digital supply voltage		2.5	3.0	5.0	V
I_{CCA}	analog supply current	operating; V_{CCA} = 3 V	6.0	8.4	10.5	mA
		standby mode; V_{CCA} = 3 V	–	3	6	µA
$I_{CC(VCO)}$	voltage controlled oscillator supply current	operating; $V_{VCOTANK1} = V_{VCOTANK2}$ = 3 V	560	750	940	µA
		standby mode; $V_{VCOTANK1} = V_{VCOTANK2}$ = 3 V	–	1	2	µA
I_{CCD}	digital supply current	operating; V_{CCD} = 3 V	2.1	3.0	3.9	mA
		standby mode; V_{CCD} = 3 V				
		bus enable line HIGH	30	56	80	µA
		bus enable line LOW	11	19	26	µA
$f_{FM(ant)}$	FM input frequency		76	–	108	MHz
T_{amb}	ambient temperature	$V_{CCA} = V_{CC(VCO)} = V_{CCD}$ = 2.5 to 5 V	–10	–	+75	°C
FM overall system parameters; see Fig.7						
V_{RF}	RF sensitivity input voltage	f_{RF} = 76 to 108 MHz; Δf = 22.5 kHz; f_{mod} = 1 kHz; (S+N)/N = 26 dB; de-emphasis = 75 µs; L = R; B_{AF} = 300 Hz to 15 kHz	–	2	3.5	µV
S_{-200}	LOW side 200 kHz selectivity	Δf = –200 kHz; f_{RF} = 76 to 108 MHz; note 1	32	36	–	dB
S_{+200}	HIGH side 200 kHz selectivity	Δf = +200 kHz; f_{RF} = 76 to 108 MHz; note 1	39	43	–	dB
V_{AFL}; V_{AFR}	left and right audio frequency output voltage	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs	60	75	90	mV
(S+N)/N	maximum signal plus noise-to-noise ratio	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs; B_{AF} = 300 Hz to 15 kHz	54	60	–	dB
$\alpha_{cs(stereo)}$	stereo channel separation	V_{RF} = 1 mV; R = L = 0 or R = 0 and L = 1 including 9% pilot; Δf = 75 kHz; f_{mod} = 1 kHz; data byte 3 bit 3 = 0; data byte 4 bit 1 = 1	24	30	–	dB
THD	total harmonic distortion	V_{RF} = 1 mV; L = R; Δf = 75 kHz; f_{mod} = 1 kHz; de-emphasis = 75 µs	–	0.4	1	%

Note

1. LOW side and HIGH side selectivity can be switched by changing the mixer from HIGH side to LOW side LO injection.

5 BLOCK DIAGRAM



The component list is given in Chapter 14.

(1) C_{comp} and C_{pull} data depends on crystal specification.

Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
CPOUT	2	charge pump output of synthesizer PLL
VCOTANK1	3	voltage controlled oscillator tuned circuit output 1
VCOTANK2	4	voltage controlled oscillator tuned circuit output 2
$V_{CC(VCO)}$	5	voltage controlled oscillator supply voltage
DGND	6	digital ground
V_{CCD}	7	digital supply voltage
DATA	8	bus data line input/output
CLOCK	9	bus clock line input
n.c.	10	not connected
WRITE/READ	11	write/read control input for the 3-wire bus
BUSMODE	12	bus mode select input
BUSENABLE	13	bus enable input
SWPORT1	14	software programmable port 1
SWPORT2	15	software programmable port 2
XTAL1	16	crystal oscillator input 1
XTAL2	17	crystal oscillator input 2
PHASEFIL	18	phase detector loop filter
PILFIL	19	pilot detector low-pass filter
n.c.	20	not connected
n.c.	21	not connected
V_{AFR}	22	right audio frequency output voltage
V_{AFL}	23	left audio frequency output voltage
TMUTE	24	time constant for soft mute
MPXO	25	FM demodulator MPX signal output
V_{ref}	26	reference voltage
TIFC	27	time constant for IF centre adjust
LIMDEC1	28	decoupling IF limiter 1
LIMDEC2	29	decoupling IF limiter 2
n.c.	30	not connected
n.c.	31	not connected
I_{gain}	32	gain control current for IF filter
AGND	33	analog ground
V_{CCA}	34	analog supply voltage
RFI1	35	RF input 1
RFGND	36	RF ground
RFI2	37	RF input 2
TAGC	38	time constant RF AGC
LOOPSW	39	switch output of synthesizer PLL loop filter
n.c.	40	not connected

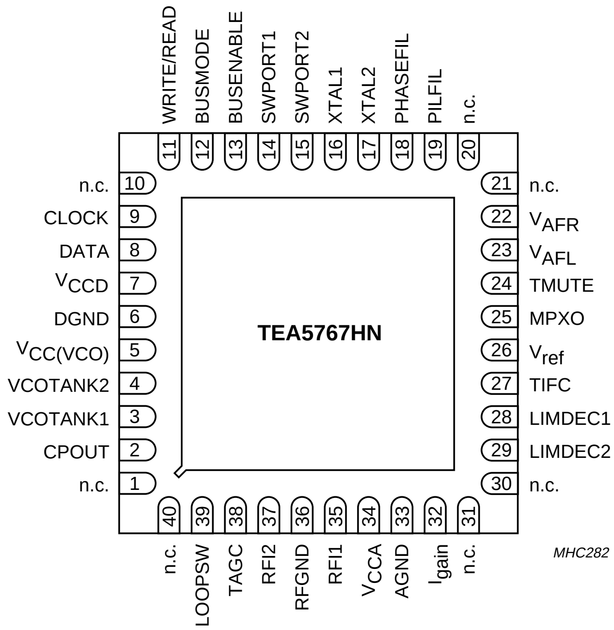


Fig.2 Pin configuration (bottom view).

7 FUNCTIONAL DESCRIPTION

7.1 Low-noise RF amplifier

The LNA input impedance together with the LC RF input circuit defines an FM band filter. The gain of the LNA is controlled by the RF AGC circuit.

7.2 FM mixer

The FM quadrature mixer converts the FM RF (76 to 108 MHz) to an IF of 225 kHz.

7.3 VCO

The varactor tuned LC VCO provides the Local Oscillator (LO) signal for the FM quadrature mixer. The VCO frequency range is 150 to 217 MHz.

7.4 Crystal oscillator

The crystal oscillator can operate with a 32.768 kHz clock crystal or a 13 MHz crystal. The temperature drift of standard 32.768 kHz clock crystals limits the operational temperature range from –10 to +60 °C.

The PLL synthesizer can be clocked externally with a 32.768 kHz, a 6.5 MHz or a 13 MHz signal via pin XTAL2.

The crystal oscillator generates the reference frequency for:

- The reference frequency divider for the synthesizer PLL
- The timing for the IF counter
- The free-running frequency adjustment of the stereo decoder VCO
- The centre frequency adjustment of the IF filters.

7.5 PLL tuning system

The PLL synthesizer tuning system is suitable to operate with a 32.768 kHz or a 13 MHz reference frequency generated by the crystal oscillator or applied to the IC from an external source. The synthesizer can also be clocked via pin XTAL2 at 6.5 MHz. The PLL tuning system can perform an autonomous search tuning function.

7.6 RF AGC

The RF AGC prevents overloading and limits the amount of intermodulation products created by strong adjacent channels.

7.7 IF filter

Fully integrated IF filter.

7.8 FM demodulator

The FM quadrature demodulator has an integrated resonator to perform the phase shift of the IF signal.

7.9 Level voltage generator and analog-to-digital converter

The FM IF analog level voltage is converted to 4 bits digital data and output via the bus.

7.10 IF counter

The IF counter outputs a 7-bit count result via the bus.

7.11 Soft mute

The low-pass filtered level voltage drives the soft mute attenuator at low RF input levels. The soft mute function can be switched off via the bus.

7.12 MPX decoder

The PLL stereo decoder is adjustment-free. The stereo decoder can be switched to mono via the bus.

7.13 Signal dependent mono to stereo blend

With a decreasing RF input level the MPX decoder blends from stereo to mono to limit the output noise. The continuous mono to stereo blend can also be programmed via the bus to an RF level depending switched mono to stereo transition. Stereo Noise Cancelling (SNC) can be switched off via the bus.

7.14 Signal dependent AF response

The audio bandwidth will be reduced with a decreasing RF input level. The function can be switched off via the bus.

7.15 Software programmable ports

Two software programmable ports (open-collector) can be addressed via the bus.

The port 1 (pin SWPORT1) function can be changed with write data byte 4 bit 0 (see Table 13). Pin SWPORT1 is then output for the ready flag of read byte 1.

7.16 I²C-bus and 3-wire bus

The 3-wire and the I²C-bus operate with a maximum clock frequency of 400 kHz.

The I²C-bus mode is selected when pin BUSMODE is LOW, when pin BUSMODE is HIGH the 3-wire bus mode is selected.

8 I²C-BUS, 3-WIRE BUS AND BUS-CONTROLLED FUNCTIONS

8.1 I²C-bus specification

Information about the I²C-bus can be found in the brochure *"The I²C-bus and how to use it"* (order number 9398 393 40011).

The standard I²C-bus specification is expanded by the following definitions.

IC address C0: 1100000.

Structure of the I²C-bus logic: slave transceiver.

Subaddresses are not used.

The maximum LOW-level input and the minimum HIGH-level input are specified to $0.2V_{CCD}$ and $0.45V_{CCD}$ respectively.

The pin BUSMODE must be connected to ground to operate the IC with the I²C-bus.

Note: The bus operates at a maximum clock frequency of 400 kHz. It is not allowed to connect the IC to a bus operating at a higher clock rate.

8.1.1 DATA TRANSFER

Data sequence: address, byte 1, byte 2, byte 3, byte 4 and byte 5 (the data transfer has to be in this order). The LSB = 0 of the address indicates a WRITE operation to the TEA5767HN.

Bit 7 of each byte is considered as the MSB and has to be transferred as the first bit of the byte.

The data becomes valid bitwise at the appropriate falling edge of the clock. A STOP condition after any byte can shorten transmission times.

When writing to the transceiver by using the STOP condition before completion of the whole transfer:

- The remaining bytes will contain the old information
- If the transfer of a byte is not completed, the new bits will be used, but a new tuning cycle will not be started.

The IC can be switched into a low current standby mode with the standby bit; the bus is then still active. The standby current can be reduced by deactivating the bus interface (pin BUSENABLE LOW). If the bus interface is deactivated (pin BUSENABLE LOW) without the standby mode being programmed, the IC maintains normal operation, but is isolated from the bus lines.

The software programmable output (SWPORT1) can be programmed to operate as a tuning indicator output. As long as the IC has not completed a tuning action, pin SWPORT1 remains LOW. The pin becomes HIGH, when a preset or search tuning is completed or when a band limit is reached.

The reference frequency divider of the synthesizer PLL is changed when the MSB in byte 5 is set to logic 1. The tuning system can then be clocked via pin XTAL2 at 6.5 MHz.

8.1.2 POWER-ON RESET

At Power-on reset the mute is set, all other bits are set to LOW. To initialize the IC all bytes have to be transferred.

8.2 I²C-bus protocol

Table 1 Write mode

S(1)	address (write)	A(2)	data byte(s)	A(2)	P(3)

Notes

1. S = START condition.
2. A = acknowledge.
3. P = STOP condition.

Table 2 Read mode

S(1)	address (read)	A(2)	data byte 1

Notes

1. S = START condition.
2. A = acknowledge.

Table 3 IC address byte

IC ADDRESS							**MODE**
1	1	0	0	0	0	0	$R/\overline{W}$(1)

Note

1. Read or write mode:
   a) 0 = write operation to the TEA5767HN
   b) 1 = read operation from the TEA5767HN.

8.3 3-wire bus specification

The 3-wire bus controls the write/read, clock and data lines and operates at a maximum clock frequency of 400 kHz.

Hint: By using the standby bit the IC can be switched into a low current standby mode. In standby mode the IC must be in the WRITE mode. When the IC is switched to READ mode, during standby, the IC will hold the data line down. The standby current can be reduced by deactivating the bus interface (pin BUSENABLE LOW). If the bus interface is deactivated (pin BUSENABLE LOW) without the standby mode being programmed, the IC maintains normal operation, but is isolated from the clock and data line.

8.3.1 DATA TRANSFER

Data sequence: byte 1, byte 2, byte 3, byte 4 and byte 5 (the data transfer has to be in this order).

A positive edge at pin WRITE/READ enables the data transfer into the IC. The data has to be stable at the positive edge of the clock. Data may change while the clock is LOW and is written into the IC on the positive edge of the clock. Data transfer can be stopped after the transmission of new tuning information with the first two bytes or after each following byte.

A negative edge at pin WRITE/READ enables the data transfer from the IC. The WRITE/READ pin changes while the clock is LOW. With the negative edge at pin WRITE/READ the MSB of the first byte occurs at pin DATA. The bits are shifted on the negative clock edge to pin DATA and can be read on the positive edge.

To do two consecutive read or write actions, pin WRITE/READ has to be toggled for at least one clock period. When a search tuning request is sent, the IC autonomously starts searching the FM band; the search direction and search stop level can be selected. When a station with a field-strength equal to or greater than the stop level is found, the tuning system stops and the ready flag bit is set to HIGH. When, during search, a band limit is reached, the tuning system stops at the band limit and the band limit flag bit is set to HIGH. The ready flag is also set to HIGH in this case.

The software programmable output (SWPORT1) can be programmed to operate as a tuning indicator output. As long as the IC has not completed a tuning action pin SWPORT1 remains LOW. The pin becomes HIGH, when a preset or search tuning is completed or when a band limit is reached.

The reference frequency divider of the synthesizer PLL is changed when the MSB in byte 5 is set to logic 1. The tuning system can then be clocked via pin XTAL2 at 6.5 MHz.

8.3.2 POWER-ON RESET

At Power-on reset the mute is set, all other bits are random. To initialize the IC all bytes have to be transferred.

8.4 Writing data

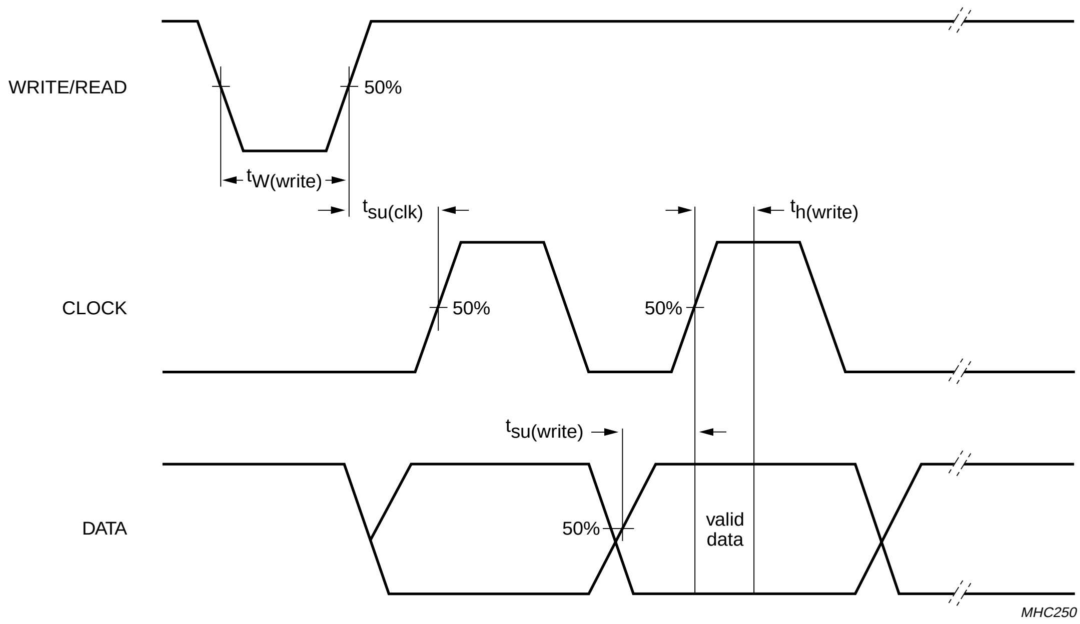


Fig.3 3-wire bus write data.

Table 4 Write mode

DATA BYTE 1	DATA BYTE 2	DATA BYTE 3	DATA BYTE 4	DATA BYTE 5

Table 5 Format of 1st data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
MUTE	SM	PLL13	PLL12	PLL11	PLL10	PLL9	PLL8

Table 6 Description of 1st data byte bits

BIT	SYMBOL	DESCRIPTION
7	MUTE	if MUTE = 1 then L and R audio are muted; if MUTE = 0 then L and R audio are not muted
6	SM	**Search Mode:** if SM = 1 then in search mode; if SM = 0 then not in search mode
5 to 0	PLL[13:8]	setting of synthesizer programmable counter for search or preset

Table 7 Format of 2nd data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0

Table 8 Description of 2nd data byte bits

BIT	SYMBOL	DESCRIPTION
7 to 0	PLL[7:0]	setting of synthesizer programmable counter for search or preset

Table 9 Format of 3rd data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
SUD	SSL1	SSL0	HLSI	MS	MR	ML	SWP1

Table 10 Description of 3rd data byte bits

BIT	SYMBOL	DESCRIPTION
7	SUD	**Search Up/Down:** if SUD = 1 then search up; if SUD = 0 then search down
6 and 5	SSL[1:0]	**Search Stop Level:** see Table 11
4	HLSI	**HIGH/LOW Side Injection:** if HLSI = 1 then HIGH side LO injection; if HLSI = 0 then LOW side LO injection
3	MS	**Mono to Stereo:** if MS = 1 then forced mono; if MS = 0 then stereo ON
2	MR	**Mute Right:** if MR = 1 then the right audio channel is muted and forced mono; if MR = 0 then the right audio channel is not muted
1	ML	**Mute Left:** if ML = 1 then the left audio channel is muted and forced mono; if ML = 0 then the left audio channel is not muted
0	SWP1	**Software programmable port 1:** if SWP1 = 1 then port 1 is HIGH; if SWP1 = 0 then port 1 is LOW

Table 11 Search stop level setting

SSL1	SSL0	SEARCH STOP LEVEL
0	0	not allowed in search mode
0	1	low; level ADC output = 5
1	0	mid; level ADC output = 7
1	1	high; level ADC output = 10

Table 12 Format of 4th data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
SWP2	STBY	BL	XTAL	SMUTE	HCC	SNC	SI

Table 13 Description of 4th data byte bits

BIT	SYMBOL	DESCRIPTION
7	SWP2	**Software programmable port 2:** if SWP2 = 1 then port 2 is HIGH; if SWP2 = 0 then port 2 is LOW
6	STBY	**Standby:** if STBY = 1 then in standby mode; if STBY = 0 then not in standby mode
5	BL	**Band Limits:** if BL = 1 then Japanese FM band; if BL = 0 then US/Europe FM band
4	XTAL	if XTAL = 1 then f_{xtal} = 32.768 kHz; if XTAL = 0 then f_{xtal} = 13 MHz
3	SMUTE	**Soft MUTE:** if SMUTE = 1 then soft mute is ON; if SMUTE = 0 then soft mute is OFF
2	HCC	**High Cut Control:** if HCC = 1 then high cut control is ON; if HCC = 0 then high cut control is OFF
1	SNC	**Stereo Noise Cancelling:** if SNC = 1 then stereo noise cancelling is ON; if SNC = 0 then stereo noise cancelling is OFF
0	SI	**Search Indicator:** if SI = 1 then pin SWPORT1 is output for the ready flag; if SI = 0 then pin SWPORT1 is software programmable port 1

Table 14 Format of 5th data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
PLLREF	DTC	–	–	–	–	–	–

Table 15 Description of 5th data byte bits

BIT	SYMBOL	DESCRIPTION
7	PLLREF	if PLLREF = 1 then the 6.5 MHz reference frequency for the PLL is enabled; if PLLREF = 0 then the 6.5 MHz reference frequency for the PLL is disabled
6	DTC	if DTC = 1 then the de-emphasis time constant is 75 μs; if DTC = 0 then the de-emphasis time constant is 50 μs
5 to 0	–	not used; position is don't care

8.5 Reading data

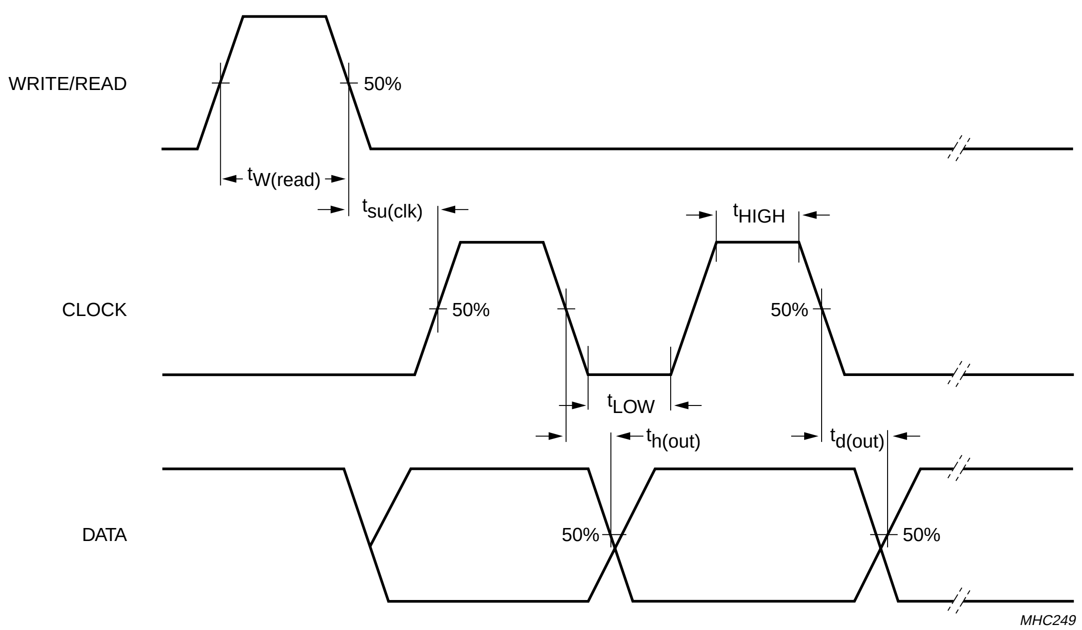


Fig.4 3-wire bus read data.

Table 16 Read mode

DATA BYTE 1	DATA BYTE 2	DATA BYTE 3	DATA BYTE 4	DATA BYTE 5

Table 17 Format of 1st data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
RF	BLF	PLL13	PLL12	PLL11	PLL10	PLL9	PLL8

Table 18 Description of 1st data byte bits

BIT	SYMBOL	DESCRIPTION
7	RF	**Ready Flag:** if RF = 1 then a station has been found or the band limit has been reached; if RF = 0 then no station has been found
6	BLF	**Band Limit Flag:** if BLF = 1 then the band limit has been reached; if BLF = 0 then the band limit has not been reached
5 to 0	PLL[13:8]	setting of synthesizer programmable counter after search or preset

Table 19 Format of 2nd data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0

Table 20 Description of 2nd data byte bits

BIT	SYMBOL	DESCRIPTION
7 to 0	PLL[7:0]	setting of synthesizer programmable counter after search or preset

Table 21 Format of 3rd data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
STEREO	IF6	IF5	IF4	IF3	IF2	IF1	IF0

Table 22 Description of 3rd data byte bits

BIT	SYMBOL	DESCRIPTION
7	STEREO	**Stereo indication:** if STEREO = 1 then stereo reception; if STEREO = 0 then mono reception
6 to 0	PLL[13:8]	IF counter result

Table 23 Format of 4th data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
LEV3	LEV2	LEV1	LEV0	CI3	CI2	CI1	0

Table 24 Description of 4th data byte bits

BIT	SYMBOL	DESCRIPTION
7 to 4	LEV[3:0]	level ADC output
3 to 1	CI[3:1]	**Chip Identification:** these bits have to be set to logic 0
0	–	this bit is internally set to logic 0

Table 25 Format of 5th data byte

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
0	0	0	0	0	0	0	0

Table 26 Description of 5th data byte bits

BIT	SYMBOL	DESCRIPTION
7 to 0	–	reserved for future extensions; these bits are internally set to logic 0

8.6 Bus timing

Table 27 Digital levels and timing

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Digital inputs					
V_{IH}	HIGH-level input voltage		$0.45V_{CCD}$	–	V
V_{IL}	LOW-level input voltage		–	$0.2V_{CCD}$	V
Digital outputs					
$I_{sink(L)}$	LOW-level sink current		500	–	μA
V_{OL}	LOW-level output voltage	I_{OL} = 500 μA	–	450	mV
Timing					
f_{clk}	clock input frequency	I^2C-bus enabled	–	400	kHz
		3-wire bus enabled	–	400	kHz
t_{HIGH}	clock HIGH time	I^2C-bus enabled	1	–	μs
		3-wire bus enabled	1	–	μs
t_{LOW}	clock LOW time	I^2C-bus enabled	1	–	μs
		3-wire bus enabled	1	–	μs
$t_{W(write)}$	pulse width for write enable	3-wire bus enabled	1	–	μs
$t_{W(read)}$	pulse width for read enable	3-wire bus enabled	1	–	μs
$t_{su(clk)}$	clock set-up time	3-wire bus enabled	300	–	ns
$t_{h(out)}$	read mode data output hold time	3-wire bus enabled	10	–	ns
$t_{d(out)}$	read mode output delay time	3-wire bus enabled	–	400	ns
$t_{su(write)}$	write mode set-up time	3-wire bus enabled	100	–	ns
$t_{h(write)}$	write mode hold time	3-wire bus enabled	100	–	ns

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{VCOTANK1}$	VCO tuned circuit output voltage 1		–0.3	+8	V
$V_{VCOTANK2}$	VCO tuned circuit output voltage 2		–0.3	+8	V
V_{CCD}	digital supply voltage		–0.3	+5	V
V_{CCA}	analog supply voltage		–0.3	+8	V
T_{stg}	storage temperature		–55	+150	°C
T_{amb}	ambient temperature		–10	+75	°C
V_{es}	electrostatic handling voltage				
	for all pins except pin DATA	note 1	–200	+200	V
		note 2	–2000	+2000	V
	for pin DATA	note 1	–150	+200	V
		note 2	–2000	+2000	V

Notes

1. Machine model (R = 0 Ω, C = 200 pF).
2. Human body model (R = 1.5 kΩ, C = 100 pF).

10 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	29	K/W

11 DC CHARACTERISTICS

$V_{CCA} = V_{VCOTANK1} = V_{VCOTANK2} = V_{CCD} = 2.7$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply voltages; note 1						
V_{CCA}	analog supply voltage		2.5	3.0	5.0	V
$V_{CC(VCO)}$	voltage controlled oscillator supply voltage		2.5	3.0	5.0	V
V_{CCD}	digital supply voltage		2.5	3.0	5.0	V
Supply currents						
I_{CCA}	analog supply current	operating				
		$V_{CCA} = 3$ V	6.0	8.4	10.5	mA
		$V_{CCA} = 5$ V	6.2	8.6	10.7	mA
		standby mode				
		$V_{CCA} = 3$ V	–	3	6	µA
		$V_{CCA} = 5$ V	–	3.2	6.2	µA
$I_{CC(VCO)}$	voltage controlled oscillator supply current	operating				
		$V_{VCOTANK1} = V_{VCOTANK2} = 3$ V	560	750	940	µA
		$V_{VCOTANK1} = V_{VCOTANK2} = 5$ V	570	760	950	µA
		standby mode				
		$V_{VCOTANK1} = V_{VCOTANK2} = 3$ V	–	1	2	µA
		$V_{VCOTANK1} = V_{VCOTANK2} = 5$ V	–	1.2	2.2	µA
I_{CCD}	digital supply current	operating				
		$V_{CCD} = 3$ V	2.1	3.0	3.9	mA
		$V_{CCD} = 5$ V	2.25	3.15	4.05	mA
		standby mode; $V_{CCD} = 3$ V				
		bus enable line HIGH	30	56	80	µA
		bus enable line LOW	11	19	26	µA
		standby mode; $V_{CCD} = 5$ V				
		bus enable line HIGH	50	78	105	µA
		bus enable line LOW	20	33	45	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DC operating points						
V_{CPOUT}	unloaded DC voltage		0.1	–	$V_{CC(VCO)}$ – 0.1	V
V_{XTAL1}		data byte 4 bit 4 = 1	1.64	1.72	1.8	V
		data byte 4 bit 4 = 0	1.68	1.75	1.82	V
V_{XTAL2}		data byte 4 bit 4 = 1	1.64	1.72	1.8	V
		data byte 4 bit 4 = 0	1.68	1.75	1.82	V
$V_{PHASEFIL}$			0.4	1.2	V_{CCA} – 0.4	V
V_{PILFIL}			0.65	0.9	1.3	V
V_{VAFL}		f_{RF} = 98 MHz; V_{RF} = 1 mV	720	850	940	mV
V_{VAFR}		f_{RF} = 98 MHz; V_{RF} = 1 mV	720	850	940	mV
V_{TMUTE}		V_{RF} = 0 V	1.5	1.65	1.8	V
V_{MPXO}		f_{RF} = 98 MHz; V_{RF} = 1 mV	680	815	950	mV
V_{Vref}			1.45	1.55	1.65	V
V_{TIFC}			1.34	1.44	1.54	V
$V_{LIMDEC1}$			1.86	1.98	2.1	V
$V_{LIMDEC2}$			1.86	1.98	2.1	V
V_{Igain}			480	530	580	mV
V_{RFI1}			0.93	1.03	1.13	V
V_{RFI2}			0.93	1.03	1.13	V
V_{TAGC}		V_{RF} = 0 V	1	1.57	2	V

Note

1. V_{CCA}, $V_{CC(VCO)}$ and V_{CCD} must not differ more than 200 mV.

12 AC CHARACTERISTICS

$V_{CCA} = V_{VCOTANK1} = V_{VCOTANK2} = V_{CCD} = 2.7$ V; $T_{amb} = 25$ °C; measured in the circuit of Fig.7; all AC values are given in RMS; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage controlled oscillator						
f_{osc}	oscillator frequency		150	–	217	MHz
Crystal oscillator						
CIRCUIT INPUT: PIN XTAL2						
$V_{i(osc)}$	oscillator input voltage	oscillator externally clocked	140	–	350	mV
R_i	input resistance	oscillator externally clocked				
		data byte 4 bit 4 = 0	2	3	4	kΩ
		data byte 4 bit 4 = 1	230	330	430	kΩ
C_i	input capacitance	oscillator externally clocked				
		data byte 4 bit 4 = 0	3.9	5.6	7.3	pF
		data byte 4 bit 4 = 1	5	6	7	pF
CRYSTAL: 32.768 kHz						
f_r	series resonance frequency	data byte 4 bit 4 = 1	–	32.768	–	kHz
$\Delta f/f_r$	frequency deviation		-20×10^{-6}	–	$+20 \times 10^{-6}$	
C_0	shunt capacitance		–	–	3.5	pF
R_S	series resistance		–	–	80	kΩ
$\Delta f_r/f_{r(25\ °C)}$	temperature drift	-10 °C < T_{amb} < +60 °C	-50×10^{-6}	–	$+50 \times 10^{-6}$	
CRYSTAL: 13 MHZ						
f_r	series resonance frequency	data byte 4 bit 4 = 0	–	13	–	MHz
$\Delta f/f_r$	frequency deviation		-30×10^{-6}	–	$+30 \times 10^{-6}$	
C_0	shunt capacitance		–	–	4.5	pF
C_{mot}	motional capacitance		1.5	–	3.0	fF
R_S	series resistance		–	–	100	Ω
$\Delta f_r/f_{r(25\ °C)}$	temperature drift	-40 °C < T_{amb} < +85 °C	-30×10^{-6}	–	$+30 \times 10^{-6}$	
Synthesizer						
PROGRAMMABLE DIVIDER; note 1						
N_{prog}	programmable divider ratio	data byte 1 = XX111111; data byte 2 = 11111110	–	–	8191	
		data byte 1 = XX010000; data byte 2 = 00000000	2048	–	–	
ΔN_{step}	programmable divider step size		–	1	–	
REFERENCE FREQUENCY DIVIDER						
N_{ref}	crystal oscillator divider ratio	data byte 4 bit 4 = 0	–	260	–	
		data byte 5 bit 7 = 1; data byte 4 bit 4 = 0	–	130	–	
		data byte 4 bit 4 = 1	–	1	–	

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
CHARGE PUMP: PIN CPOUT						
I_{sink}	charge pump peak sink current	0.2 V < V_{CPOUT} < $V_{VCOTANK2}$ – 0.2 V; $f_{VCO} > f_{ref} \times N_{prog}$	–	0.5	–	μA
I_{source}	charge pump peak source current	0.2 V < V_{CPOUT} < $V_{VCOTANK2}$ – 0.2 V; $f_{VCO} < f_{ref} \times N_{prog}$	–	–0.5	–	μA
IF counter						
V_{RF}	RF input voltage for correct IF count		–	12	18	μV
N_{IF}	IF counter length		–	7	–	bit
$N_{precount}$	IF counter prescaler ratio		–	64	–	
$T_{count(IF)}$	IF counter period	f_{xtal} = 32.768 kHz	–	15.625	–	ms
		f_{xtal} = 13 MHz	–	15.754	–	ms
$RES_{count(IF)}$	IF counter resolution	f_{xtal} = 32.768 kHz	–	4.096	–	kHz
		f_{xtal} = 13 MHz	–	4.0625	–	kHz
IF_{count}	IF counter result for search tuning stop	f_{xtal} = 32.768 kHz	31	–	3E	HEX
		f_{xtal} = 13 MHz	32	–	3D	HEX
Pins DATA, CLOCK, WRITE/READ, BUSMODE and BUSENABLE						
R_i	input resistance		10	–	–	MΩ
Software programmable ports						
PIN SWPORT1						
$I_{sink(max)}$	maximum sink current	data byte 4 bit 0 = 0; data byte 5 bit 0 = 0; $V_{SWPORT1}$ < 0.5 V	500	–	–	μA
$I_{leak(max)}$	maximum leakage current	data byte 4 bit 0 = 1; $V_{SWPORT1}$ < 5 V	–1	–	+1	μA
PIN SWPORT2						
$I_{sink(max)}$	maximum sink current	data byte 5 bit 7 = 0; $V_{SWPORT1}$ < 0.5 V	500	–	–	μA
$I_{leak(max)}$	maximum leakage current	data byte 5 bit 1 = 1; $V_{SWPORT1}$ < 5 V	–1	–	+1	μA
FM signal channel						
FM RF INPUT						
R_i	input resistance at pins RFI1 and RFI2 to RFGND		75	100	125	Ω
C_i	input capacitance at pins RFI1 and RFI2 to RFGND		2.5	4	6	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{RF}	RF sensitivity input voltage	f_{RF} = 76 to 108 MHz; Δf = 22.5 kHz; f_{mod} = 1 kHz; (S+N)/N = 26 dB; de-emphasis = 75 µs; B_{AF} = 300 Hz to 15 kHz	–	2	3.5	µV
$IP3_{in}$	in-band 3rd-order intercept point related to $V_{RFI1-RFI2}$ (peak value)	Δf_1 = 200 kHz; Δf_2 = 400 kHz; f_{tune} = 76 to 108 MHz	81	84	–	dBµV
$IP3_{out}$	out-band 3rd-order intercept point related to $V_{RFI1-RFI2}$ (peak value)	Δf_1 = 4 MHz; Δf_2 = 8 Hz; f_{tune} = 76 to 108 MHz	82	85	–	dBµV
RF AGC						
V_{RF1}	RF input voltage for start of AGC	f_{RF1} = 93 MHz; f_{RF2} = 98 MHz; V_{RF2} = 50 dBµV; $\left\lvert \frac{\Delta V_{TMUTE}}{V_{RF1}} \right\rvert < \frac{14\ mV}{3\ dB\mu V}$; note 2	66	72	78	dBµV
IF filter						
f_{IF}	IF filter centre frequency		215	225	235	kHz
B_{IF}	IF filter bandwidth		85	94	102	kHz
S_{+200}	HIGH side 200 kHz selectivity	Δf = +200 kHz; f_{tune} = 76 to 108 MHz; note 3	39	43	–	dB
S_{-200}	LOW side 200 kHz selectivity	Δf = –200 kHz; f_{tune} = 76 to 108 MHz; note 3	32	36	–	dB
S_{+100}	HIGH side 100 kHz selectivity	Δf = +100 kHz; f_{tune} = 76 to 108 MHz; note 3	8	12	–	dB
S_{-100}	LOW side 100 kHz selectivity	Δf = –100 kHz; f_{tune} = 76 to 108 MHz; note 3	8	12	–	dB
IR	image rejection	f_{tune} = 76 to 108 MHz; V_{RF} = 50 dBµV	24	30	–	dB
FM IF level detector and mute voltage						
V_{RF}	RF input voltage for start of level ADC	read mode data byte 4 bit 4 = 1	2	3	5	µV
ΔV_{step}	level ADC step size		2	3	5	dB
PIN TMUTE						
V_{level}	level output DC voltage	V_{RF} = 0 µV	1.55	1.65	1.80	V
		V_{RF} = 3 µV	1.60	1.70	1.85	V
$V_{level(slope)}$	slope of level voltage	V_{RF} = 10 to 500 µV	150	165	180	$\frac{mV}{20\ dB}$
R_o	output resistance		280	400	520	kΩ

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
FM demodulator: pin MPXO						
V_{MPXO}	demodulator output voltage	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 μs; B_{AF} = 300 Hz to 15 kHz	60	75	90	mV
(S+N)/N	maximum signal plus noise-to-noise ratio	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 μs; B_{AF} = 300 Hz to 15 kHz	54	60	–	dB
THD	total harmonic distortion	V_{RF} = 1 mV; L = R; Δf = 75 kHz; f_{mod} = 1 kHz; de-emphasis = 75 μs	–	0.5	1.5	%
α_{AM}	AM suppression	V_{RF} = 300 μV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; m = 0.3; de-emphasis = 75 μs; B_{AF} = 300 Hz to 15 kHz	40	–	–	dB
R_o	demodulator output resistance		–	–	500	Ω
I_{sink}	demodulator output sink current		–	–	30	μA
Soft mute						
V_{RF}	RF input voltage for soft mute start	α_{mute} = 3 dB; data byte 4 bit 3 = 1	3	5	10	μV
α_{mute}	mute attenuation	V_{RF} = 1 μV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz de-emphasis = 75 μs; B_{AF} = 300 Hz to 15 kHz; data byte 4 bit 3 = 1	10	20	30	dB
MPX decoder						
V_{AFL}; V_{AFR}	left and right audio frequency output voltage	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 μs	60	75	90	mV
R_{AFL}; R_{AFR}	left and right audio frequency output resistance		–	–	50	Ω
$I_{sink(AFL)}$; $I_{sink(AFR)}$	left and right audio frequency output sink current		170	–	–	μA
$V_{MPXIN(max)}$	input overdrive margin	THD < 3%	4	–	–	dB
V_{AFL}/V_{AFR}	left and right audio frequency output voltage difference	V_{RF} = 1 mV; L = R; Δf = 75 kHz; f_{mod} = 1 kHz; de-emphasis = 75 μs	–1	–	+1	dB
$\alpha_{cs(stereo)}$	stereo channel separation	V_{RF} = 1 mV; R = L = 0 or R = 0 and L = 1 including 9% pilot; Δf = 75 kHz; f_{mod} = 1 kHz; data byte 3 bit 3 = 0; data byte 4 bit 1 = 1	24	30	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
(S+N)/N	maximum signal plus noise-to-noise ratio	V_{RF} = 1 mV; L = R; Δf = 22.5 kHz; f_{mod} = 1 kHz; de-emphasis = 75 μs; B_{AF} = 300 Hz to 15 kHz	54	60	–	dB
THD	total harmonic distortion	V_{RF} = 1 mV; L = R; Δf = 75 kHz; f_{mod} = 1 kHz; de-emphasis = 75 μs	–	0.4	1	%
α_{pilot}	pilot suppression measured at pins V_{AFL} and V_{AFR}	related to Δf = 75 kHz; f_{mod} = 1 kHz; de-emphasis = 75 μs	40	50	–	dB
Δf_{pilot}	stereo pilot frequency deviation	V_{RF} = 1 mV; read mode; data byte 3				
		bit 7 = 1	–	3.6	5.8	kHz
		bit 7 = 0	1	3	–	kHz
$\frac{\Delta f_{pilot1}}{\Delta f_{pilot2}}$	pilot switch hysteresis	V_{RF} = 1 mV	2	–	–	dB
HIGH CUT CONTROL						
TC_{de-em}	de-emphasis time constant	V_{RF} = 1 mV				
		data byte 5 bit 2 = 0	38	50	62	μs
		data byte 5 bit 2 = 1	57	75	93	μs
		V_{RF} = 1 μV				
		data byte 5 bit 2 = 0	114	150	186	μs
		data byte 5 bit 2 = 1	171	225	279	μs
MONO TO STEREO BLEND CONTROL						
$\alpha_{cs(stereo)}$	stereo channel separation	V_{RF} = 45 μV; R = L = 0 or R = 0 and L = 1 including 9% pilot; Δf = 75 kHz; f_{mod} = 1 kHz; data byte 3 bit 3 = 0; data byte 4 bit 1 = 1	4	10	16	dB
MONO TO STEREO SWITCHED						
$\alpha_{cs(stereo)}$	stereo channel separation switching from mono to stereo with increasing RF input level	V_{RF} = 1 μV; R = L = 0 or R = 0 and L = 1 including 9% pilot; Δf = 75 kHz; f_{mod} = 1 kHz; data byte 3 bit 3 = 0; data byte 4 bit 1 = 0	24	–	–	dB
$\alpha_{cs(stereo)}$	stereo channel separation switching from stereo to mono with decreasing RF input level	V_{RF} = 20 μV; R = L = 0 or R = 0 and L = 1 including 9% pilot; Δf = 75 kHz; f_{mod} = 1 kHz; data byte 3 bit 3 = 0; data byte 4 bit 1 = 0	–	–	1	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BUS-DRIVEN MUTE FUNCTIONS						
Tuning mute						
α_{mute}	V_{AFL} and V_{AFR} muting depth	data byte 1 bit 7 = 1	–	–	–60	dB
$\alpha_{mute(L)}$	V_{AFL} muting depth	data byte 3 bit 1 = 1; f_{AF} = 1 kHz; $R_{load(L)} < 30$ kΩ	–	–	–80	dB
$\alpha_{mute(R)}$	V_{AFR} muting depth	data byte 3 bit 2 = 1; f_{AF} = 1 kHz; $R_{load(R)} < 30$ kΩ	–	–	–80	dB

Notes

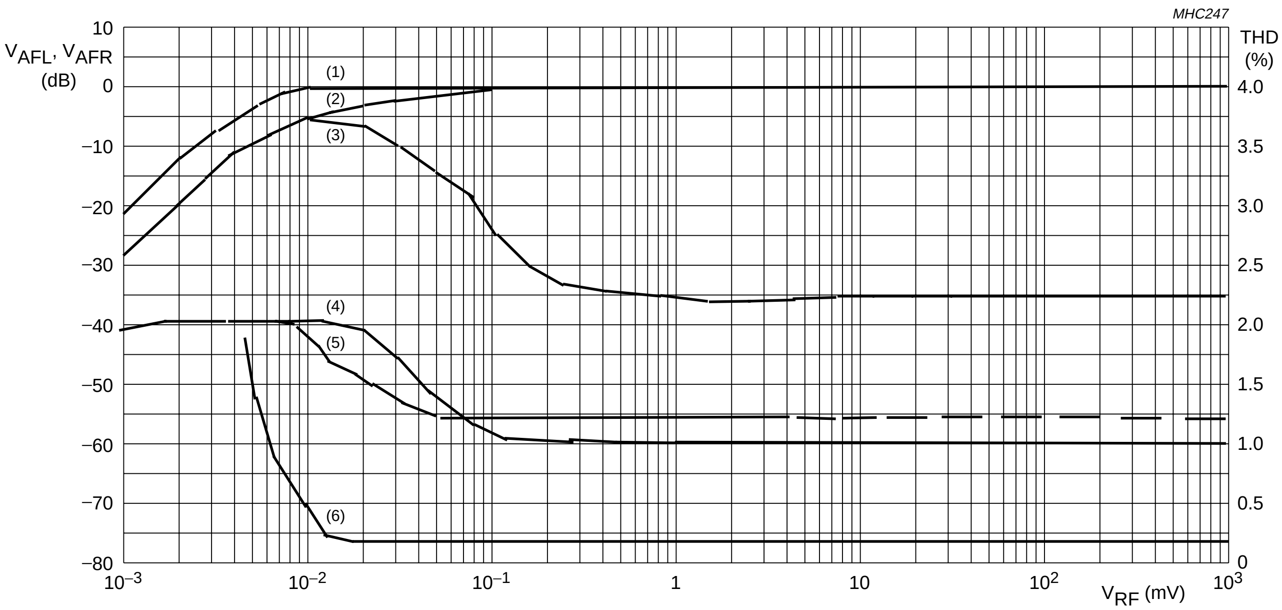
1. Calculation of this 14-bit word can be done as follows:

   formula for HIGH side injection: $N = \frac{4 \times (f_{RF} + f_{IF})}{f_{ref}}$; formula for LOW side injection: $N = \frac{4 \times (f_{RF} - f_{IF})}{f_{ref}}$

   where:
   N = decimal value of PLL word
   f_{RF} = the wanted tuning frequency [Hz]
   f_{IF} = the intermediate frequency [Hz] = 225 kHz
   f_{ref} = the reference frequency [Hz] = 32.768 kHz for the 32.768 kHz crystal; f_{ref} = 50 kHz for the 13 MHz crystal or when externally clocked with 6.5 MHz.

   Example for receiving a channel at 100 MHz with HIGH side injection: $N = \frac{4 \times (100 \times 10^6 + 225 \times 10^3)}{32768} = 12234$.

   The PLL word becomes 2FCAH.
2. V_{RF} in Fig.7 is replaced by $V_{RF1} + V_{RF2}$. The radio is tuned to 98 MHz (HIGH side injection).
3. LOW side and HIGH side selectivity can be switched by changing the mixer from HIGH side to LOW side LO injection.



(1) Mono signal; soft mute on.

(2) Left channel with modulation left; SNC on.

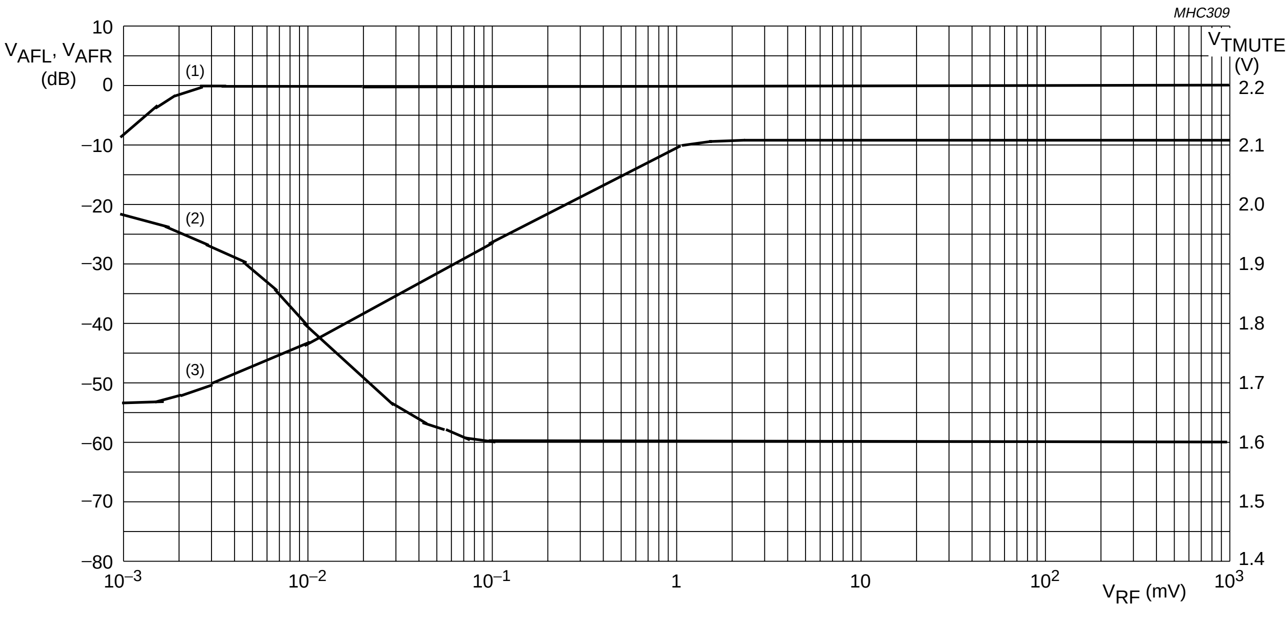
(3) Right channel with modulation left; SNC on.

(4) Noise in mono mode; soft mute on.

(5) Noise in stereo mode; SNC on.

(6) Total harmonic distortion; Δf = 75 kHz; L = R; f_{mod} = 1 kHz.

Fig.5 FM characteristics 1.



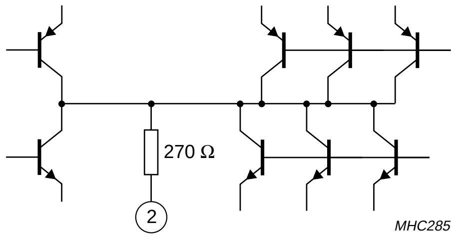
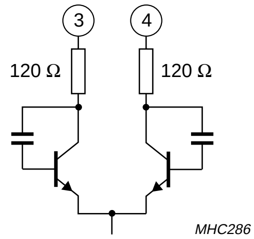
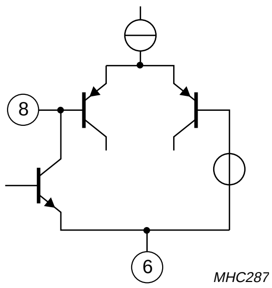
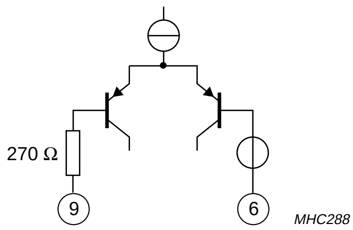
(1) Mono signal; no soft mute.

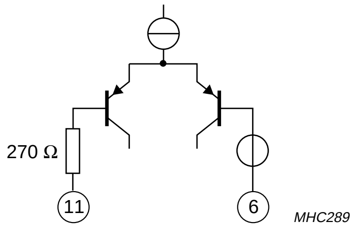
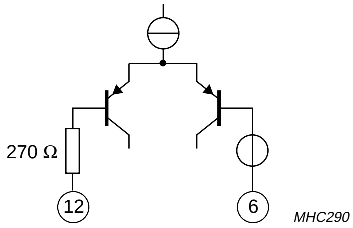
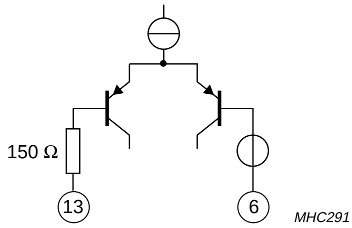
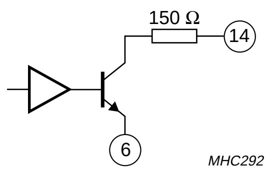
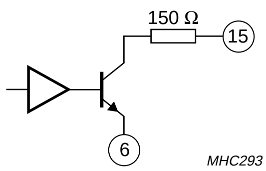
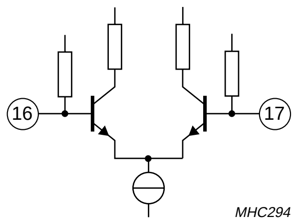
(2) Noise in mono mode; no soft mute.

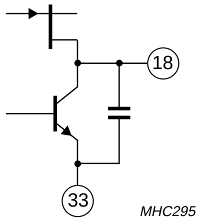
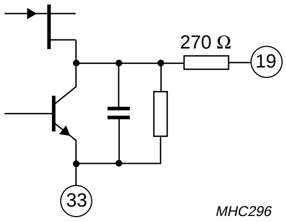
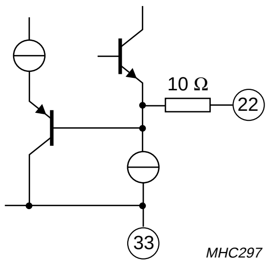
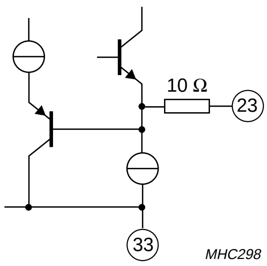
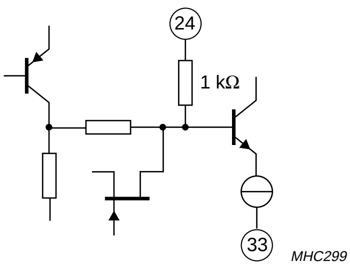
(3) Level voltage; V_{CCA} = 2.7 V.

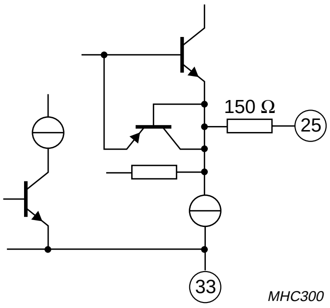
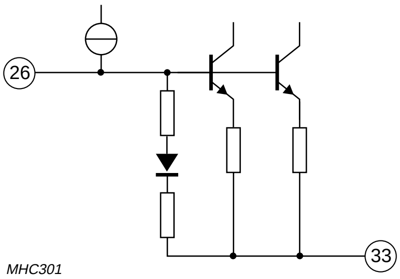
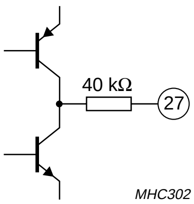
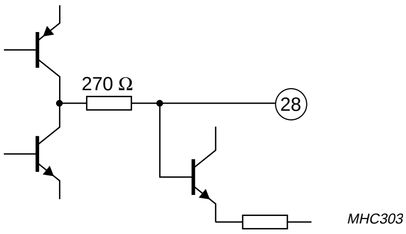
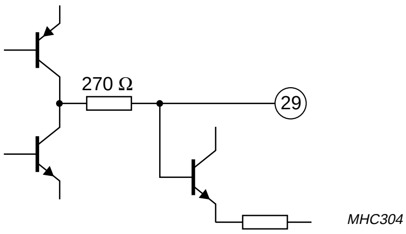
Fig.6 FM characteristics 2.

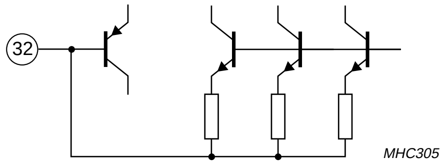
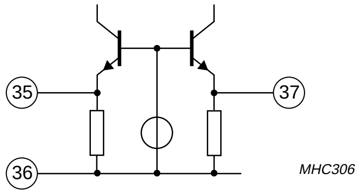
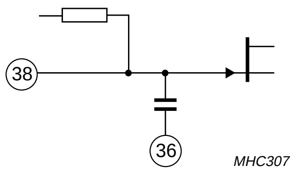
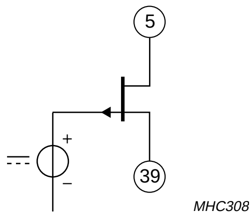
13 INTERNAL PIN CONFIGURATION

PIN	SYMBOL	EQUIVALENT CIRCUIT
1	n.c.	
2	CPOUT	
3	VCOTANK1	
4	VCOTANK2	
5	$V_{CC(VCO)}$	
6	DGND	
7	V_{CCD}	
8	DATA	
9	CLOCK	
10	n.c.	

PIN	SYMBOL	EQUIVALENT CIRCUIT
11	WRITE/READ	
12	BUSMODE	
13	BUSENABLE	
14	SWPORT1	
15	SWPORT2	
16	XTAL1	
17	XTAL2	

PIN	SYMBOL	EQUIVALENT CIRCUIT
18	PHASEFIL	
19	PILFIL	
20	n.c.	
21	n.c.	
22	V_{AFR}	
23	V_{AFL}	
24	TMUTE	

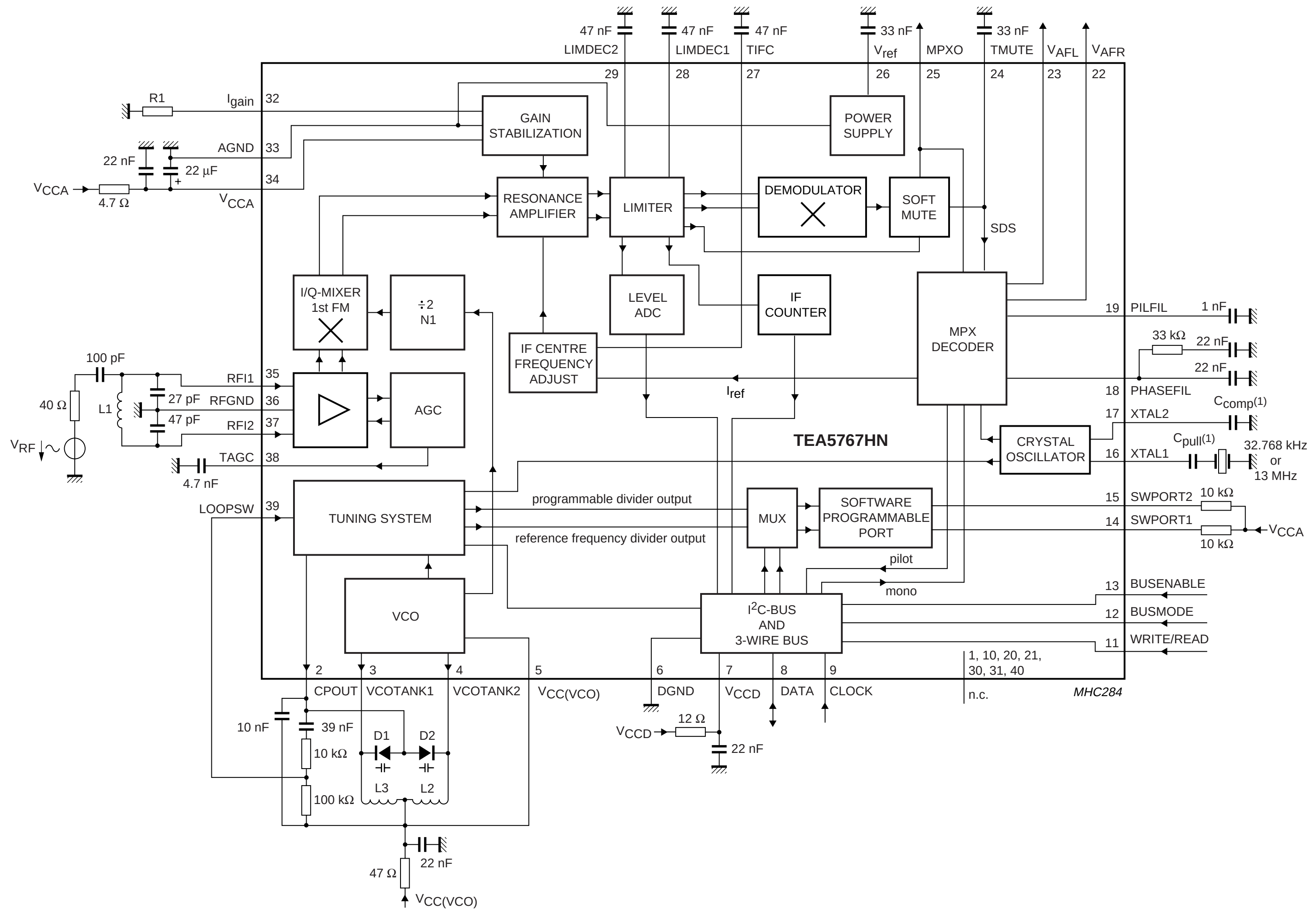
PIN	SYMBOL	EQUIVALENT CIRCUIT
25	MPXO	
26	V_{ref}	
27	TIFC	
28	LIMDEC1	
29	LIMDEC2	
30	n.c.	
31	n.c.	

PIN	SYMBOL	EQUIVALENT CIRCUIT
32	I_{gain}	
33	AGND	
34	V_{CCA}	
35	RFI1	
36	RFGND	
37	RFI2	
38	TAGC	
39	LOOPSW	
40	n.c.	

14 APPLICATION INFORMATION

Table 28 Component list for Figs 1 and 7

COMPONENT	PARAMETER	VALUE	TOLERANCE	TYPE	MANUFACTURER
R1	resistor with low temperature coefficient	18 kΩ	±1%	RC12G	Philips
D1 and D2	varicap for VCO tuning	–	–	BB202	Philips
L1	RF band filter coil	120 nH	±2%	Q_{min} = 40	
L2 and L3	VCO coil	33 nH	±2%	Q_{min} = 40	
XTAL13	13 MHz crystal	–	–	NX4025GA	
C_{pull}	pulling capacitor for NX4025GA	10 pF	–		
XTAL32.768	32.768 kHz crystal	–	–		

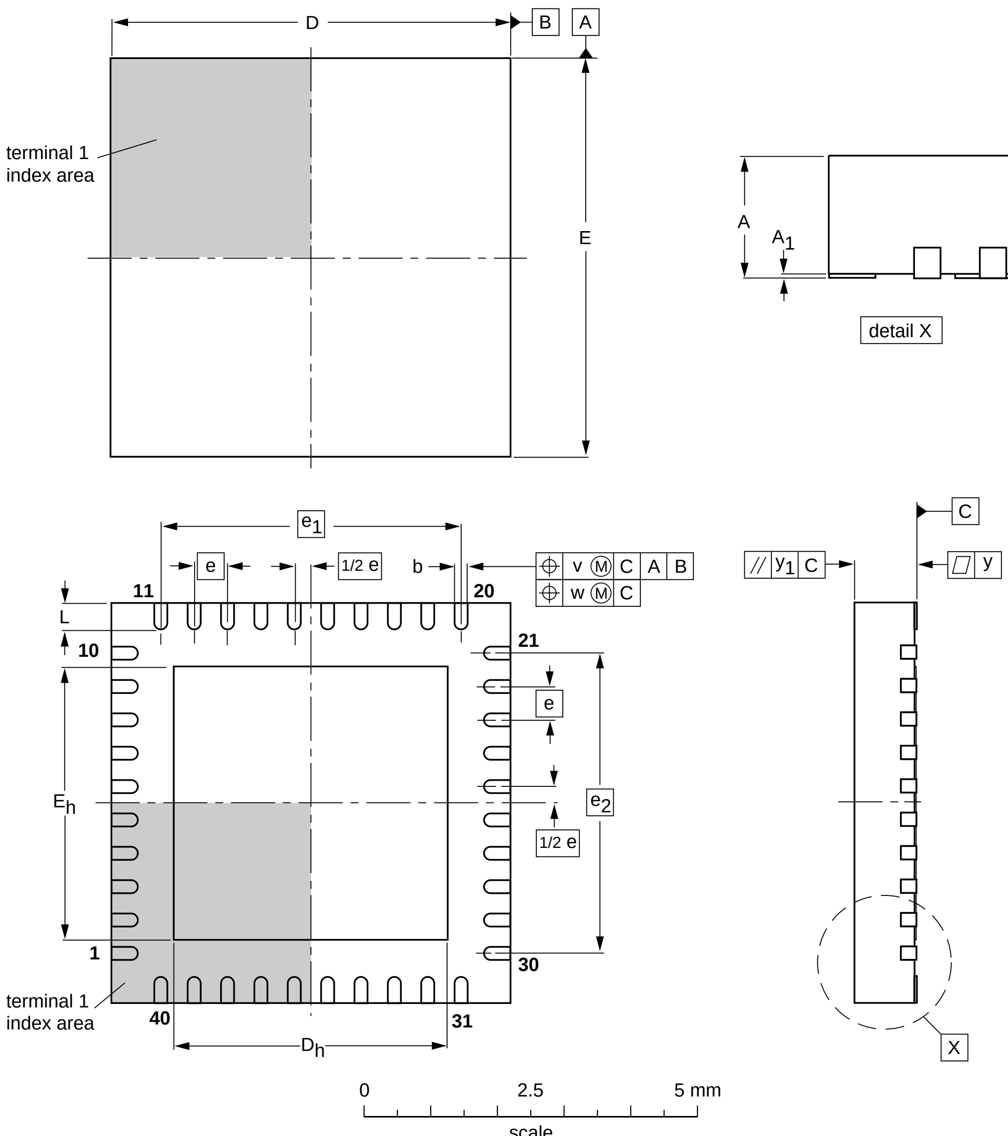


(1) C_{comp} and C_{pull} data depends on crystal specification.

Fig.7 Test circuit.

15 PACKAGE OUTLINE

HVQFN40: plastic thermal enhanced very thin quad flat package; no leads; 40 terminals; body 6 x 6 x 0.85 mm **SOT618-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	6.1 5.9	4.25 3.95	6.1 5.9	4.25 3.95	0.5	4.5	4.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT618-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-22

16 SOLDERING

16.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

16.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 220 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA and SSOP-T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 235 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

16.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

16.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

16.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE[1]	SOLDERING METHOD	
	WAVE	REFLOW[2]
BGA, LBGA, LFBGA, SQFP, SSOP-T[3], TFBGA, VFBGA	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable[4]	suitable
PLCC[5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[5][6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended[7]	suitable
PMFP[8]	not suitable	not suitable

Notes

1. For more detailed information on the BGA packages refer to the *"(LF)BGA Application Note"* (AN01026); order a copy from your Philips Semiconductors sales office.
2. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
3. These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.
4. These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.
5. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
6. Wave soldering is suitable for LQFP, TQFP and QFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
7. Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.
8. Hot bar or manual soldering is suitable for PMFP packages.

17 DATA SHEET STATUS

LEVEL	DATA SHEET STATUS[1]	PRODUCT STATUS[2][3]	DEFINITION
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