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RENESAS

User's Manual

Multimedia Processor for Mobile Applications

Camera Interface

EMMA Mobile1

Document No. S19285EJ2V0UM00 (2nd edition)
Date Published April 2009

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M8E 02. 11-1

PREFACE

Readers

This manual is intended for hardware/software application system designers who wish to understand and use the camera interface functions of EMMA Mobile1 (EM1), a multimedia processor for mobile applications.

Purpose

This manual is intended to explain to users the hardware and software functions of the camera interface of EM1, and be used as a reference material for developing hardware and software for systems that use EM1.

Organization

This manual consists of the following chapters.

- Chapter 1 Overview
- Chapter 2 Pin functions
- Chapter 3 Registers
- Chapter 4 Description of functions
- Chapter 5 Usage

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electricity, logic circuits, and microcontrollers.

To understand the functions of the camera interface of EM1 in detail

→ Read this manual according to the **CONTENTS**.

To understand the other functions of EM1

→ Refer to the user's manual of the respective module.

To understand the electrical specifications of EM1

→ Refer to the Data Sheet.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH
Data type:	Word … 32 bits
	Halfword … 16 bits
	Byte … 8 bits

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name		Document No.
MC-10118A Data sheet		S19657E
μPD77630A Data sheet		S19686E
User's manual	Audio/Voice and PWM Interfaces	S19253E
	DDR SDRAM Interface	S19254E
	DMA Controller	S19255E
	I^2C Interface	S19256E
	ITU-R BT.656 Interface	S19257E
	LCD Controller	S19258E
	MICROWIRE	S19259E
	NAND Flash Interface	S19260E
	SPI	S19261E
	UART Interface	S19262E
	Image Composer	S19263E
	Image Processor Unit	S19264E
	System Control/General-Purpose I/O Interface	S19265E
	Timer	S19266E
	Terrestrial Digital TV Interface	S19267E
	Camera Interface	This manual
	USB Interface	S19359E
	SD Memory Card Interface	S19361E
	PDMA	S19373E
	One Chip (MC-10118A)	S19598E
	One Chip (μPD77630A)	S19687E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

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LIST OF FIGURES

LIST OF TABLES

CHAPTER 1 OVERVIEW

This manual describes the camera interface (CAM) for EM1.

1.1 Function Overview

CAM captures YUV422 image data from an external camera module, reduces the image to any size (down to 1/16), and transfers it to an external memory.

1.2 Features

○ Camera interface signal
- Data bus (CAM_YUV[7:0])
- Vertical synchronization (CAM_VS)
- Horizontal synchronization (CAM_HS)
- Pixel clock (CAM_CLKI)

○ Synchronization signal encoding
- Vertical/horizontal synchronization signal sampling
- Enable signal sampling
- ITU-R BT.656 encoding

○ ITU-R BT.656 input
- The following three modes are available.
  - Store the first field to buffer A, and the second field to buffer B.
  - Store only the first field to buffer A.
  - Store only the second field to buffer A.

○ Data format
- Input: YUV422
- Output: Selected from YUV422 or YUV420 format
  (YUV Semi-Planar, YUV Interleave and YUV Planar modes are selectable in YUV422 mode.
  YUV Semi-Planar and YUV Planar modes are selectable in YUV420 mode.)

○ Maximum image size
- 4,088 pixels (horizontal) × 4,092 pixels (vertical)

○ Data sampling

Data can be sampled at the following timing for the pixel clock:
- Rising edge
- Falling edge
- Both edges

○ Level adjustment

The gain and offset of the captured external camera images can be adjusted. Values can be specified separately for Y, U and V.

○ Reduction
- Nearest-neighbor sampling
- Reduction range of 1 to 1/16 (can be set to any size)

○ Frame-skipped transfer
  - No skipping: Every frame is transferred.
  - 1/2 skipping: One out of two frames is transferred.
  - 1/3 skipping: One out of three frames is transferred.
  - 1/4 skipping: One out of four frames is transferred.

○ Horizontal and vertical flipping

  Data can be individually flipped horizontally and/or vertically and transferred to memory.

○ Double buffer transfer

  The transfer destination frame is switched automatically for each transfer frame.

○ Buffer memory

  Two 32-bit × 256-word buffer memories

○ Compliant with AMBA™ system bus architecture (Rev. 2.0)

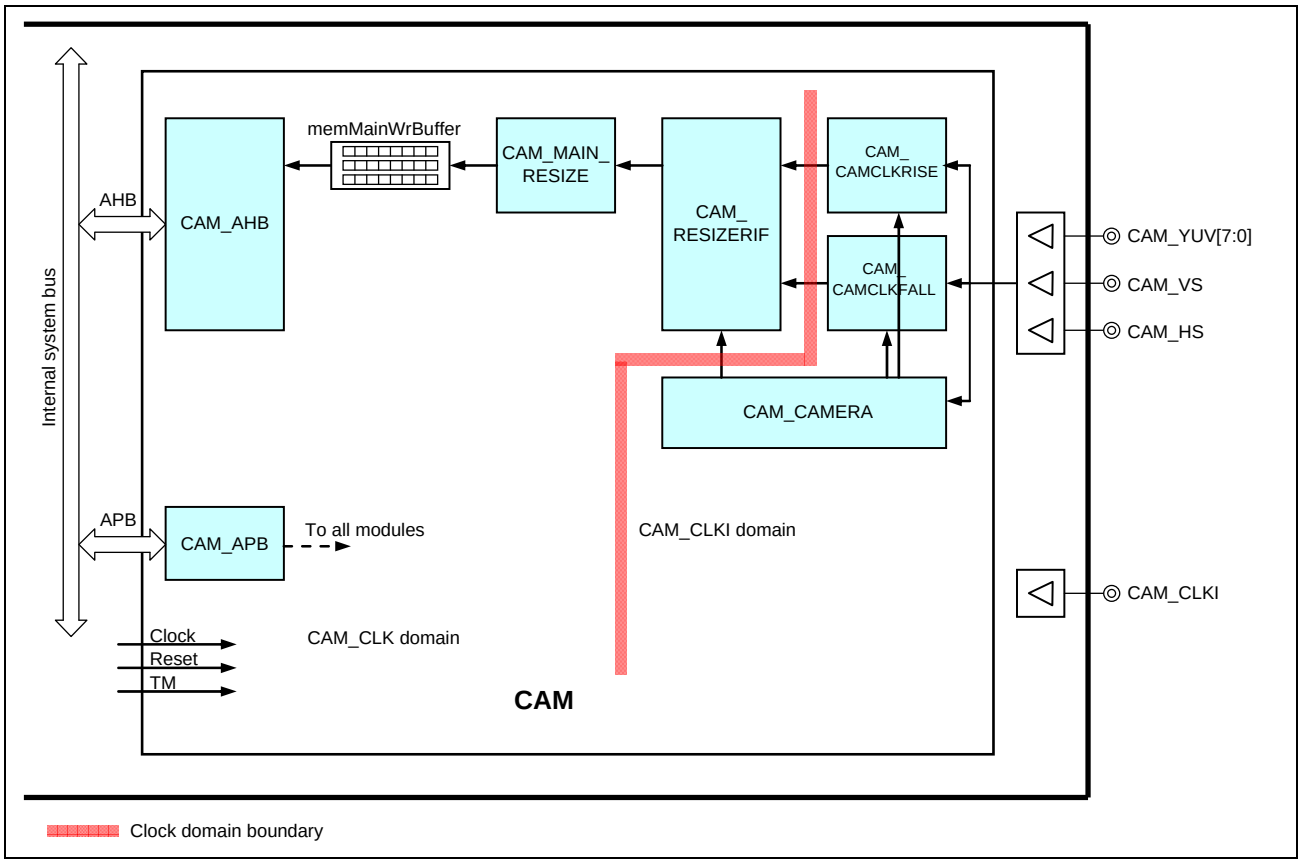
○ Simple QoS
  - Controls the priority of the AXI (AHB) bus modules based on the vacant space in the data buffer.
  - The threshold of the vacant space in the data buffer can be specified by using a register.
  - CAM outputs a priority signal to the control side.

○ Outputting of amount of valid data in FIFO (data buffer)
  - The amount of valid data in the data buffer is output.

○ Safe reset
  - A reset is asserted only when the AHB bus is in the idle state.

1.3 Function Block Diagram

Figure 1-1. Block Diagram



The CAM module and the clock domains are outlined below.

(1) CAM_AHB (CAM_CLK domain)

This is an interface compliant with the AMBA AHB Specification. This interface functions as a bus master and writes the image to a frame memory via the system bus.

(2) CAM_APB (CAM_CLK domain)

This is an interface compliant with the AMBA APB Specification. Registers are allocated to this block and are used to control CAM through setup via the system bus.

(3) CAM_MAIN_RESIZE (CAM_CLK domain)

This block resizes the images in a range of 1/1 to 1/16 by using nearest-neighbor sampling.

(4) CAM_RESIZERIF (CAM_CLK domain)

This block adjusts the gain and offset values and synchronizes an asynchronous signal sent from the CAM_CLKI domain.

(5) memMainWrBuffer (CAM_CLK domain)

This is a 32-bit × 256-word write buffer.

(6) CAM_CAMERA (CAM_CLKI domain)

This block performs frame skipping and selects the sampling edge of CAM_CLKI. In addition, this block generates a signal for handshaking with the CAM_CLK domain.

(7) CAM_CAMCLKRISE (CAM_CLKI domain)

This block samples the rising edges of CAM_YUV, CAM_VS, and CAM_HS.

(8) CAM_CAMCLKFALL (CAM_CLKI domain)

This block samples the falling edges of CAM_YUV, CAM_VS, and CAM_HS.

CHAPTER 2 PIN FUNCTIONS

2.1 Camera Interface Pins

Pin Name	I/O	After Reset	Function	Alternate Pin
CAM_YUV0	Input	–	Camera YUV data	NTS_DATA0 GIO_P75 SP1_SO
CAM_YUV1	Input	–	Camera YUV data	NTS_DATA1 GIO_P76 SP1_CS0
CAM_YUV2	Input	–	Camera YUV data	NTS_DATA2 GIO_P77 SP1_CS1
CAM_YUV3	Input	–	Camera YUV data	NTS_DATA3 GIO_P78 SP1_CS2
CAM_YUV4	Input	–	Camera YUV data	NTS_DATA4 GIO_P79 SP1_CS3
CAM_YUV5	Input	–	Camera YUV data	SD1_CMD
CAM_YUV6	Input	–	Camera YUV data	SD1_DATA0
CAM_YUV7	Input	–	Camera YUV data	SD1_DATA1
CAM_VS	Input	–	Camera vertical synchronization signal	SD1_DATA2
CAM_HS	Input	–	Camera horizontal synchronization signal	SD1_DATA3
CAM_CLKI	Input	–	Camera clock	SD1_CLI GIO_P92
CAM_SCLK	Output	0	Camera clock	GIO_P5 NAND_RB2

CHAPTER 3 REGISTERS

3.1 Registers

Do not access reserved registers. An undefined value is returned for a read access.

Do not write any value other than 0 to reserved bits in each register.

Base address: 400B_0000H (1/2)

Address	Register Name	Function	R/W	Reset
0000H	CA_STATUS	INT status register	R	0000_0000H
0004H	CA_RAWSTATUS	INT raw status register	R	0000_0000H
0008H	CA_ENSET	INT enable set register	R/W	0000_0000H
000CH	CA_ENCLR	INT enable clear register	W	0000_0000H
0010H	CA_FFCLR	INT source clear register	W	0000_0000H
0014H	CA_ERRORADR	Error address register	R/W	0000_0000H
0018H to 001CH	–	Reserved	–	–
0020H	CA_CSR	Camera control register	R/W	0000_0000H
0024H to 002CH	–	Reserved	–	–
0030H	CA_X1R	Transfer start X coordinate register	R/W	0000_0000H
0034H	CA_X2R	Transfer end X coordinate register	R/W	0000_0000H
0038H	CA_Y1R	Transfer start Y coordinate register	R/W	0000_0000H
003CH	CA_Y2R	Transfer end Y coordinate register	R/W	0000_0000H
0040H	CA_BNZR	Luminance signal offset register	R/W	0000_0000H
0044H	CA_BNGR	Luminance signal gain register	R/W	0000_0080H
0048H	CA_CBZR	U color difference signal offset register	R/W	0000_0000H
004CH	CA_CBGR	U color difference signal gain register	R/W	0000_0080H
0050H	CA_CRZR	V color difference signal offset register	R/W	0000_0000H
0054H	CA_CRGR	V color difference signal gain register	R/W	0000_0080H
0058H to 007CH	–	Reserved	–	–
0080H	CA_DMACNT	Transfer control register	R/W	0000_0000H
0084H	CA_FRAME	Transfer frame register	R/W	0000_0005H
0088H	CA_DMAREQ	Transfer request register	R/W	0000_0000H
008CH	CA_DMASTOP	Transfer request cancellation register	W	0000_0000H
0090H to 00FCH	–	Reserved	–	–
0100H	CA_LINESIZE_MAIN	Address addition value register (main frame)	R/W	0000_0000H
0104H	CA_XRATIO_MAIN	Horizontal reduction ratio register (main frame)	R/W	0000_0000H
0108H	CA_YRATIO_MAIN	Vertical reduction ratio register (main frame)	R/W	0000_0000H
010CH	CA_DMAX_MAIN	Horizontal transfer size register (main frame)	R/W	0000_0000H
0110H	CA_DMAY_MAIN	Vertical transfer size register (main frame)	R/W	0000_0000H

(2/2)

Address	Register Name	Function	R/W	Reset
0114H	CA_YPLANE_A	Y plane transfer address register (A frame)	R/W	0000_0000H
0118H	CA_UVPLANE_A	UV plane transfer address register (A frame)	R/W	0000_0000H
011CH	CA_YPLANE_B	Y plane transfer address register (B frame)	R/W	0000_0000H
0120H	CA_UVPLANE_B	UV plane transfer address register (B frame)	R/W	0000_0000H
0124H to 0228H	–	Reserved	–	–
022CH	CA_MODULECONT	Module control register	R/W	0000_0000H
0230H	CA_UPDATE	Update register	R/W	0000_0000H
0234H	CA_MIRROR	Horizontal/vertical flip control register	R/W	0000_0000H
0238H	CA_OD_BYTELANE	Byte lane control register (dedicated to YUV 422 Interleave)	R/W	0000_00E4H
023CH	–	Reserved	–	–
0240H	CA_X3R	Transfer end X coordinate register (dedicated to enable signal sampling mode)	R/W	0000_0000H
0244H	CA_VPLANE_A	V plane transfer address register (A frame)	R/W	0000_0000H
0248H	CA_VPLANE_B	V plane transfer address register (B frame)	R/W	0000_0000H
024CH to 0250H	–	Reserved	–	–
0254H	CA_OD_BYTELANE2	Byte lane control register 2 (for video-system macros)	R/W	0000_E4E4H
0258H	CA_QOS	Simple QoS setting register	R/W	0000_0000H
025CH to FFFFH	–	Reserved	–	–

3.2 Register Functions

3.2.1 Interrupt registers

CAM uses four interrupt sources. Control of interrupts is assigned to each bit of the control register. For details, see **Table 3-1**.

Table 3-1. Interrupt Sources

Interrupt Name	Source	Bit Assignment
Main frame overrun interrupt	This interrupt is issued when the internal buffer overruns during main frame transfer.	3
Main frame transfer completion interrupt	This interrupt is issued upon completion of transfer of one-frame data to the main frame.	2
Transfer error interrupt	This interrupt is issued if an ERROR, RETRY, or SPLIT response is received during an AHB transfer. When a transfer error occurs, the transaction during transfer is lost but the subsequent transfer is continued.	1
Vertical synchronization interrupt	This interrupt is issued at an edge of CAM_VS frame starting (VS_POL setting). If a CAM_VS signal is the positive logic, an interrupt is issued at a rising edge of the CAM_VS. If a CAM_VS signal is the negative logic, an interrupt is issued at a falling edge of the CAM_VS.	0

Remark If an interrupt source is set and cleared at the same time, setting takes precedence.

(1) INT status register

This register (CA_STATUS: 400B_0000H) indicates the status of the interrupt sources unmasked in the CA_ENSET register.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				MAINOR	MAINTC	DMAERR	CAM_VS

Name	R/W	Bit	After Reset	Function
Reserved	R	31:4	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
MAINOR	R	3	0H	Indicates the status of the main frame overrun interrupt source. 0: No interrupt source 1: Interrupt source has occurred
MAINTC	R	2	0H	Indicates the status of the main frame transfer completion interrupt source. 0: No interrupt source 1: Interrupt source has occurred
DMAERR	R	1	0H	Indicates the status of the transfer error interrupt source. 0: No interrupt source 1: Interrupt source has occurred
CAM_VS	R	0	0H	Indicates the status of the vertical synchronization interrupt source. 0: No interrupt source 1: Interrupt source has occurred

(2) INT raw status register

This register (CA_RAWSTATUS: 400B_0004H) indicates the status of the interrupt sources, regardless of the CA_ENSET register settings.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				MAINORRAW	MAINTCRAW	DMAERRRAW	CAM_VSRAW

Name	R/W	Bit	After Reset	Function
Reserved	R	31:4	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
MAINORRAW	R	3	0H	Indicates the raw status of the main frame overrun interrupt source. 0: No interrupt source 1: Interrupt source has occurred
MAINTCRAW	R	2	0H	Indicates the raw status of the main frame transfer completion interrupt source. 0: No interrupt source 1: Interrupt source has occurred
DMAERRRAW	R	1	0H	Indicates the raw status of the transfer error interrupt source. 0: No interrupt source 1: Interrupt source has occurred
CAM_VSRAW	R	0	0H	Indicates the raw status of the vertical synchronization interrupt source. 0: No interrupt source 1: Interrupt source has occurred

(3) INT enable set register

This register (CA_ENSET: 400B_0008H) cancels masking of interrupts.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

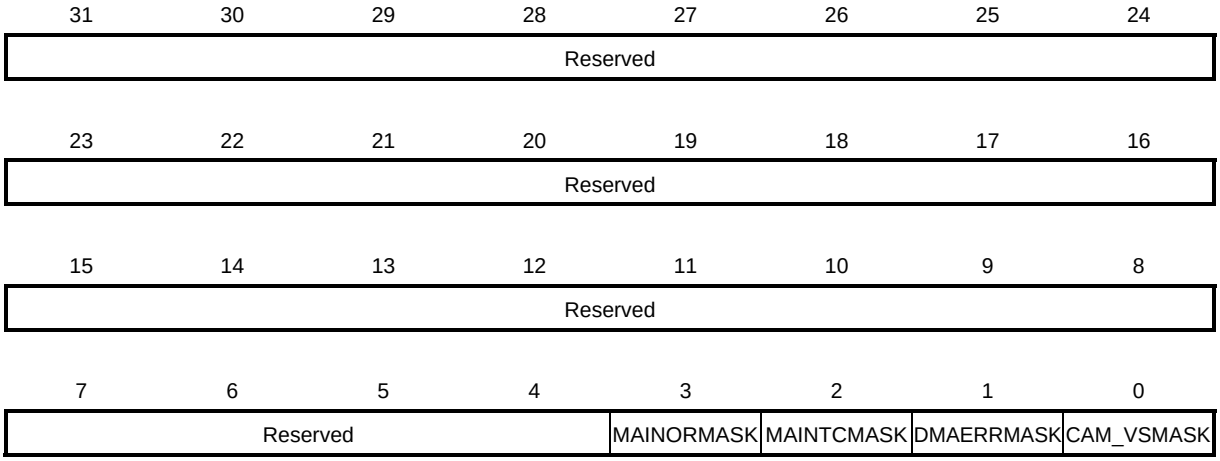
7	6	5	4	3	2	1	0
Reserved				MAINOR_EN	MAINTC_EN	DMAERR_EN	CAM_VS_EN

Name	R/W	Bit	After Reset	Function
Reserved	R	31:4	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
MAINOR_EN	R	3	0H	Indicates whether issuance of main frame overrun interrupt requests is enabled. 0: Not enabled (Masked) 1: Enabled (Unmasked)
	W	3	0H	Enables issuance of main frame overrun interrupt requests. 0: Ignored 1: Cancels interrupt masking.
MAINTC_EN	R	2	0H	Indicates whether issuance of main frame transfer completion interrupt requests is enabled. 0: Not enabled (Masked) 1: Enabled (Unmasked)
	W	2	0H	Enables issuance of main frame transfer completion interrupt requests. 0: Ignored 1: Cancels interrupt masking.
DMAERR_EN	R	1	0H	Indicates whether issuance of DMA transfer error interrupt requests is enabled. 0: Not enabled (Masked) 1: Enabled (Unmasked)
	W	1	0H	Enables issuance of DMA transfer error interrupt requests. 0: Ignored 1: Cancels interrupt masking.
CAM_VS_EN	R	0	0H	Indicates whether issuance of vertical synchronization interrupt requests is enabled. 0: Not enabled (Masked) 1: Enabled (Unmasked)
	W	0	0H	Enables issuance of vertical synchronization interrupt requests. 0: Ignored 1: Cancels interrupt masking.

Caution When setting the CAM_VS_EN bit, wait for at least 16 CAM_CLKI cycles after the reset state of the CAM_CLKI domain is released.

(4) INT enable clear register

This register (CA_ENCLR: 400B_000CH) masks issuance of interrupt requests.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:4	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
MAINORMASK	W	3	0H	Disables issuance of main frame overrun interrupt requests. 0: Ignored 1: Masks the interrupt.
MAINTCMASK	W	2	0H	Disables issuance of main frame transfer completion interrupt requests. 0: Ignored 1: Masks the interrupt.
DMAERRMASK	W	1	0H	Disables issuance of transfer error interrupt requests. 0: Ignored 1: Masks the interrupt.
CAM_VSMASK	W	0	0H	Disables issuance of vertical synchronization interrupt requests. 0: Ignored 1: Masks the interrupt.

(5) INT source clear register

This register (CA_FFCLR: 400B_0010H) clears interrupt sources. The bit is cleared when the corresponding source is cleared.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

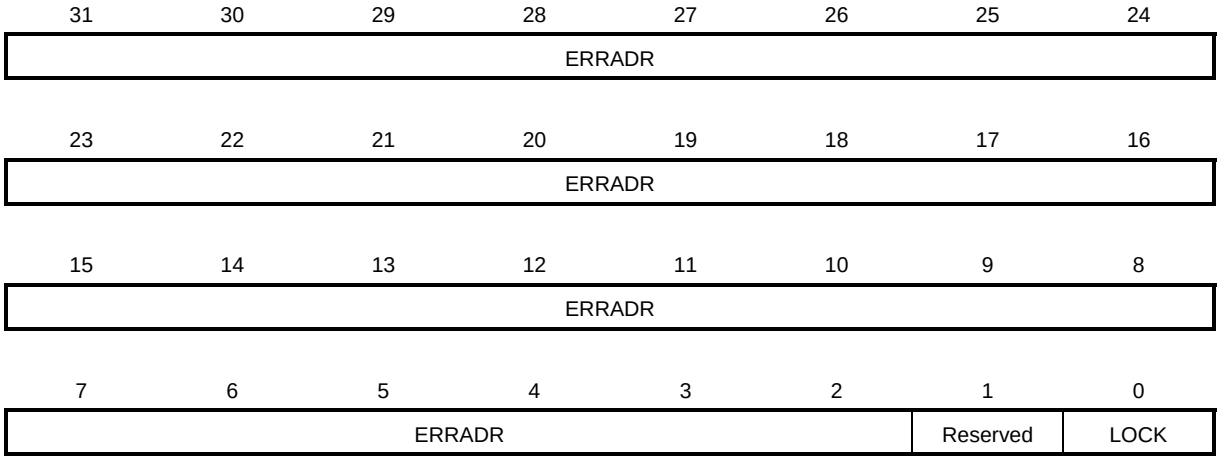
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				MAINORCLR	MAINTCCLR	DMAERRCLR	CAM_VSCLR

Name	R/W	Bit	After Reset	Function
Reserved	R	31:4	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
MAINORCLR	W	3	0H	Clears the main frame overrun interrupt source. 0: Ignored 1: Clears the interrupt source.
MAINTCCLR	W	2	0H	Clears the main frame transfer completion interrupt source. 0: Ignored 1: Clears the interrupt source.
DMAERRCLR	W	1	0H	Clears the transfer error interrupt source. 0: Ignored 1: Clears the interrupt source.
CAM_VSCLR	W	0	0H	Clears the vertical synchronization interrupt source. 0: Ignored 1: Clears the interrupt source.

(6) Error address register

This register (CA_ERRORADR: 400B_0014H) retains the current HADDR status when an AHB bus response ERROR, RETRY, or SPLIT is received during DMA transfer.



Name	R/W	Bit	After Reset	Function
ERRADR	R	31:2	0H	Stores HADDR upon occurrence of a response other than OKAY.
Reserved	R	1	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
LOCK	R/W	0	0H	Error status 0: Waiting to store the address where an error response occurred. 1: An error response occurred and the address was stored.

Caution If an error response occurs when the LOCK bit is 0, the current HADDR status is stored in the ERRADR bit and the LOCK bit is set to 1. To acquire the error status again, set the LOCK bit to 0. Writing 1 to the LOCK bit does not affect the setting.

3.2.2 Control registers

(1) Camera control register

This 16-bit register (CA_CSR: 400B_0020H) controls the CAM module. To specify the CAM_VS/CAM_HS signal sampling mode, set the SYNCTYPE and SYNCMODE bits to 0H.

Change the values only when DMA transfer is not being performed (transfer request register = 0H).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
656MODE		PIXEL_YUV	SYNCTYPE	PIXELMODE	DATA_OD	DATA_ID	LD_TMG

7	6	5	4	3	2	1	0
VS_DET	HS_DET	LIMITSEL	SYNCMODE	CLK_EDGE	DATA_DET	VS_POL	HS_POL

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31:16	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
656MODE	R/W	15:14	0H	Specifies the field to be stored in the ITU-R BT.656 mode. (These bits are valid only when the ITU-R BT.656 mode is set by using the SYNCMODE bit.) 00: Stores both the first and second fields to a buffer, starting with the first field. 01: Stores both the first and second fields to a buffer, starting with the second field. 10: Stores only the first field to a buffer. 11: Stores only the second field to a buffer.
PIXEL_YUV	R/W	13	0H	Specifies the format of the data to be transferred to memory. 0: Depends on the PIXELMODE bit setting. 1: YUV420/YUV422 Planar mode (Ignores the PIXELMODE bit setting.)
SYNCTYPE	R/W	12	0H	Specifies the data sampling mode. (This bit is valid only when the CAM_VS/CAM_HS signal sampling mode is set by using the SYNCMODE bit.) 0: CAM_VS/CAM_HS signal sampling mode 1: Enable signal sampling mode
PIXELMODE	R/W	11	0H	Specifies the format of the data to be transferred to memory. (This bit is valid only when the CAM_VS/CAM_HS signal sampling mode is set by using the SYNCMODE bit.) 0: YUV 420/422 Semi-Planar mode 1: YUV422 Interleave mode

(2/2)

Name	R/W	Bit	After Reset	Function
DATA_OD	R/W	10	0H	Specifies the endian of the data to be transferred to memory. (This bit is valid only when the YUV 420/422 Semi-Planar mode is set by using the PIXELMODE bit.) Bit 32 Bit 0 0: Y plane | Y2 | Y3 | Y0 | Y1 | UV plane | U1 | V1 | U0 | V0 | 1: Y plane | Y3 | Y2 | Y1 | Y0 | UV plane | V1 | U1 | V0 | U0 |
DATA_ID	R/W	9	0H	Specifies the sequence of data input via the CAM YUV signal. 0: U → Y → V → Y 1: Y → U → Y → V
LD_TMG	R/W	8	0H	Selects the register value enable timing (see **Figure 3-1**). 0: At the beginning of CAM_VS (rising edge of CAM_VS if CAM_VS is positive) 1: At the end of CAM_VS (falling edge of CAM_VS if CAM_VS is positive)
VS_DET	R/W	7	0H	Selects the CAM_VS detection clock edge. 0: Rising edge of CAM_CLKI 1: Falling edge of CAM_CLKI
HS_DET	R/W	6	0H	Selects the CAM_HS detection clock edge. 0: Rising edge of CAM_CLKI 1: Falling edge of CAM_CLKI
LIMITSEL	R/W	5	0H	Selects the limit value of the YUV output data. 0: Conforms to ITU-R BT.656 (Y: 16 to 235, U and V: 16 to 240) 1: All 8 bits are valid (Y, U, and V: 0 to 255)
SYNCMODE	R/W	4	0H	Selects the synchronization mode. 0: CAM_VS/CAM_HS signal sampling mode 1: ITU-R BT.656 mode
CLK_EDGE	R/W	3	0H	Selects a clock edge. 0: Single-edge transfer 1: Both-edge transfer For single-edge transfer, the valid edge of CAM_CLKI is selected by using the DATA_DET, HS_DET, and VS_DET bits. For both-edge transfer, CAM_VS and CAM_HS are detected at the rising edge.
DATA_DET	R/W	2	0H	Selects the CAM YUV detection clock edge. 0: Rising edge of CAM_CLKI 1: Falling edge of CAM_CLKI
VS_POL	R/W	1	0H	Selects the polarity of CAM_VS. 0: Positive logic 1: Negative logic The result varies depending on the specified data sampling mode (SYNCTYPE bit). See **Figure 3-2** for details.
HS_POL	R/W	0	0H	Selects the polarity of CAM_HS. 0: Positive logic 1: Negative logic The result varies depending on the specified data sampling mode (SYNCTYPE bit). See **Figure 3-2** for details.

Caution
- **For the SYNCTYPE and SYNCMODE bits, and the modes, see Table 3-2 Relationship Between SYNCTYPE and SYNCMODE Bits and Sampling Modes.**
- **Be sure to set up this register while the CAM_CLKI domain is in the reset state. The operation will not be guaranteed if the values of this register are changed while DMA transfer is being requested or while CAM is operating.**
- **In ITU-R BT.656 mode (SYNCMODE = 1, SYNCTYPE = 0), match the polarity of VS_DET and HS_DET with that of DATA_DET.**

Table 3-2. Relationship Between SYNCTYPE and SYNCMODE Bits and Sampling Modes

Sampling Mode	SYNCTYPE Bit	SYNCMODE Bit
CAM_VS, CAM_HS signal sampling mode	0	0
ITU-R BT.656 mode	0	1
Enable signal sampling mode	1	0

Table 3-3. Relationship Between Sampling Modes and Valid Bits

Sampling Mode	VS_POL	HS_POL	LD_TMG Bit
CAM_VS, CAM_HS signal sampling mode	Valid	Valid	Valid
ITU-R BT.656 mode	Valid	Valid	Valid
Enable signal sampling mode	Valid	Valid	Not valid

Bits other than VS_POL, HS_POL and LD_TMG are valid in all sampling modes.

Figure 3-1. Relationship Between LD_TMG Bit Value and Register Value Enable Timing

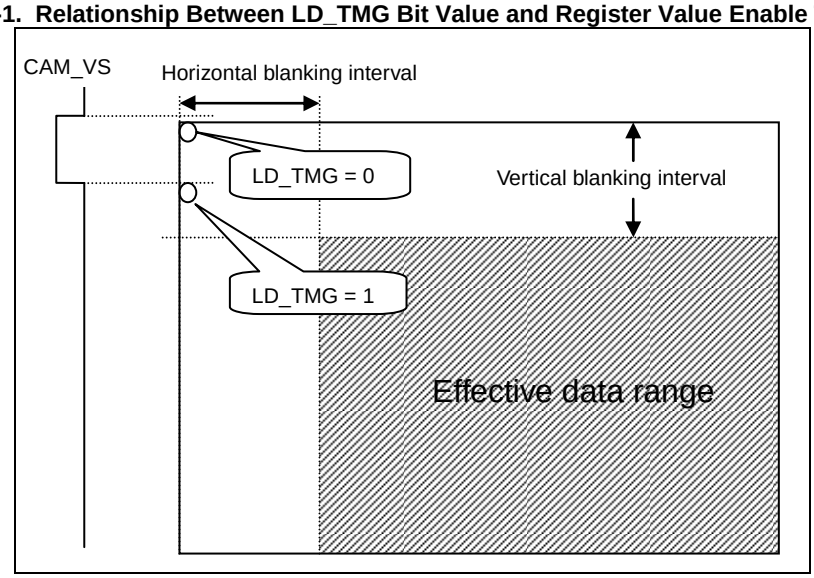
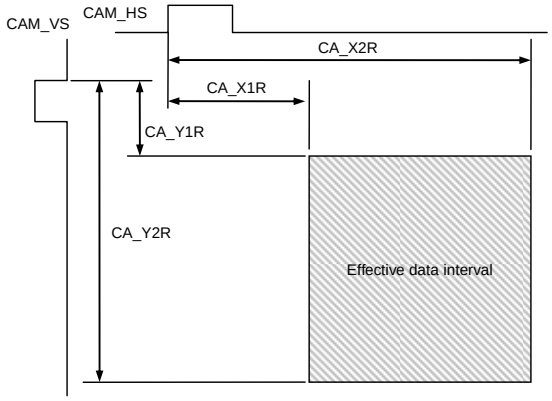


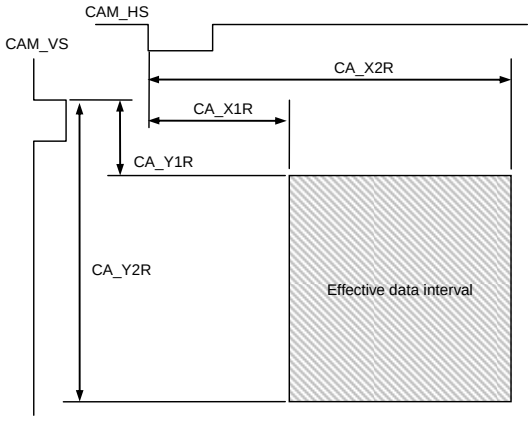
Figure 3-2. Sampling Modes and Settings of VS_POL and HS_POL

CAM_VS/CAM_HS signal sampling mode (SYNCTYPE = 0)

When VS_POL = 0 and HS_POL = 0:
CA_Y1R, CA_Y2R, CA_X1R and CA_X2R are specified based on the rising edges of CAM_VS and CAM_HS.

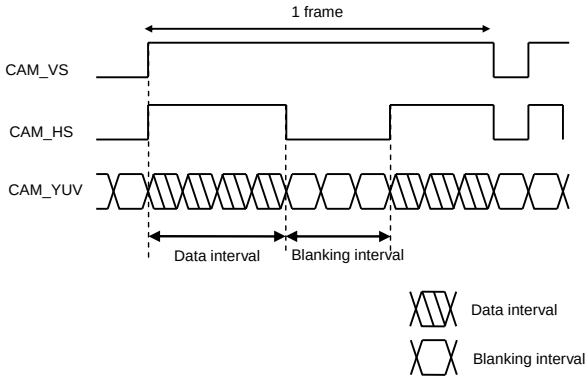


When VS_POL = 1 and HS_POL = 1:
CA_Y1R, CA_Y2R, CA_X1R and CA_X2R are specified based on the falling edges of CAM_VS and CAM_HS.

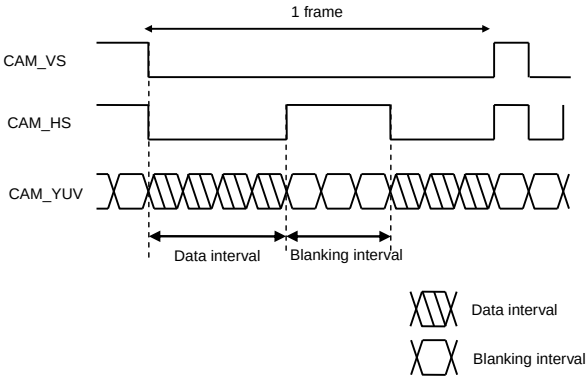


Enable signal sampling mode (SYNCTYPE = 1)

When VS_POL = 0 and HS_POL = 0:
The interval while CAM_VS = 1 and CAM_HS = 1 is regarded as a data interval.
CA_Y1R, CA_Y2R, CA_X1R and CA_X2R are specified based on the rising edges of CAM_VS and CAM_HS.



When VS_POL = 1 and HS_POL = 1:
The interval while CAM_VS = 0 and CAM_HS = 0 is regarded as a data interval.
CA_Y1R, CA_Y2R, CA_X1R and CA_X2R are specified based on the falling edge of CAM_VS and CAM_HS



(2) Byte lane control register

This register (CA_OD_BYTELANE: 400B_0238H) controls which component is to be output to the byte lane when data is stored in memory. This register can be set only in the YUV422 Interleave mode.

Change the value of this register when DMA transfer is not being performed (transfer request register = 0H).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
YUV_OD_BYTELANE							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:8	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
YUV_OD_BYTELANE	R/W	7:0	E4H	Specifies the byte lane of the data to be transferred to memory (see **Figure 3-3**). (This bit is valid only when the YUV422 Interleave mode is set by using the camera control register (CA_CSR).) Selects the component to be output to the byte lane when data is stored in memory. Interleave 00: Y0 01: Y1 10: U0 11: V0

Bit Corresponding to YUV_OD_BYTELANE	Byte Lane Corresponding to Output Data Component Selection
7:6	31:24
5:4	23:16
3:2	15:8
1:0	7:0

(3) Byte lane control register 2

This register (CA_OD_BYTELANE2: 400B_0254H) controls which component is to be output to the byte lane when data is stored in memory. The settings of this register apply to all output modes.

Change the value of this register when DMA transfer is not being performed (transfer request register = 0H).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Y_BYTELANE							

7	6	5	4	3	2	1	0
UV_BYTELANE							

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31:16	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
Y_BYTELANE	R/W	15:8	E4H	Specifies the byte lane of the data to be transferred to the memory. Selects the component to be output to the byte lane when data is stored in memory. 1) YUV 422 Interleave 00: Y0 01: Y1 10: U0 11: V0

Bit Corresponding to Y_BYTELANE	Byte Lane Corresponding to Output Data Component Selection
7:6	31:24
5:4	23:16
3:2	15:8
1:0	7:0

2) YUV 420/422 Semi-Planar and YUV 420/422 Planar

00: Y0 01: Y1 10: Y2 11: Y3

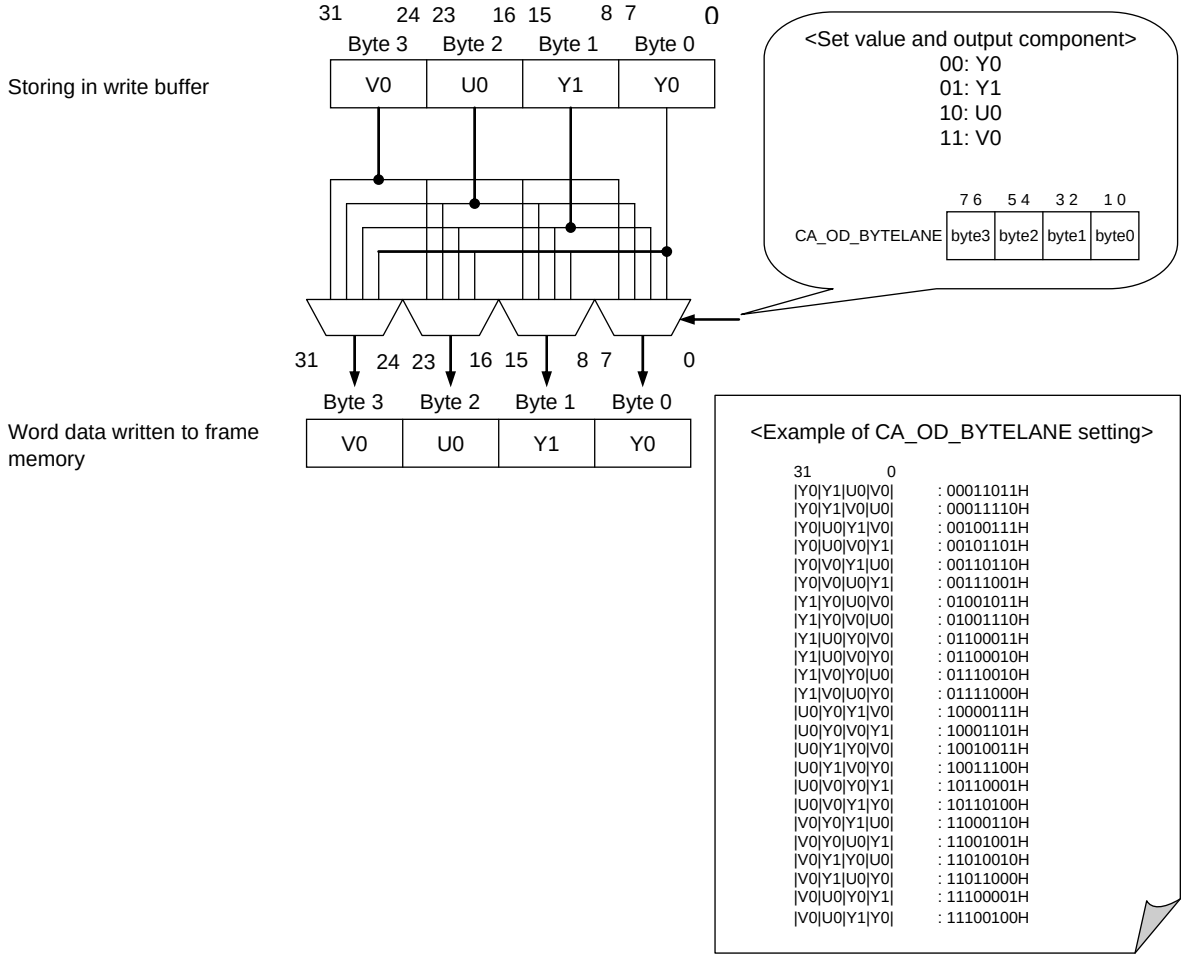
Bit Corresponding to Y_BYTELANE	Byte Lane Corresponding to Output Data Component Selection
7:6	31:24
5:4	23:16
3:2	15:8
1:0	7:0

(2/2)

<table>
<tr><th>Name</th><th>R/W</th><th>Bit</th><th>After Reset</th><th>Function</th></tr>
<tr><td>UV_BYTELANE</td><td>R/W</td><td>7:0</td><td>E4H</td><td>Specifies the byte lane of the data to be transferred to the memory.
(This bit is valid only when the YUV420/YUV422 Semi-Planar or YUV420/YUV422 Planar mode is set by using the YUVFMT bit.)
Selects the component to be output to the byte lane when data is stored in memory.
1) YUV 420/422 Semi-Planar
00: U0 01: V0 10: U1 11: V1
<table>
<tr><th>Bit Corresponding to UV_ BYTELANE</th><th>Byte Lane Corresponding to Output Data Component Selection</th></tr>
<tr><td>7:6</td><td>31:24</td></tr>
<tr><td>5:4</td><td>23:16</td></tr>
<tr><td>3:2</td><td>15:8</td></tr>
<tr><td>1:0</td><td>7:0</td></tr>
</table>
2) YUV 420/422 Planar
00: U0/V0 01: U1/V1 10: U2/V2 11: U3/V3
<table>
<tr><th>Bit Corresponding to UV_ BYTELANE</th><th>Byte Lane Corresponding to Output Data Component Selection</th></tr>
<tr><td>7:6</td><td>31:24</td></tr>
<tr><td>5:4</td><td>23:16</td></tr>
<tr><td>3:2</td><td>15:8</td></tr>
<tr><td>1:0</td><td>7:0</td></tr>
</table>
</td></tr>
</table>

Figure 3-3. Relationship Between CA_OD_BYTELANE/CA_OD_BYTELANE2 Value and Output Data

■ Setting example when YUV Interleave is the output data format



■ Setting example when YUV Planar is the output data format

Word data written to frame memory

Y3	Y2	Y1	Y0	Y plane
U3	U2	U1	U0	U plane
V3	V2	V1	V0	V plane

Set value: E4H (default)

Y2	Y3	Y0	Y1	Y plane
U2	U3	U0	U1	U plane
V2	V3	V0	V1	V plane

Set value: B1H

Caution Output format and valid byte lane setting:
The valid setting for a byte lane varies depending on the output format. See the following table.

Table 3-4. Output Formats and Valid Byte Lanes

Output Format	DATA_OD Bit (Endian Setting)	CA_OD_BYTELANE Register	CA_OD_BYTELANE2 Register
YUV 422 Interleave	Not valid	Valid	Valid
YUV 420/422 Semi-Planar	Valid	Not valid	Valid
YUV 420/422 Planar	Not valid	Not valid	Valid

Caution Do not specify the byte lane using multiple registers. Use the default value for registers other than the register being used to specify the byte lane. For example, use the CA_OD_BYTELANE2 register with the default value (E4H) when specifying the byte lane by using the DATA_OD bit of the CA_CSR register.

3.2.3 Effective image range setting registers

These registers are used to specify the effective range of the data to be captured from a camera. The design is such that data specified in the effective range starts with U (blue difference signal) or Y (luminance signal). The YUV422 data format handles one pixel as 2 bytes, so one pixel is captured during one CAM_CLKI cycle when executing both-edge transfer, and one pixel is captured during two CAM_CLKI cycles when executing single-edge transfer. Specify the effective image range according to the mode, based on the minimum setting units (YUV422 interleave mode: 2-pixel units, YUV422 interleave mode: 2-pixel units, and Planar mode: 8-pixel units).

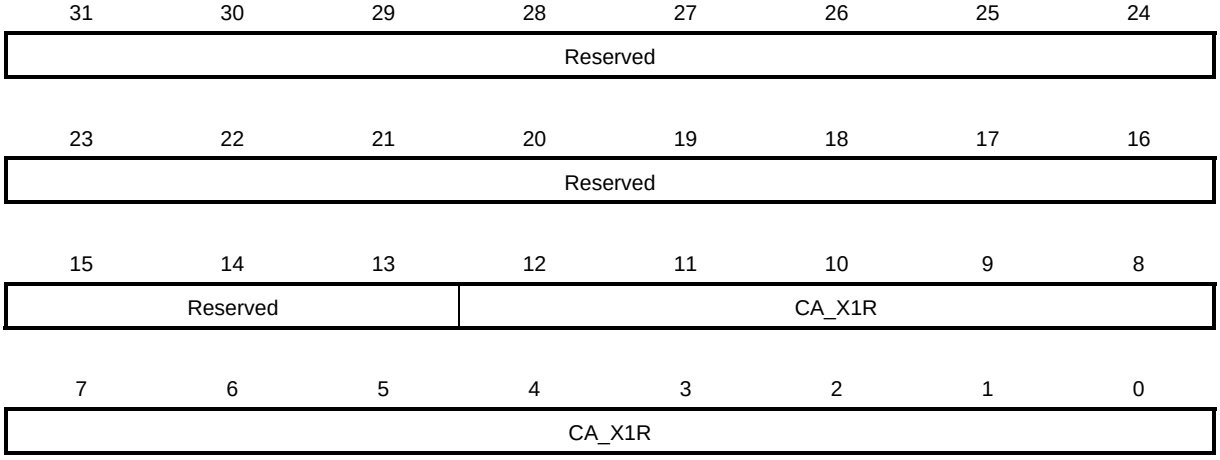
During normal transfer, data in the effective range captured from a camera is transferred to memory. However, note that during resize transfer, the transfer range is specified by the transfer size register and the transfer size is specified by using a different method. For details, see **4.8 Data Transfer Range Specification**.

The effective image range values specified by each register (CA_X1R, CA_X2R, CA_X3R, CA_Y1R, and CA_Y2R) are enabled by the update register. For details, see **3.2.10 Update register**.

(1) Transfer start X coordinate register

This register (CA_X1R: 400B_0030H) specifies the start timing of horizontal transfer according to the number of CAM_CLKI clocks, assuming that the start position is a rising edge of CAM_HS (if the CAM_HS signal has positive logic). Specify the number of clocks until the start timing by using this register.

For details, see **4.8 Data Transfer Range Specification** and **4.9 Restrictions on Transfer Data Range Values**.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:13	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
CA_X1R	R/W	12:0	0H	Transfer start X coordinate register CA_X1R (Camera X1 register) Specifies the number of clocks from CAM_HS to the effective image start position. Specify the number of clocks until cropping starts in the enable signal sampling mode (see **3.2.2 (1) Camera control register (CA_CSR)**).

Caution The minimum setting value varies according to the mode.

- **Vertical/horizontal synchronization signal sampling: 0**
- **Enable signal sampling: 0**

(2) Transfer end X coordinate register

This register (CA_X2R: 400B_0034H) specifies the right edge of the image transfer area. Specify the end position of the area to be made effective, assuming that the end point is a rising edge of CAM_HS (if the CAM_HS signal has positive logic). Specify the number of clocks until the end timing by using this register.

An image in the range specified by the CA_X1R and CA_X2R registers is transferred to memory. For details, see **4.8 Data Transfer Range Specification** and **4.9 Restrictions on Transfer Data Range Values**.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved			CA_X2R				

7	6	5	4	3	2	1	0
CA_X2R							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:13	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
CA_X2R	R/W	12:0	0H	Transfer end X coordinate register CA_X2R (Camera X2 register) Specifies the number of clocks from CAM_HS to the effective image end position. Specify the number of clocks until cropping ends in the enable signal sampling mode (see **3.2.2 (1) Camera control register (CA_CSR)**).

(3) Transfer end X coordinate register (dedicated to enable signal sampling mode)

This register (CA_X3R: 400B_0240H) is valid only in the enable signal sampling mode (SYNCTYPE bit of camera control register = 1). Specify the number of clocks until the effective image end position.

For details, see **4.8 Data Transfer Range Specification** and **4.9 Restrictions on Transfer Data Range Values**. This register is ignored in the CAM_VS/CAM_HS signal sampling mode (SYNCTYPE bit of CA_CSR register = 0).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved			CA_X3R				

7	6	5	4	3	2	1	0
CA_X3R							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:13	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
CA_X3R	R/W	12:0	0H	Transfer end X coordinate register CA_X3R (Camera X3 register) Specifies the number of clocks until the effective image X end position in the enable signal sampling mode.

(4) Transfer start Y coordinate register

This register (CA_Y1R: 400B_0038H) specifies the upper edge of the image transfer area. Specify the image transfer start line according to the number of CAM_HS counts, assuming that the start position is a rising edge of CAM_VS (if the CAM_VS signal is the positive logic).

For details, see **4.8 Data Transfer Range Specification** and **4.9 Restrictions on Transfer Data Range Values**.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved				CA_Y1R			

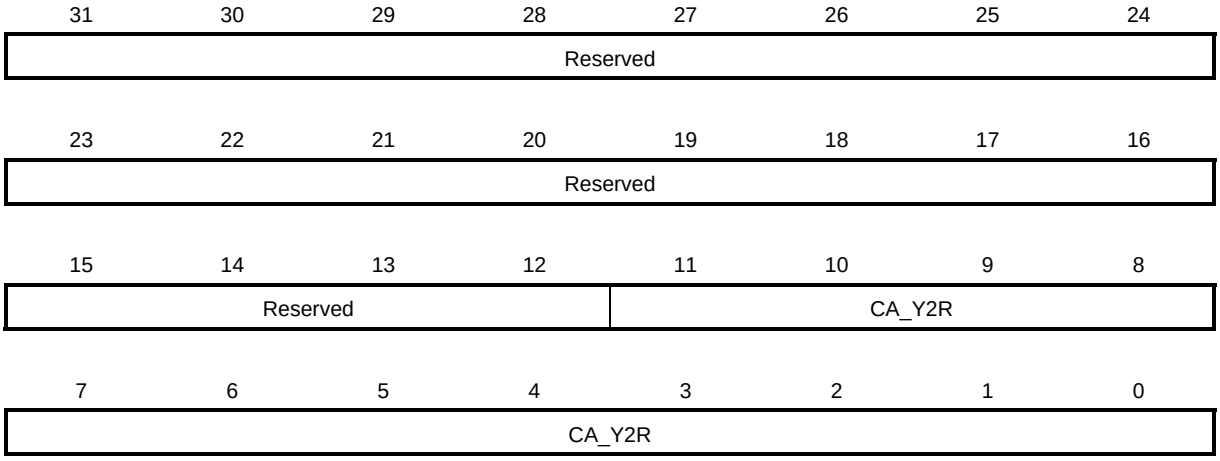
7	6	5	4	3	2	1	0
CA_Y1R							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:12	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
CA_Y1R	R/W	11:0	0H	Transfer start Y coordinate register CA_Y1R (Camera Y1 register) Specifies the effective image start line. Specify the number of lines until cropping starts in the enable signal sampling mode (**3.2.2 (1) Camera control register (CA_CSR)**). If the output format is YUV420, specify the value in 2-line units. For other formats, the value can be specified in line units.

(5) Transfer end Y coordinate register

This register (CA_Y2R: 400B_003CH) specifies the bottom edge of the image transfer area. Specify the image transfer end line according to the number of CAM_HS counts, assuming that the end position is a rising edge of CAM_VS (if the CAM_VS signal has positive logic).

For details, see **4.8 Data Transfer Range Specification** and **4.9 Restrictions on Transfer Data Range Values**.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:12	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
CA_Y2R	R/W	11:0	0H	Transfer end Y coordinate register CA_Y2R (Camera Y2 register) Specifies the effective image end line. Specify the number of lines until cropping ends in the enable signal sampling mode (**3.2.2 (1) Camera control register (CA_CSR)**). If the output format is YUV420, specify the value in 2-line units. For other formats, the value can be specified in line units.

3.2.4 Level adjustment registers

(1) Gain registers (Luminance signal, U color difference signal, V color difference signal)

These registers (CA_BNGR: 400B_0044H, CA_CBGR: 400B_004CH, CA_CRGR: 400B_0054H) are used to adjust the gain for input data. The values can be specified for Y, U, and V, respectively.

These registers store an unsigned 8-bit fixed-point value. The MSB (INT0 bit) is used as the integer part and the 7 bits from the LSB (DEC[6:0]) are used as the decimal part. A gain of 0 to about 1.99 can be specified, in 1/128 units. If not adjusting the gain, set these registers to 80H (INT0 = 1, DEC[6:0] = 0).

If the gain registers are set to 0, the Y, U, and V component data items are replaced with the values specified by the respective offset registers and transferred to memory.

The values specified by these registers are enabled by the update register. For details, see **3.2.10 Update register**.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
BNGR/CBGR/CRGR							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:8	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
BNGR	R/W	7:0	80H	Luminance gain register Ygain = Yin × BNGR
CBGR	R/W	7:0	80H	U color difference gain register Ugain = Uin × CBGR
CRGR	R/W	7:0	80H	V color difference gain register Vgain = Vin × CRGR

(2) Offset registers (Luminance signal, U color difference signal, V color difference signal)

These registers (CA_BNZR: 400B_0040H, CA_CBZR: 400B_0048H, CA_CRZR: 400B_0050H) are used to add and reduce the offset for data after gain adjustment. The values can be specified for Y, U, and V, respectively.

These registers store a signed 8-bit integer value. The MSB (sign bit) indicates the sign and the 7 bits from the LSB (OD[6:0]) indicate the integer part. Values from −128 to +127 can be specified. If not adjusting the gain, set these registers to 0H.

These registers specify the Y/U/V data value when the gain registers are set to 0. If the register corresponding to the component data is set to 0, the data is replaced with the value specified by the offset register and transferred to memory. By using this mode, the color of an image can be converted to monochrome or sepia and transferred.

The values specified by these registers are enabled by the update register. For details, see **3.2.10 Update register**.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
BNZR/CBZR/CRZR							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:8	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
BNZR	R/W	7:0	0H	Luminance offset register Yoffset = Ygain + BNZR Specify a signed 8-bit integer from −128 to +127 (2's complement) for BNZR.
CBZR	R/W	7:0	0H	U color difference offset register Uoffset = Ugain + CBZR Specify a signed 8-bit integer from −128 to +127 (2's complement) for CBZR.
CRZR	R/W	7:0	0H	V color difference offset register Voffset = Vgain + CRZR Specify a signed 8-bit integer from −128 to +127 (2's complement) for CRZR.

3.2.5 Transfer control registers

(1) Transfer control register

This register (CA_DMACNT: 400B_0080H) controls data transfer.

Change the values only when DMA transfer is not being performed (transfer request register = 0H).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved			MAINYUV	Reserved		MAINREC	

7	6	5	4	3	2	1	0
Reserved		MAINMODE		Reserved	MNRESIZE	PCULLR	

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31:13	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
MAINYUV	R/W	12	0H	Specifies the format of main frame output to memory. 0: YUV422 1: YUV420
Reserved	R	11:10	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
MAINREC	R/W	9:8	0H	Indicates the history of the last frame transferred as a main frame. The history can be checked by reading these bits[Note 1]. Writing 1, 1 clears the history. Writing other values is invalid.
Reserved	R	7:6	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.

MAINREC1	MAINREC0	Read	Write
0	0	A frame	–
0	1	A frame	–
1	0	B frame	–
1	1	B frame	Clears the history

(2/2)

<table>
<tr><th>Name</th><th>R/W</th><th>Bit</th><th>After Reset</th><th>Function</th></tr>
<tr><td>MAINMODE</td><td>R/W</td><td>5:4</td><td>0H</td><td>Specifies the main frame transfer mode.
<table>
<tr><th>MAIN MODE1</th><th>MAIN MODE0</th><th>Transfer Mode</th></tr>
<tr><td>0</td><td>0</td><td>Single transfer
Only one frame is transferred to the frame specified by the transfer frame register.</td></tr>
<tr><td>0</td><td>1</td><td>Repeat transfer (frame buffer fixed)
A frame is repeatedly transferred to the destination specified by the transfer frame register.</td></tr>
<tr><td>1</td><td>0</td><td>Repeat transfer (double buffer)Note 2
A and B frames are transferred alternately, starting with an A frame.</td></tr>
<tr><td>1</td><td>1</td><td>Repeat transfer (double buffer)Note 2
A and B frames are transferred alternately, starting with an A frame.</td></tr>
</table></td></tr>
<tr><td>Reserved</td><td>R</td><td>3</td><td>0H</td><td>Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.</td></tr>
<tr><td>MNRESIZE</td><td>R/W</td><td>2</td><td>0H</td><td>Specifies whether to resize main frames.
0: Does not resize main frames.
1: Resizes main frames.</td></tr>
<tr><td>PCULLR</td><td>R/W</td><td>1:0</td><td>0H</td><td>Specifies the skipping ratio of transfer frames. If no skipping mode is specified, every data frame is transferred. If a skipping ratio is specified, one data frame is transferred at intervals of the specified ratio.
<table>
<tr><th>PCULLR1</th><th>PCULLR0</th><th>Mode</th><th>Transfer Rate in 30 fps Operation</th></tr>
<tr><td>0</td><td>0</td><td>No skipping</td><td>30 fps</td></tr>
<tr><td>0</td><td>1</td><td>1/2 skipping</td><td>15 fps</td></tr>
<tr><td>1</td><td>0</td><td>1/3 skipping</td><td>10 fps</td></tr>
<tr><td>1</td><td>1</td><td>1/4 skipping</td><td>7.5 fps</td></tr>
</table></td></tr>
</table>

Caution The operation will not be guaranteed if the values of this register are changed while DMA transfer is being requested or while CAM is operating.

Notes 1. The history value becomes valid after transfer is complete.

2. To perform repeat transfer (double buffer), reset CAM immediately before transfer.

(2) Transfer frame register

This register (CA_FRAME: 400B_0084H) specifies the transfer frame destination. This setting is valid when single transfer or repeat transfer (frame buffer fixed) is specified in the transfer control register.

Change the values while DMA transfer is not being performed (transfer request register = 0H).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						MAINFRM	

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
MAINFRM	R/W	1:0	1H	Specifies the transfer destination of a main frame. This setting is valid when single transfer or repeat transfer (frame buffer fixed) is specified by the transfer control register.

MAINFRM1	MAINFRM0	Frame
0	0	A frame
0	1	A frame
1	0	B frame
1	1	B frame

(3) Transfer request register

This register (CA_DMAREQ: 400B_0088H) specifies the starting of DMA transfer.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							MAINREQ

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
MAINREQ	R	0	0H	This bit is set to 1 when DMAREQ is acknowledged. This bit is cleared when DMA transfer terminates. In single transfer mode, this bit is cleared automatically after the end of 1-frame transfer.
	W		–	Requests DMA transfer when set to 1. The operation varies depending on the value of the MAINMODE bit of the transfer control register (CA_DMACNT). Single transfer mode: 1-frame transfer is performed. Repeat transfer mode: DMA transfer is repeated until the MAINSTOP bit of the CA_DMASTOP register is set to 1. Writing 0 to the MAINREQ bit does not affect the setting.

(4) Transfer request cancellation register

This register (CA_DMASTOP: 400B_008CH) stops transfer during repeat transfer. This register is enabled at transfer frame termination after request cancellation is specified. The transfer request status can be checked by polling the transfer request register.

This is a write-only register. Writing 1 terminates DMA transfer. Writing 0 to this register does not affect the setting.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							MAINSTOP

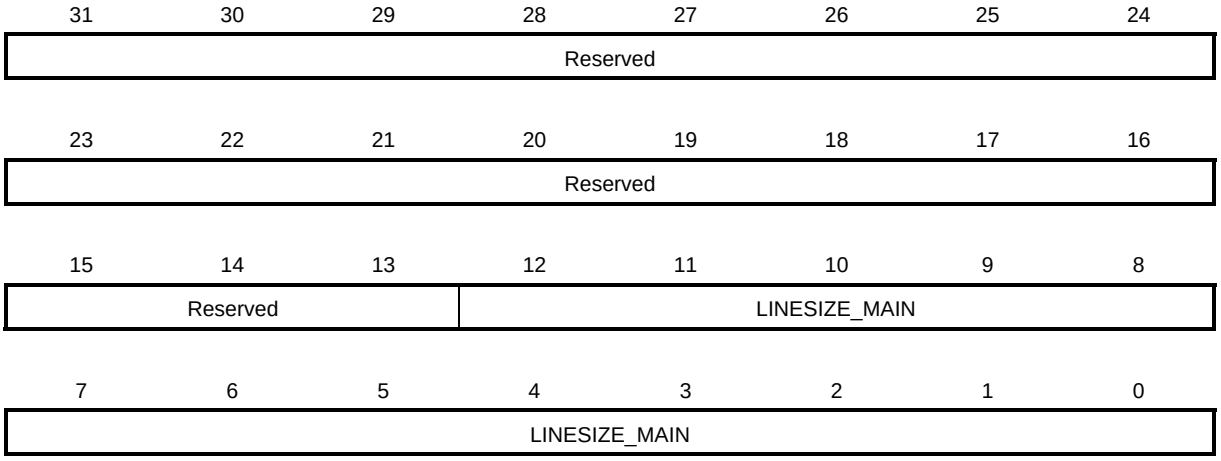
Name	R/W	Bit	After Reset	Function
Reserved	W	31:1	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
MAINSTOP	W	0	0H	Stops main frame repeat transfer. 1: Stops transfer.

3.2.6 Address addition value register

(1) Address addition value register

This register (CA_LINESIZE_MAIN: 400B_0100H) specifies the address size of one line of a transfer image. By using another method to specify the address size of one line of an image already saved in the transfer destination memory, a camera image in the required rectangular position can be sent to overwrite an image on the memory.

The values specified by this register are enabled by the update register. For details, see **3.2.10 Update register**.



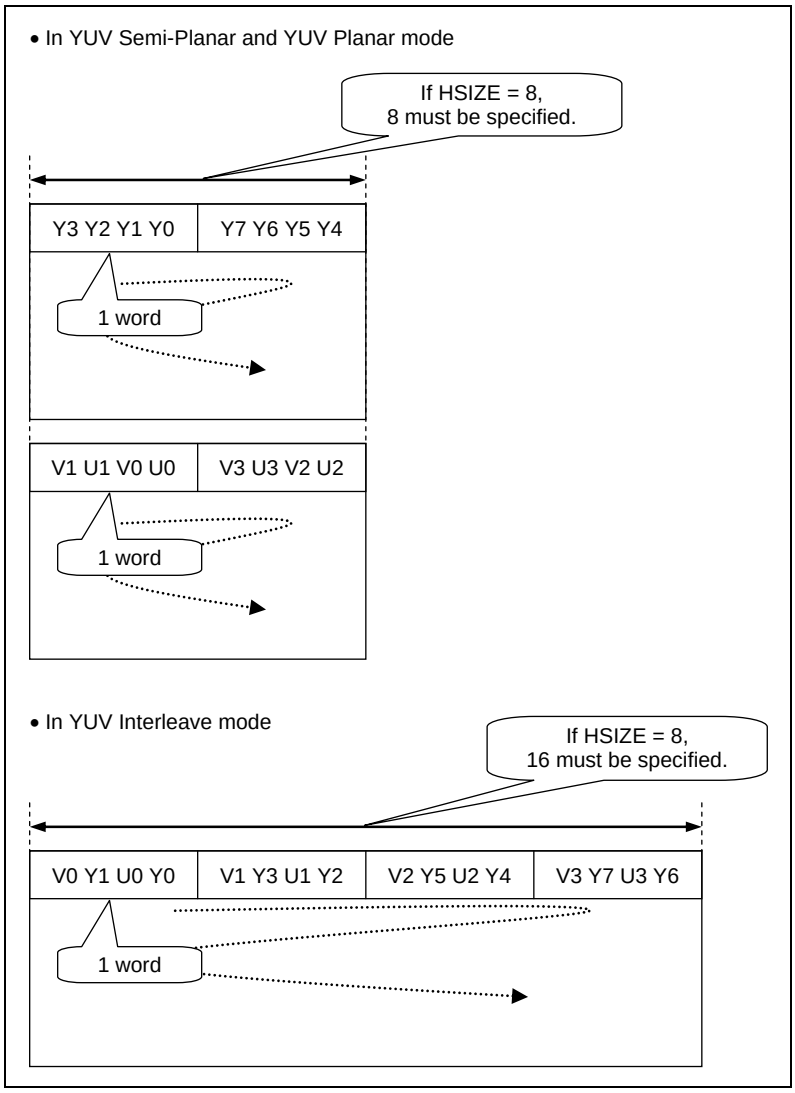
Name	R/W	Bit	After Reset	Function
Reserved	R	31:13	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
LINESIZE_MAIN	R/W	12:0	0H	Specifies the address addition value for one line. (The lower 2 bits are fixed to 0.)

Caution The specifiable value varies between the YUV420/YUV422 Semi-Planar mode and YUV422 Interleave mode (see 3.2.2 (1) Camera control register (CA_CSR)).

Table 3-5. Minimum Specifiable Unit

Output Format	Pixel Mode	Minimum Specifiable Unit
YUV422	YUV Interleave	4 bytes (1 word) (2 pixels)
	YUV Semi-Planar	4 bytes (1 word) (4 pixels)
	YUV Planar	8 bytes (2 words) (8 pixels)
YUV420	YUV Semi-Planar	4 bytes (1 word) (4 pixels)
	YUV Planar	8 bytes (2 words) (8 pixels)

Figure 3-4. Memory Storage and Specified Values



3.2.7 Resize registers

(1) Horizontal reduction ratio register

This register (CA_XRATIO_MAIN: 400B_0104H) specifies a reduction ratio in the horizontal direction. This register is valid when the RESIZE bit of the CA_DMACNT register is set to 1.

The values specified by this register are enabled by the update register. For details, see **3.2.10 Update register**.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved						XRATIO_MAIN	

7	6	5	4	3	2	1	0
XRATIO_MAIN							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:10	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
XRATIO_MAIN	R/W	9:0	0H	Specifies a reduction ratio in the horizontal direction. The specifiable range is 0 to 959. Reduction transfer becomes valid when the MNRESIZE bit of the CA_DMACNT register is set to 1. In this case, reduction is not performed if XRATIO is set to 0. The reduction ratio is obtained according to XRATIO, by the following equation. $\text{Reduction ratio} = \frac{64}{64 + \text{XRATIO}}$

(2) Vertical reduction ratio register

This register (CA_YRATIO_MAIN: 400B_0108H) specifies a reduction ratio in the vertical direction. This register is valid when the RESIZE bit of the CA_DMACNT is set to 1.

The values specified by this register are enabled by the update register. For details, see **3.2.10 Update register**.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved						YRATIO_MAIN	

7	6	5	4	3	2	1	0
YRATIO_MAIN							

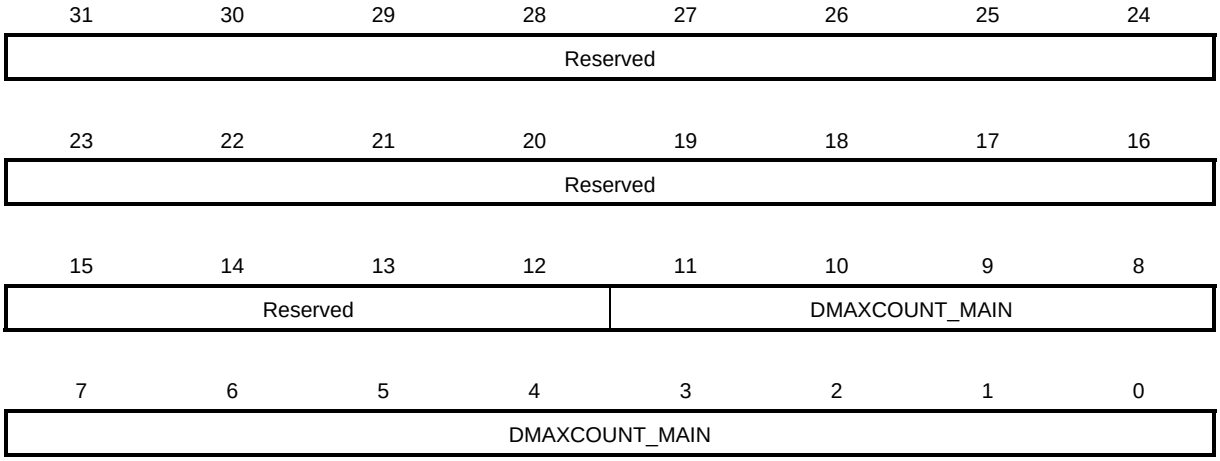
Name	R/W	Bit	After Reset	Function
Reserved	R	31:10	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
YRATIO_MAIN	R/W	9:0	0H	Specifies a reduction ratio in the vertical direction. The specifiable range is 0 to 959. Reduction transfer becomes valid when the MNRESIZE bit of the CA_DMACNT register is set to 1. In this case, reduction is not performed if YRATIO is set to 0. The reduction ratio is obtained according to YRATIO, by the following equation. $\text{Reduction ratio} = \frac{64}{64 - \text{YRATIO}}$

3.2.8 Frame control registers

(1) Horizontal transfer size register

This register (CA_DMAX_MAIN: 400B_010CH) specifies the number of horizontal pixels to be transferred. Specify the transfer pixels for each mode based on the minimum pixel units (YUV422 Interleave mode: 2-pixel units, Semi-Planar mode: 4-pixel units, and Planar mode: 8-pixel units).

The values specified by this register are enabled by the update register. For details, see **3.2.10 Update register**.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:12	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
DMAXCOUNT_MAIN	R/W	11:0	0H	Specifies the number of horizontal pixels to be transferred (4,088 max.). Specify in 2-, 4- or 8-pixel units depending on the mode. (The lowest bit is fixed to 0.)

Caution The minimum specifiable value varies between the YUV420/YUV422 Semi-Planar mode and YUV422 Interleave mode (see 3.2.2 (1) Camera control register (CA_CSR)).

(2) Vertical transfer size register

This register (CA_DMAY_MAIN: 400B_0110H) specifies the number of lines to be transferred vertically. The number of lines to be transferred can be specified in line units.

The values specified by this register are enabled by the update register. For details, see **3.2.10 Update register**.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved				DMAYCOUNT_MAIN			

7	6	5	4	3	2	1	0
DMAYCOUNT_MAIN							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:12	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
DMAYCOUNT_MAIN	R/W	11:0	0H	Specifies the number of lines to be transferred vertically (4,088 max.). The value can be specified in line units.

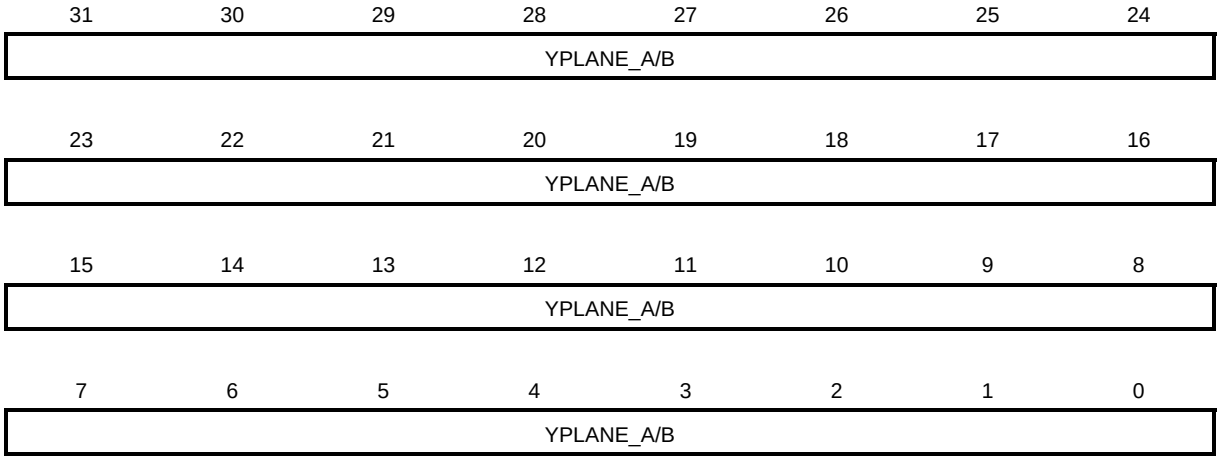
(3) Y plane transfer address registers (A/B frame)

These registers (CA_YPLANE_A: 400B_0114H, CA_YPLANE_B: 400B_011CH) specify the transfer destination addresses of Y plane data.

To support double buffer control, two frame setting registers for main frames A and B are provided.

For details about double buffer control, see **4.11.2 Transfer mode**.

Change the values while DMA transfer is not being performed (transfer request register = 0H).



Name	R/W	Bit	After Reset	Function
YPLANE_A/B	R/W	31:0	0H	Specifies a Y plane address. The lower 2 bits are fixed to 0.

Caution In the YUV422 Interleave mode (see 3.2.2 (1) Camera control register (CA_CSR)), all the YUV data is output to the addresses specified by these registers.

(4) UV plane transfer address registers (A/B frame)

These registers (CA_UVPLANE_A: 400B_0118H, CA_UVPLANE_B: 400B_0120H) specify the transfer destination addresses of UV plane data.

To support double buffer control, two frame setting registers for main frames A and B are provided.

For details about double buffer control, see **4.11.2 Transfer mode**.

Change the values while DMA transfer is not being performed (transfer request register = 0H).

31	30	29	28	27	26	25	24
UVPLANE_A/B							

23	22	21	20	19	18	17	16
UVPLANE_A/B							

15	14	13	12	11	10	9	8
UVPLANE_A/B							

7	6	5	4	3	2	1	0
UVPLANE_A/B							

Name	R/W	Bit	After Reset	Function
UVPLANE_A/B	R/W	31:0	0H	Specifies a UV plane address. The lower 2 bits are fixed to 0.

Caution The addresses specified by these registers are ignored in the YUV422 Interleave mode (see 3.2.2 (1) Camera control register (CA_CSR)).

(5) V plane transfer address register (A/B frame)

These registers (CA_VPLANE_A: 400B_0244H, CA_VPLANE_B: 400B_0248H) specify the transfer destination addresses of V plane data.

To support double buffer control, two frame setting registers for main frames A and B are provided.

For details about double buffer control, see **4.11.2 Transfer mode**.

Change the values while DMA transfer is not being performed (transfer request register = 0H).

31	30	29	28	27	26	25	24
VPLANE_A/B							

23	22	21	20	19	18	17	16
VPLANE_A/B							

15	14	13	12	11	10	9	8
VPLANE_A/B							

7	6	5	4	3	2	1	0
VPLANE_A/B							

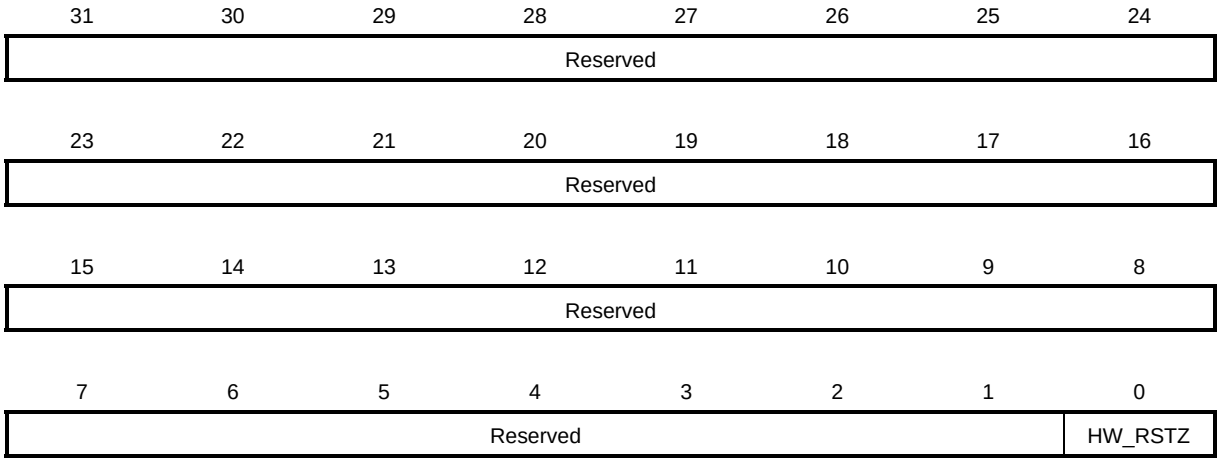
Name	R/W	Bit	After Reset	Function
VPLANE_A/B	R/W	31:0	0H	Specifies a V plane address. The lower 2 bits are fixed to 0.

Caution The addresses specified by these registers are ignored in the YUV422 Interleave and YUV420/422 Semi-planar modes (see 3.2.2 (1) Camera control register (CA_CSR)).

3.2.9 Module control register

(1) Module control register

This register (CA_MODULECONT: 400B_022CH) initializes a module synchronizing with CAM_CLKI.



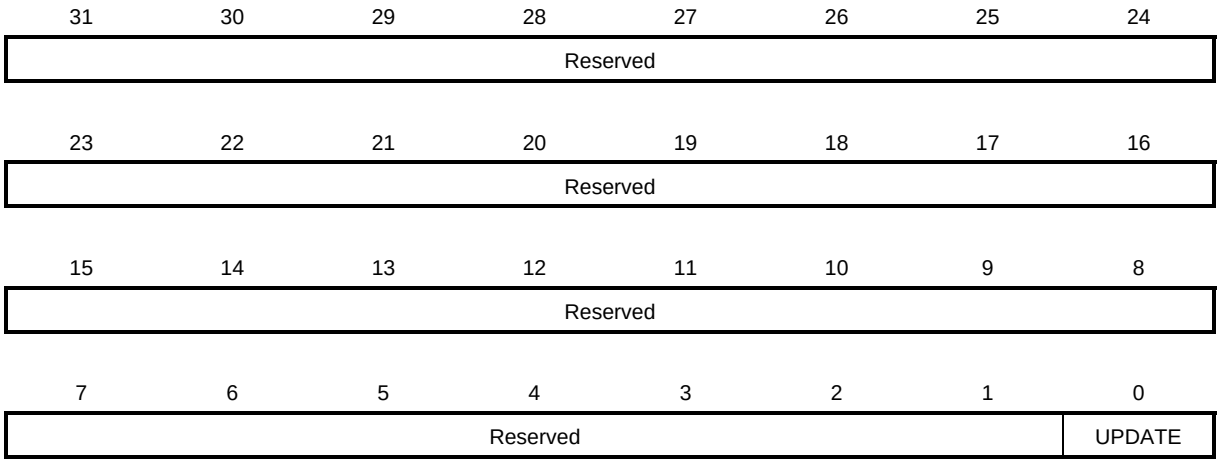
Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
HW_RSTZ	R/W	0	0H	Performs hardware reset of modules operating with CAM_CLKI. 0: Reset 1: Cancels reset.

Caution The operation will not be guaranteed if the values of this register are changed while DMA transfer is being requested or while CAM is operating.

3.2.10 Update register

(1) Update register

This register (CA_UPDATE: 400B_0230H) enables the capture position, capture size, resize ratio, DMA transfer size, YUV offset/gain, and flipping specified by the corresponding register. Writing 1 to the UPDATE bit sets the update reservation status in which each specified value is ready to be updated. When a register is updated (defined by the LD_TMG bit of camera control register), each specified value is enabled and the update register is cleared. Writing 0 to this register does not affect the setting.

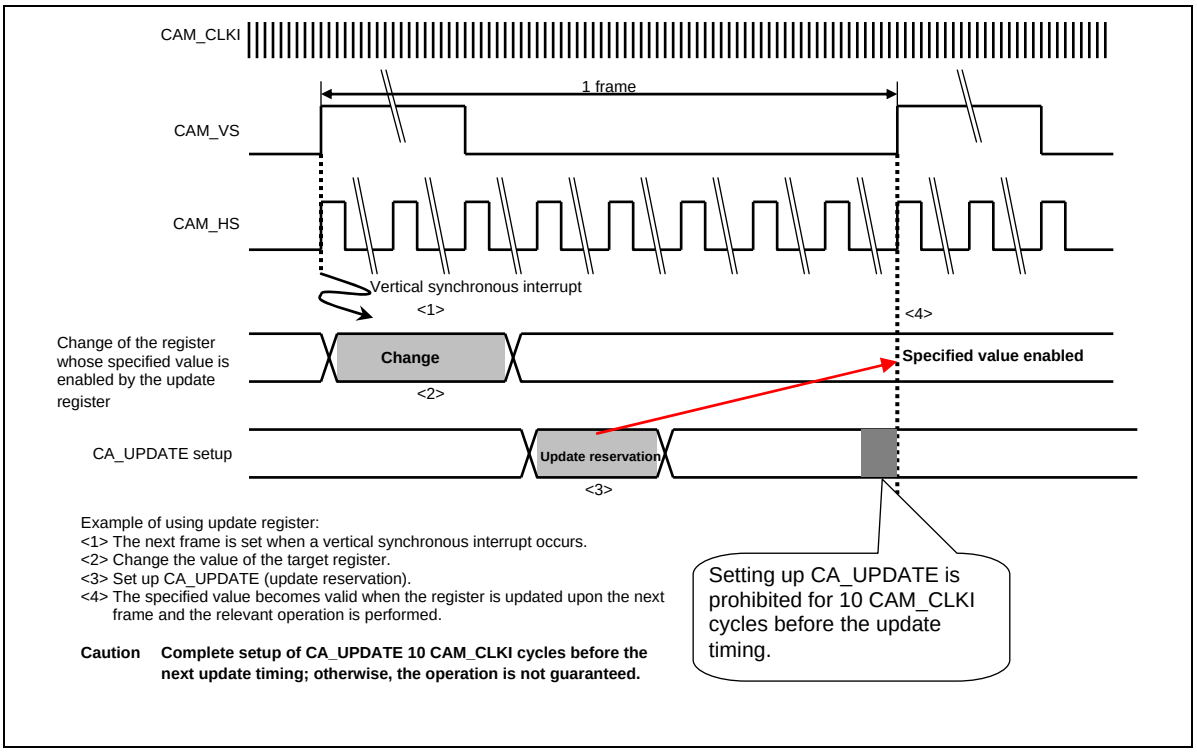


Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
UPDATE	R	0	0H	Specifies the update reservation status. 0: The set values are not updated. 1: The set values are updated at the register update timing.
	W			Enables the value specified by a specific register. 1: Reservation for updating

Caution The values specified by the following registers are enabled by the update register. Do not change the values of registers other than the update register while DMA transfer is being requested or while CAM is operating.

- CA_X (Y)1(2)R
- CA_X3R
- CA_CBG(Z)R
- CA_LINESIZE_MAIN
- CA_DMAX(Y)_MAIN
- CA_BNG(Z) R
- CA_CRG(Z) R
- CA_X (Y)RATIO_MAIN
- CA_MIRROR

Figure 3-5. Update Register Setup Timing

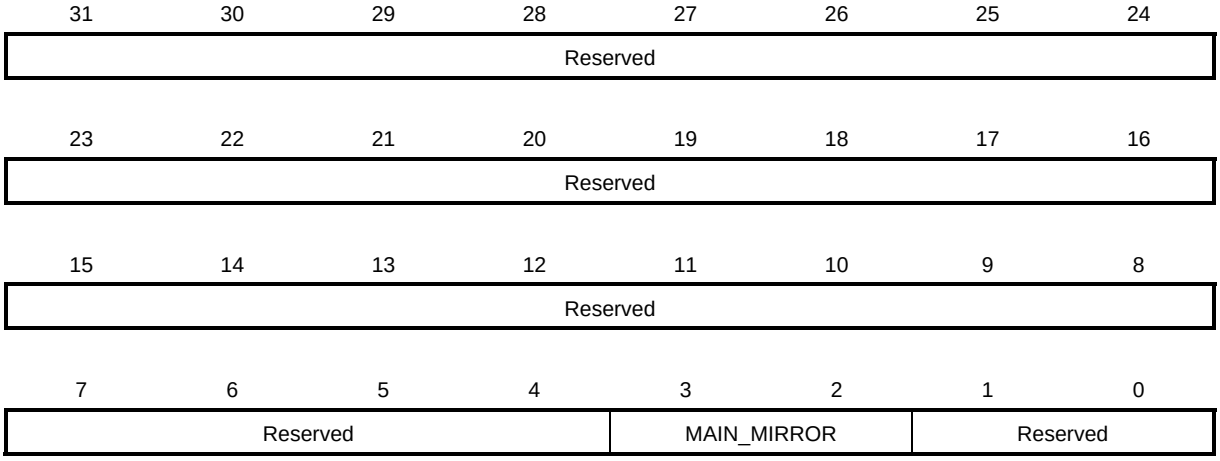


3.2.11 Horizontal/vertical flip control register

(1) Horizontal/vertical flip control register

This register (CA_MIRROR: 400B_0234H) specifies flipping of an image during DMA transfer. Horizontal flip and vertical flip can be specified separately.

The values specified by this register are enabled by the update register. For details, see **3.2.10 Update register**.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:4	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
MAIN_MIRROR	R/W	3:2	0H	Specifies flipping of the main frame. MAIN_MIRROR: 00B – No flip 01B – Horizontal flip 10B – Vertical flip 11B – Horizontal and vertical flip (180° rotation)
Reserved	R	1:0	0H	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.

3.2.12 Simple QoS setting register

(1) Simple QoS setting register

This register (CA_QOS: 400B_0258H) specifies simple QoS.

Simple QoS is used to prevent overrun and underrun from occurring in image-system modules.

When a QoS request is issued from an image-system module, the bus switch temporarily gives a higher priority to accesses from that module, which reduces the access latency.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							QOSEN

7	6	5	4	3	2	1	0
QOSSET							

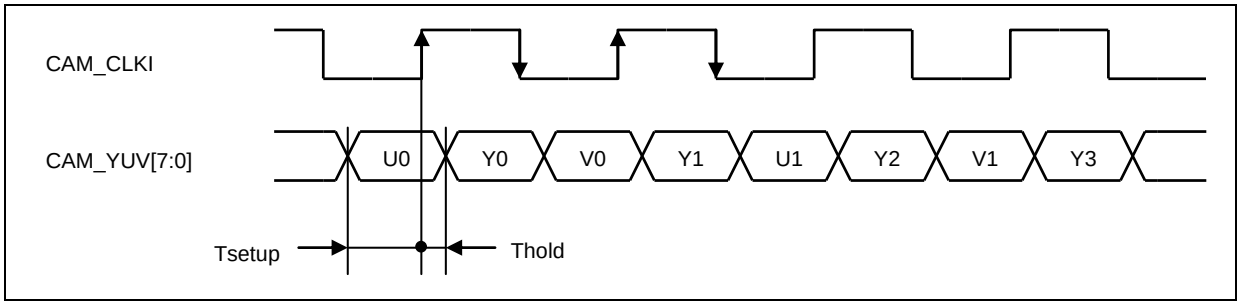
Name	R/W	Bit	After Reset	Function
Reserved	R	31:9	0	Reserved. Do not write any value other than 0. Writing 1 to these bits causes an illegal operation.
QOSEN	R/W	8	0	Specifies whether to enable simple QoS. 0: Disable 1: Enable
QOSSET	R/W	7:0	0	A QoS request is issued if the size of the vacant space in a buffer falls below the value specified in this field.

CHAPTER 4 DESCRIPTION OF FUNCTIONS

4.1 Input Data Capture Timing

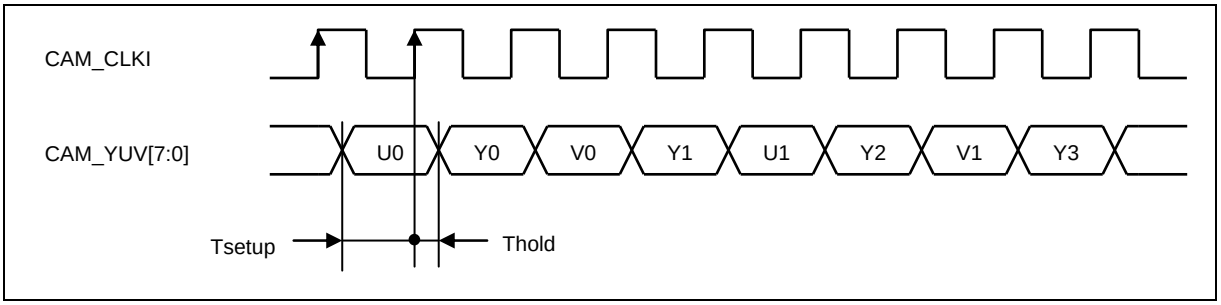
(1) Capture at rising and falling edges

Figure 4-1. Example of Capturing at Rising and Falling Edges



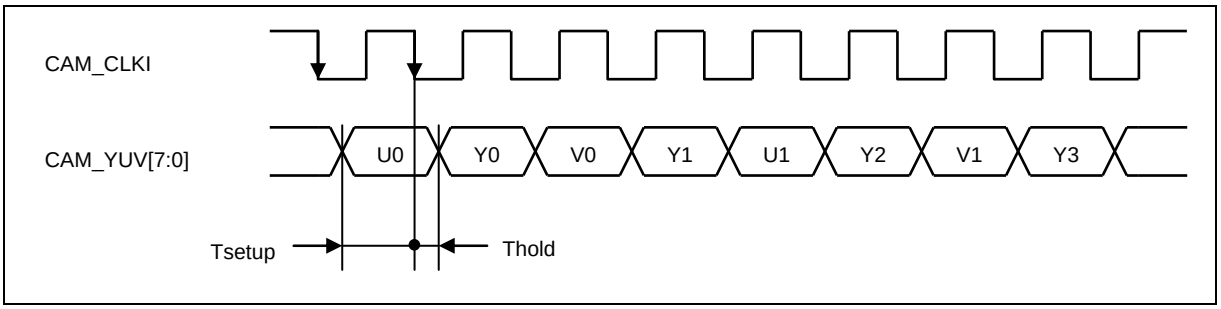
(2) Capture at rising edge

Figure 4-2. Example of Capturing at Rising Edge



(3) Capture at falling edge

Figure 4-3. Example of Capturing at Falling Edge

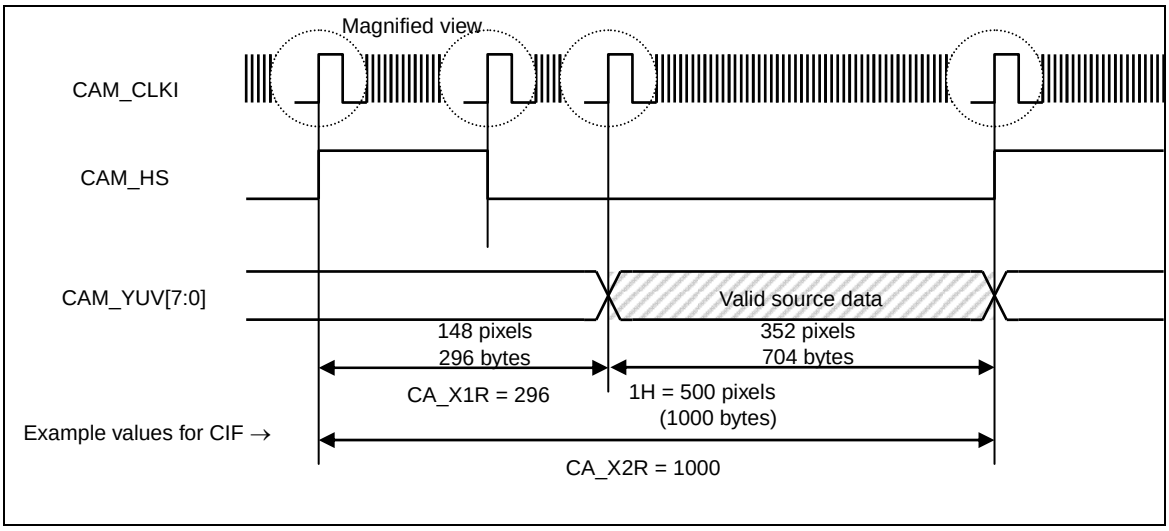


4.2 Horizontal/Vertical Synchronization Signal Sampling

(1) Horizontal synchronization signal sampling timing

The following figure shows an example of the horizontal synchronization signal sampling timing values for CIF (352H × 288V).

Figure 4-4. Horizontal Synchronization Signal Sampling Timing (If CAM_HS Has Positive Logic)

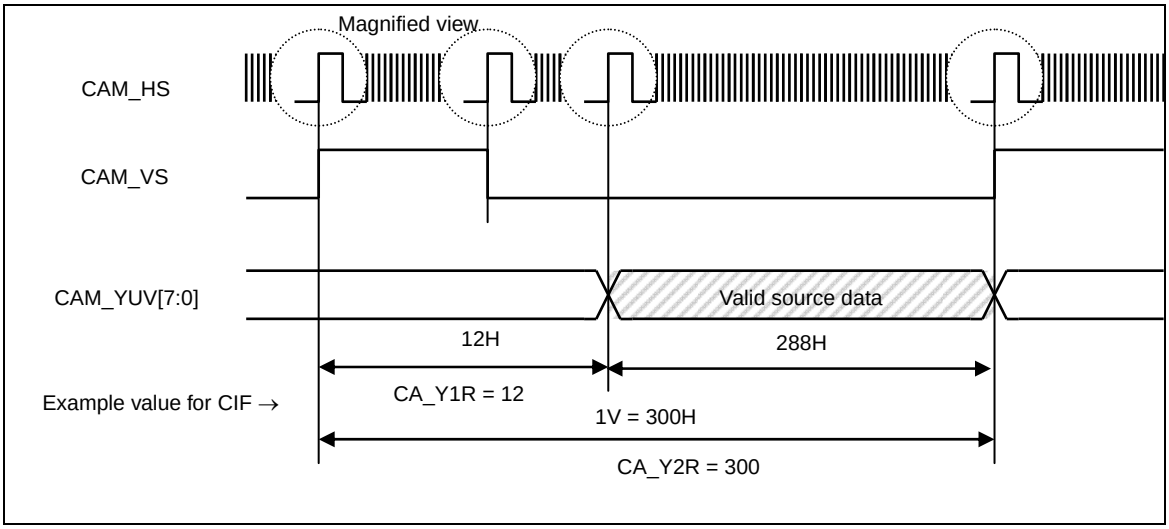


Caution Intervals for CAM_HS must be within the number of CAM_CLKI clocks × 8192. Synchronization at longer intervals is not supported.

(2) Vertical synchronization signal sampling timing

The following figure shows an example of the vertical synchronization signal sampling timing values for CIF (352H × 288V).

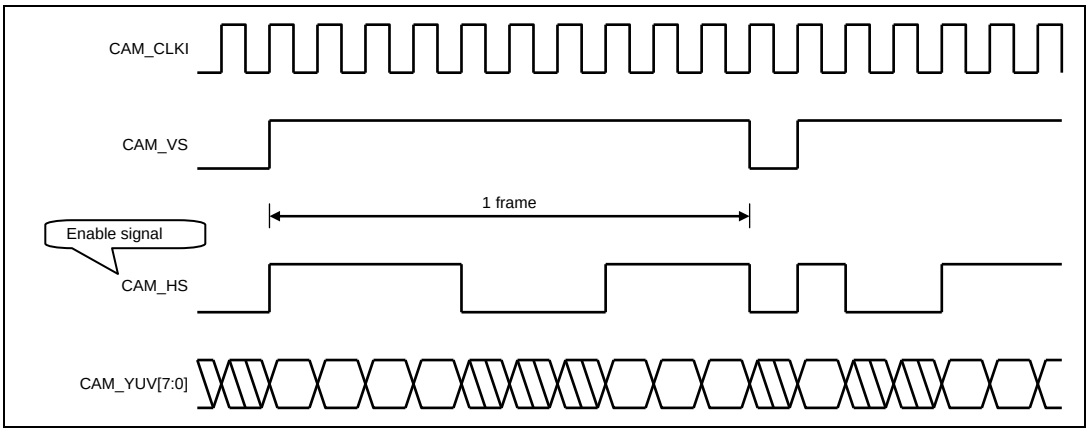
Figure 4-5. Vertical Synchronization Signal Sampling Timing (If CAM_VS Has Positive Logic)



4.3 Enable Signal Sampling

Connect the enable signal to the CAM_HS pin for enable sampling. The period during which the CAM_VS signal is asserted is recognized as one frame and data when the enable signal is valid is captured.

Figure 4-6. Enable Signal Sampling Timing

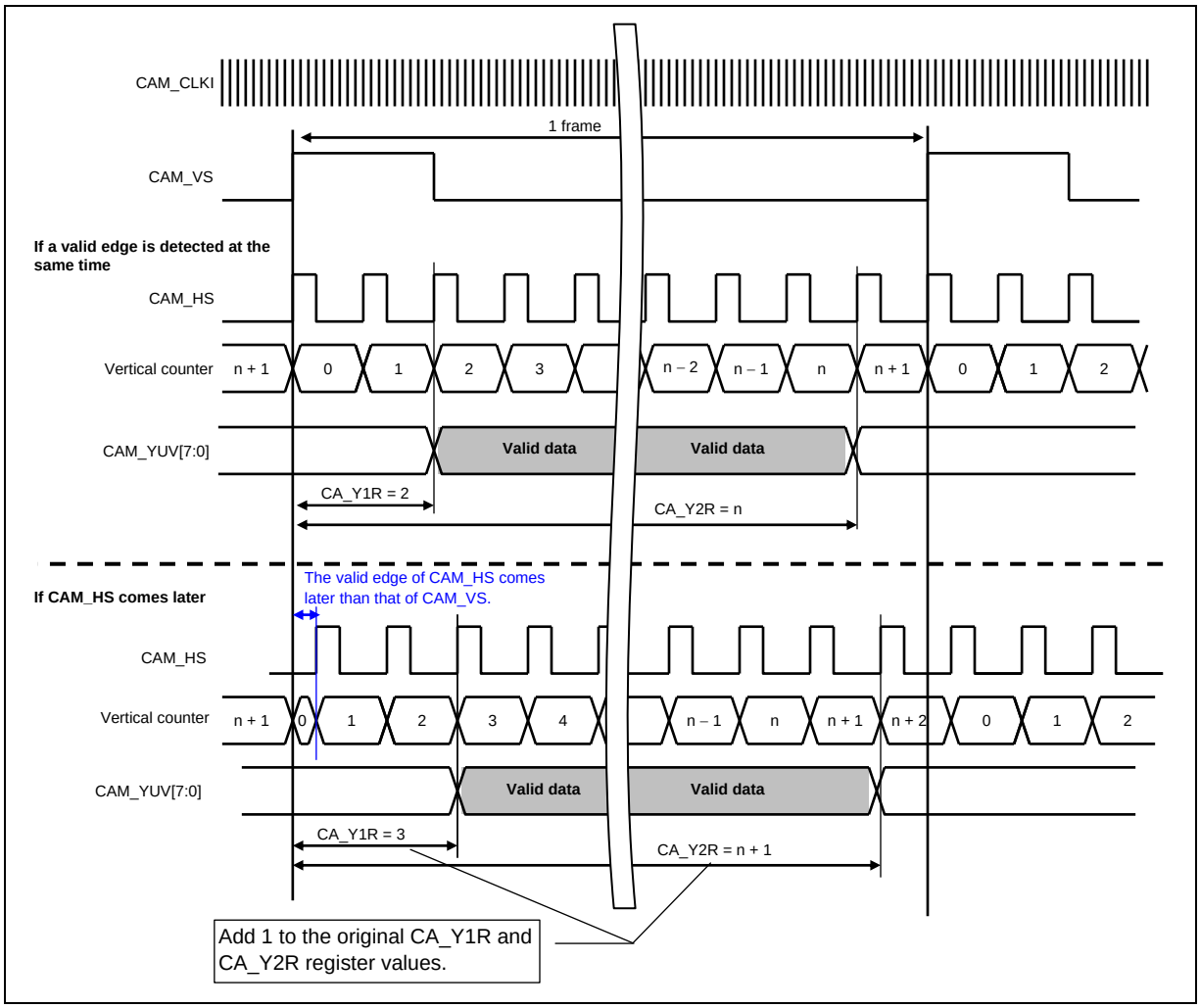


4.4 CAM_VS/CAM_HS Timing and CA_Y1R/CA_Y2R Values

The CAM module is designed assuming that the valid edge timing of CAM_VS and CAM_HS matches. If the valid edge of CAM_HS comes later than that of CAM_VS, the values of the CA_Y1R and CA_Y2R registers must be incremented by 1.

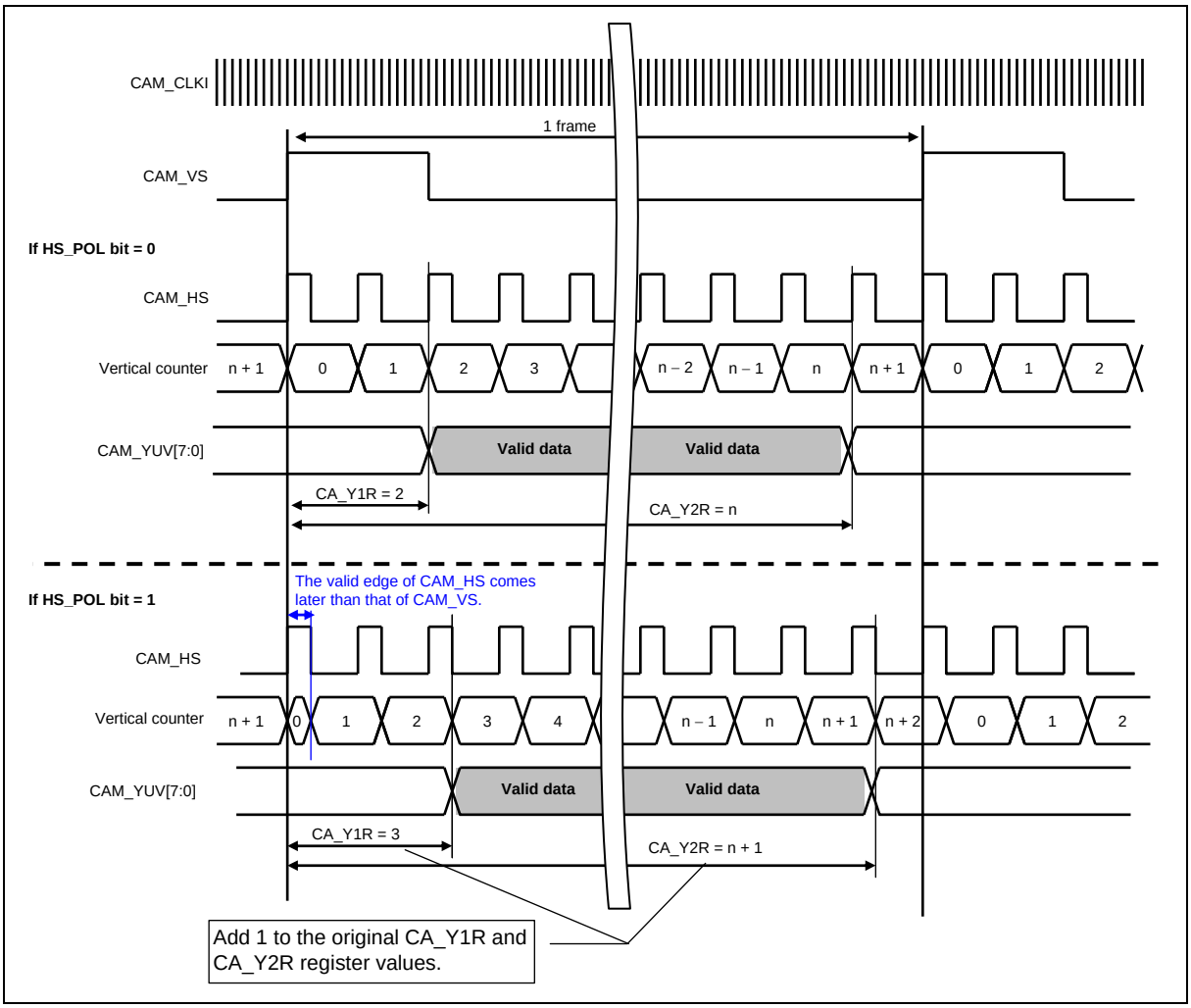
Figure 4-7 shows the relationship between the CAM_VS/CAM_HS input timing and the values specified by the CA_Y1R and CA_Y2R registers.

Figure 4-7. CAM_VS/CAM_HS Timing and CA_Y1R/CA_Y2R Values



If the HS_POL bit is set to 1 at the CAM_VS and CAM_HS input timing shown in Figure 4-8, add 1 to the CA_Y1R and CA_Y2R register values of when the HS_POL bit is set to 0.

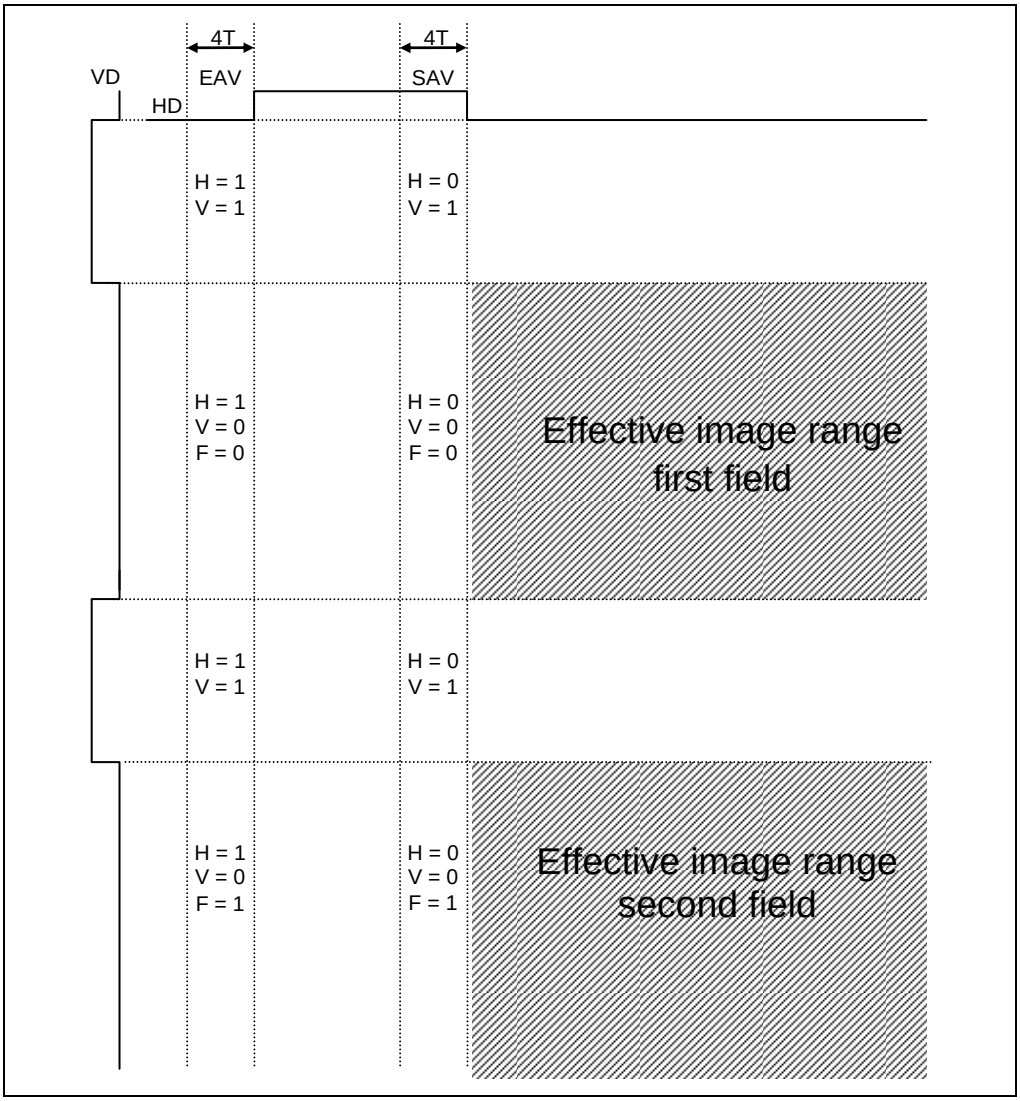
Figure 4-8. CAM_VS/CAM_HS Timing and CA_Y1R/CA_Y2R Values (If CAM_HS Has Negative Logic)



4.5 ITU-R BT.656 Encoding

With ITU-R BT.656, a data field consists of the EAV and SAV fields indicating the synchronization timing. The ITU-R BT.656 encoding mode sets horizontal synchronization and vertical synchronization internally at the timing of the fourth word of the SAV and EAV fields. Figure 4-9 shows a conceptual diagram of the EAV and SAV fields and the synchronization signals.

Figure 4-9. ITU-R BT.656 Encoding Timing



The fields to be stored can be specified by using the 656MODE bit of the camera control register (CA_CSR). The 656MODE bit is valid only when the ITU-R BT.656 mode is selected by using the SYNCMODE bit.

Store operations listed in Table 4-1 can be specified by combinations of the transfer mode specification (MAINMODE) of the transfer control register (CA_DMACNT) and the transfer frame register (CA_FRAME).

Table 4-1. Field Store Operation Selected by Specifying 656MODE Bit

CA_CSR 656MODE Bit	CA_DMACNT MAINMODE Bit	CA_FRAME MAINFRM Bit	Field Store Operation
00	10 (Repeat transfer, double buffer)	Don't care	Starts storing from the first field. Stores the first field to the A frame and the second field to the B frame.
00	01 (Repeat transfer, fixed buffer)	00	Starts storing from the first field. Stores both the first and second fields to the A frame repeatedly.
01	10 (Repeat transfer, double buffer)	Don't care	Starts storing from the second field. Stores the second field to the A frame and the first field to the B frame.
01	01 (Repeat transfer, fixed buffer)	00	Starts storing from the second field. Stores both the first and second fields to the A frame repeatedly.
10	01 (Repeat transfer, fixed buffer)	00	Stores only the first field to the A frame (main frame setting)
10	00 (Single transfer)	Don't care	Prohibited[Note].
11	01 (Repeat transfer, fixed buffer)	10	Stores only the second field to the B frame (main frame setting).
11	00 (Single transfer)	Don't care	Prohibited[Note].

Note In the ITU-R BT.656 mode, specifying single transfer by using the MAINMODE bit is prohibited. To input an image of one frame, specify the repeat transfer mode and stop processing after a transfer completion interrupt has been issued. Figure 4-12 shows storage when one frame is input.

Figure 4-10. Field Data and Storage Frame According to Specification by 656MODE Bit

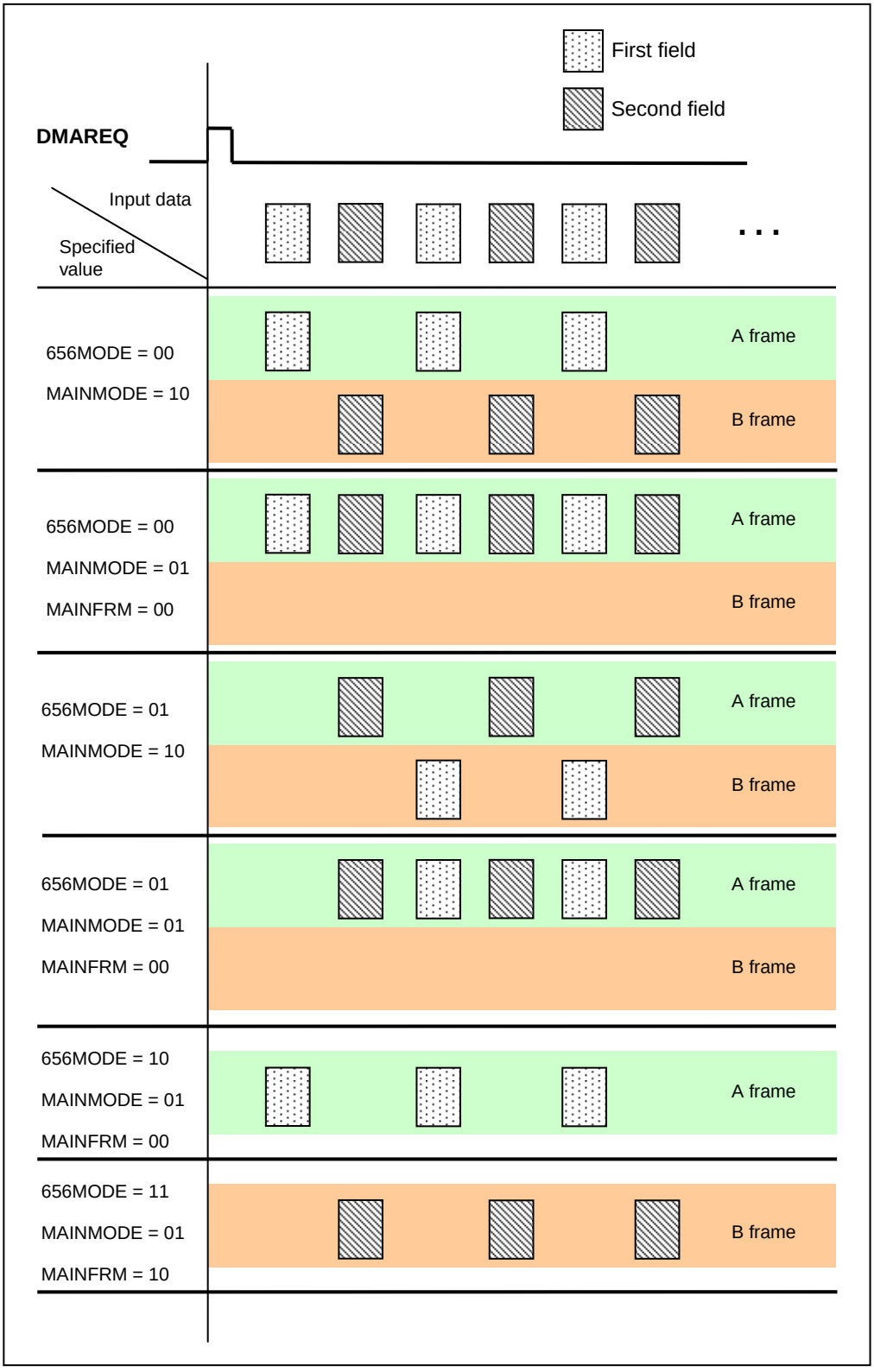


Figure 4-11 shows the timing of a vertical synchronization interrupt and a transfer completion interrupt for each 656MODE bit setting in the ITU-R BT.656 mode.

A vertical synchronization interrupt is output at the beginning of the data (position at which this signal is detected), in frame units. Two-stage registers are then updated when a vertical synchronization interrupt is issued. When data transfer ends, a transfer completion interrupt is issued in field units.

Figure 4-11. Timing of Vertical Synchronization Interrupt and Transfer Completion Interrupt According to Specification by 656MODE Bit

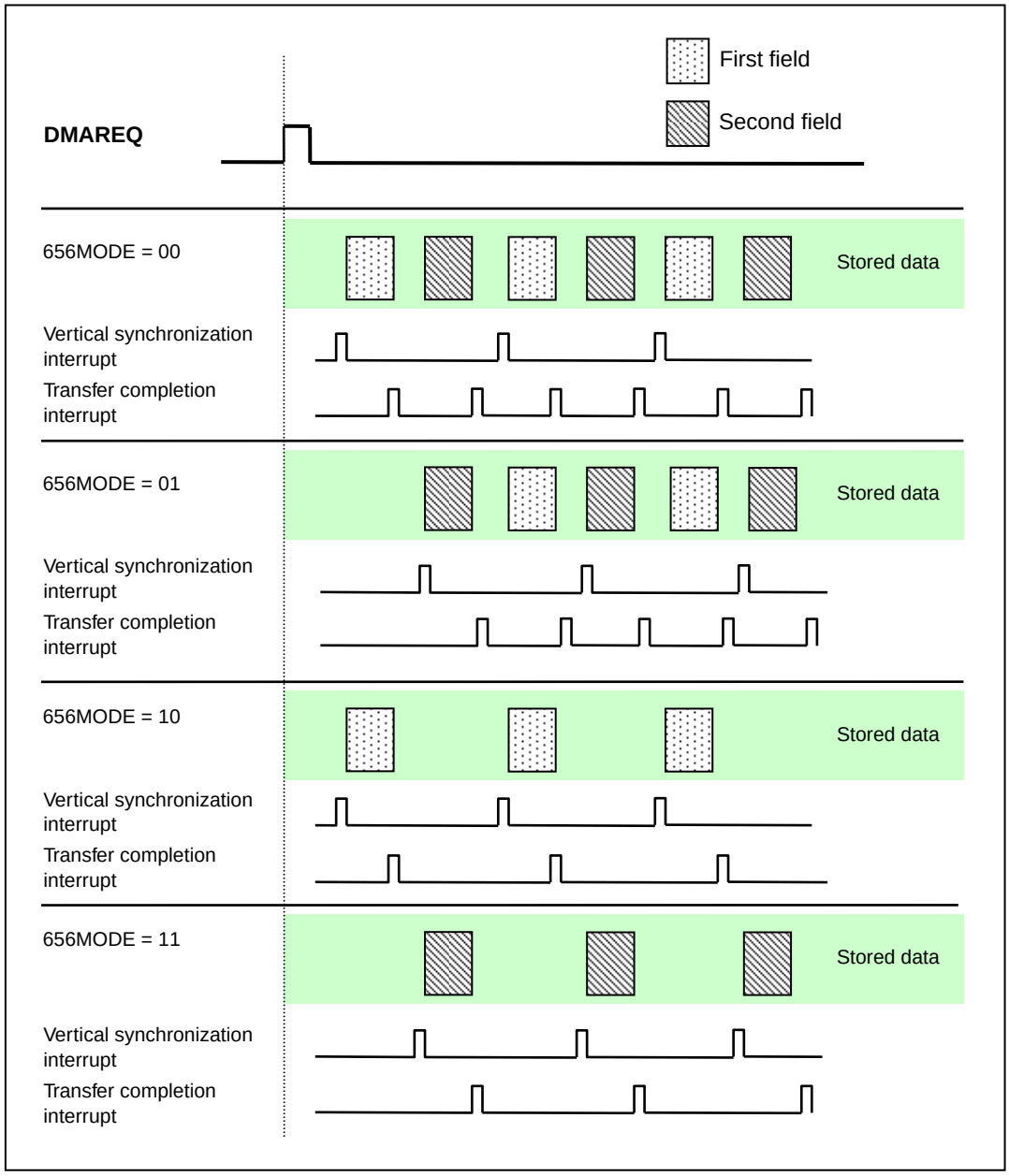
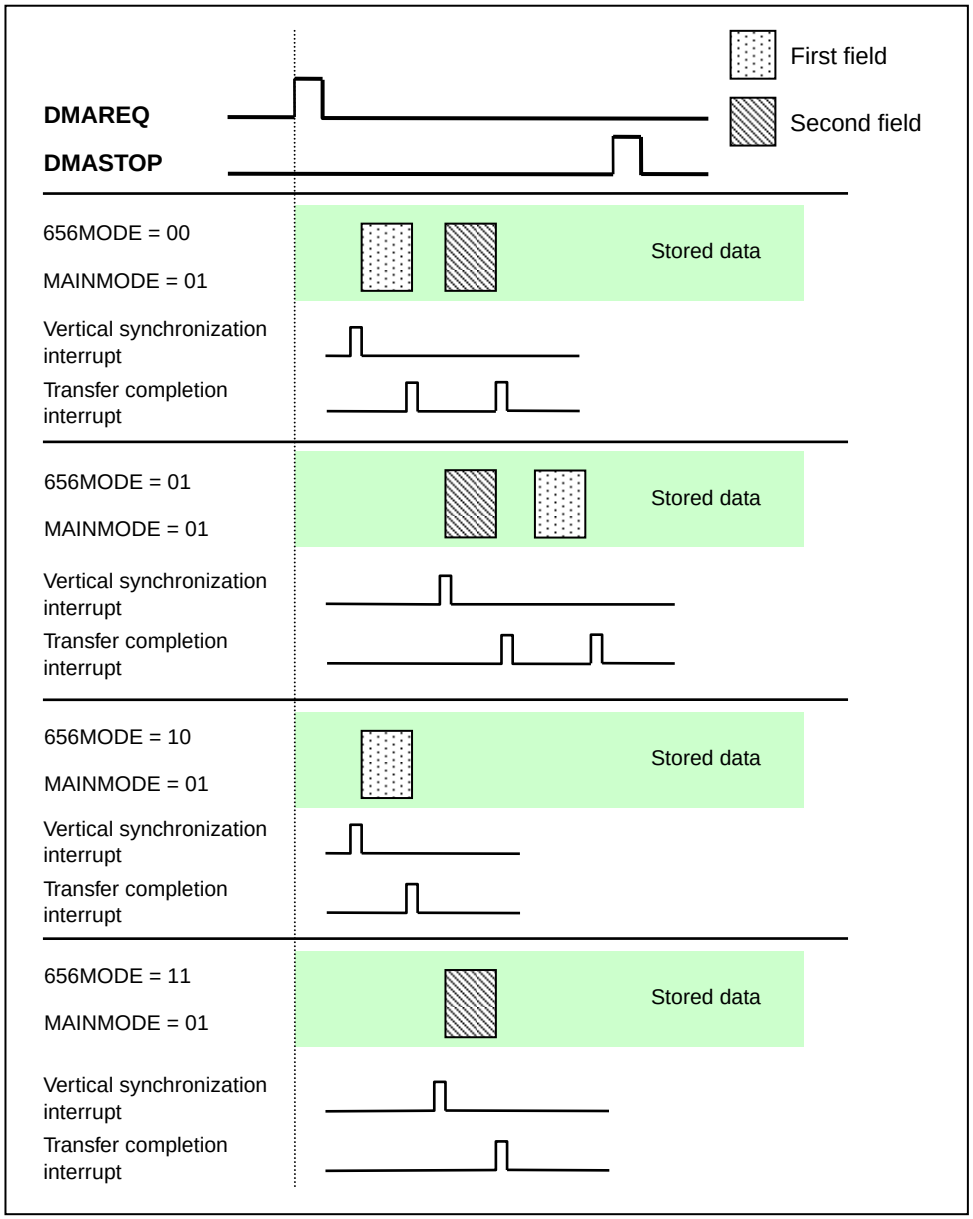


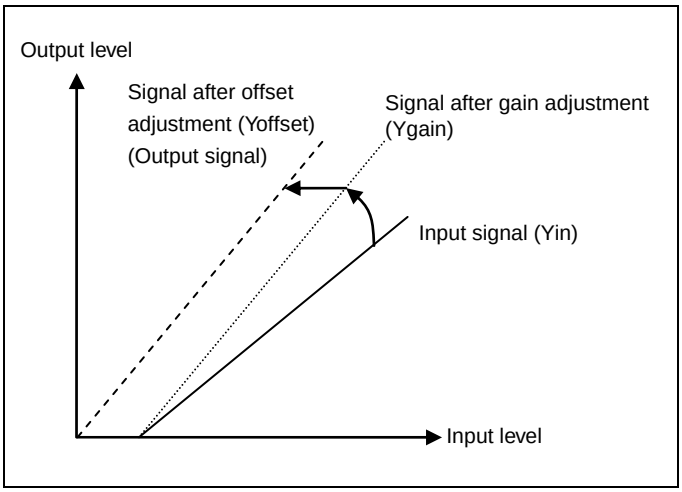
Figure 4-12. Data Storage During 1-Frame Transfer



4.6 Level Adjustment

The gain and offset can be adjusted for the input data level. The gain of data input via the CAM interface is first adjusted, and then the offset value of the data after gain adjustment is performed. Figure 4-13 shows the concept of this processing.

Figure 4-13. Level Adjustment

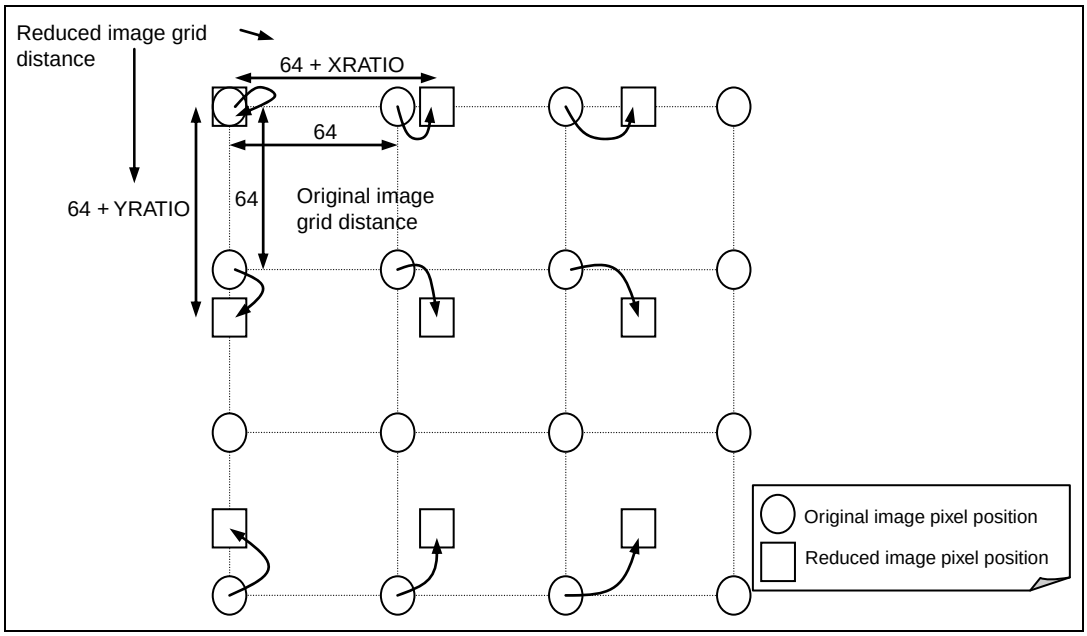


4.7 Reduction Method

The reduction method used is nearest-neighbor sampling, which copies the nearest neighbor pixels of an original image to the pixel positions of a reduced image. As shown in Figure 4-14, a reduced image is generated by finding the relationship between the pixels of the original image and the reduced image, using the method described below.

The pixel-to-pixel distance of an original image is defined to be 64, and a value obtained by adding 64 to the value of the XRATIO/YRATIO register is defined to be the pixel-to-pixel distance of the reduced image, so that the coordinate positions obtained by multiplying this distance by integers function as the pixels of a reduced image. The reduced image is generated by copying the nearest neighbor pixels of an original image to the coordinate positions of the reduced image. Accordingly, the weight center of the pixels of the reduced image shifts by up to 1/2, but the vividness is preserved because the original image is not processed.

Figure 4-14. Reduced Image Sampling



Calculate the value to be set to XRATIO as follows.

$$\text{XRATIO} = \frac{64 \times \text{Input size}}{\text{Output size}} - 64 \text{ (The fractional digits are discarded.)}$$

Example When capturing an image of 320 × 240 pixels and resizing it to 160 × 120 pixels

$$\text{XRATIO} = \frac{64 \times 320}{160} - 64 = 128 - 64 = 64$$

$$\text{YRATIO} = \frac{64 \times 240}{120} - 64 = 128 - 64 = 64$$

4.8 Data Transfer Range Specification

The register setting for the number of transfer pixels varies between normal transfer and resize transfer.

Figure 4-15 shows the relationship between the range of effective data transferred via CAM and the range of data transferred to memory. The following explanation uses the CAM_VS/CAM_HS signal sampling mode as an example, but the setting is the same for the enable signal sampling mode.

4.8.1 Horizontal transfer range

Normal transfer: The number of transfer pixels varies as follows, depending on the value of the clock edge select bit (CLK_EDGE) of the camera control register (CA_CSR).

Rising or falling edge sampling: {(CA_X2R – CA_X1R) / 2} pixels

Rising and falling edge sampling: (CA_X2R – CA_X1R) pixels

Resize transfer: The number of pixels specified by the CA_DMAXCOUNT_MAIN register is used.

Specify a value satisfying the following conditional expressions.

Rising or falling edge sampling:

DMAXCOUNT_MAIN ≤ {(CA_X2R – CA_X1R) / 2} * {64 / (64 + XRATIO_MAIN)}

Rising and falling edge sampling:

DMAXCOUNT_MAIN ≤ (CA_X2R – CA_X1R) * {64 / (64 + XRATIO_MAIN)}

4.8.2 Vertical transfer range

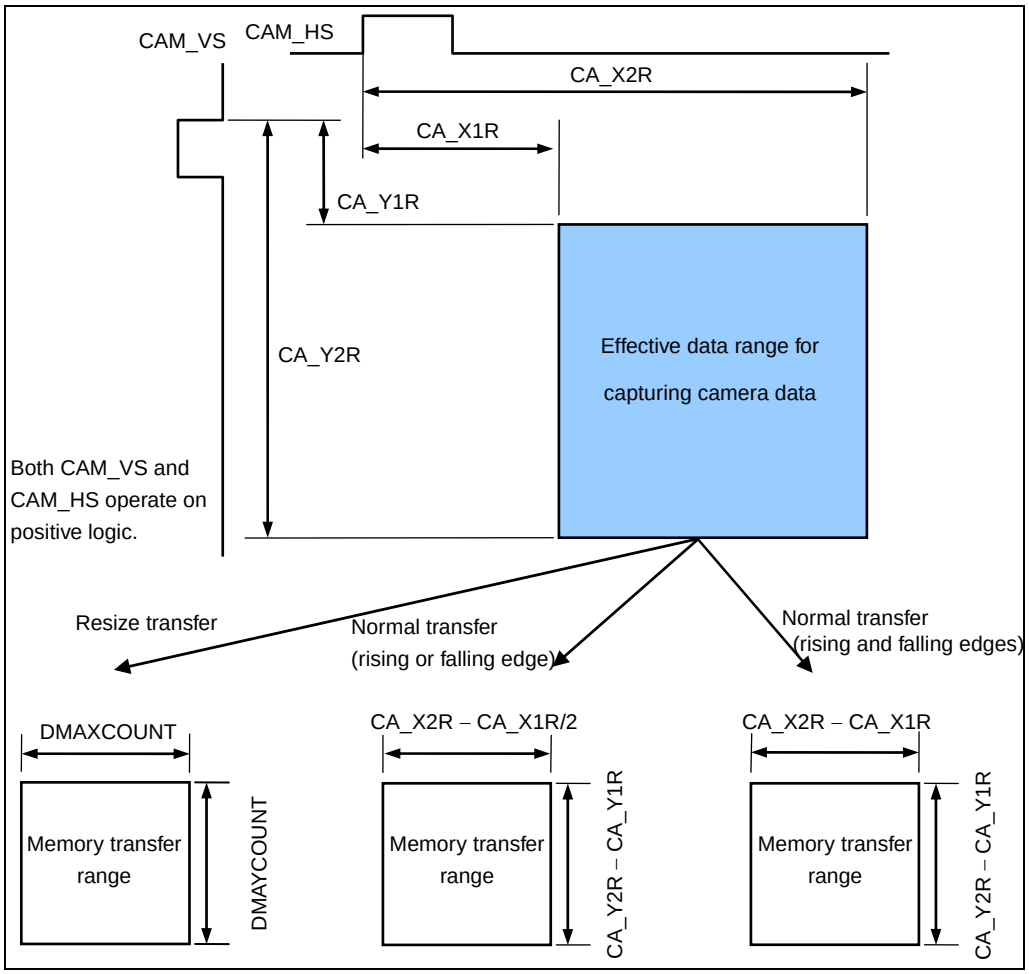
Normal transfer: (CA_Y2R – CA_Y1R)

Resize transfer: The number of pixels specified by the DMAYCOUNT_MAIN register is used.

Specify a value satisfying the following conditional equations.

DMAYCOUNT_MAIN ≤ (CA_Y2R – CA_Y1R) * {64 / (64 + YRATIO_MAIN)}

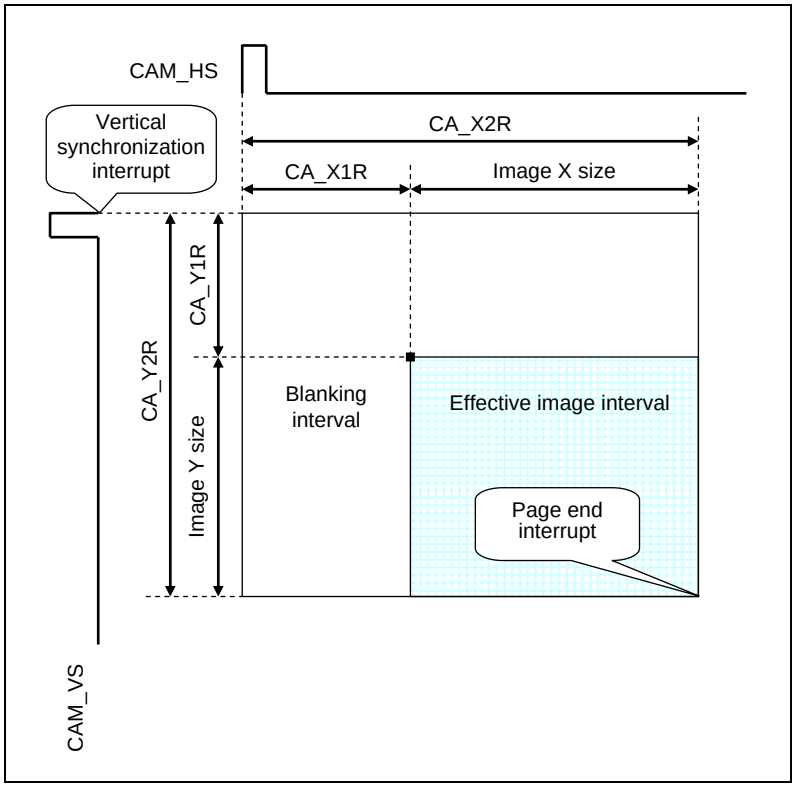
Figure 4-15. Data Transfer Range



4.9 Restrictions on Data Transfer Range Values

4.9.1 Vertical/horizontal synchronization signal sampling

Figure 4-16. CAM_VS/CAM_HS Signal Sampling



Set up the registers as follows.

Register Name	Condition
CA_Y2R	CA_Y2R = Image Y size + CA_Y1R
CA_Y1R	0 ≤ CA_Y1R
CA_X2R	CA_X2R = (Image X size × 2) + CA_X1R (rising or falling edge)
	CA_X2R = Image X size + CA_X1R (rising and falling edges)
CA_X1R	0 ≤ CA_X1R

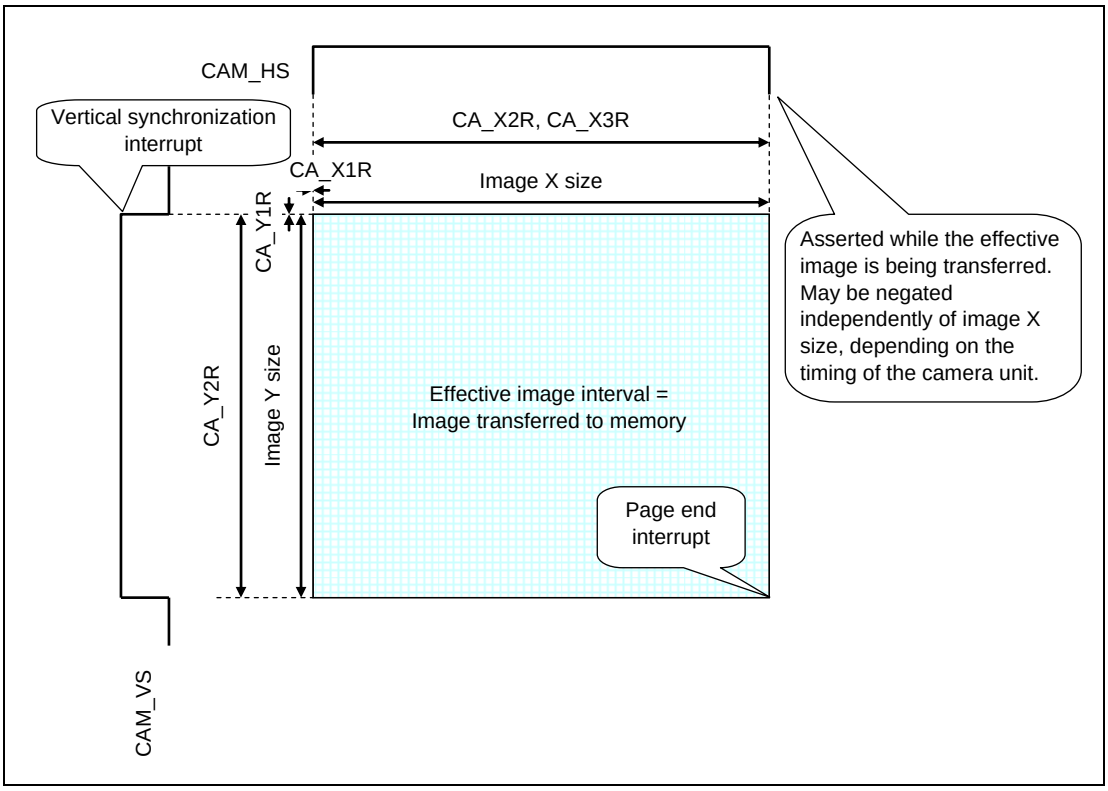
Caution The value set to CA_X3R is ignored.

4.9.2 Enable signal sampling

(1) Normal

All the effective image data input via the CAM interface is captured and written to the frame memory.

Figure 4-17. Enable Signal Sampling (Normal)



Set up the registers as follows.

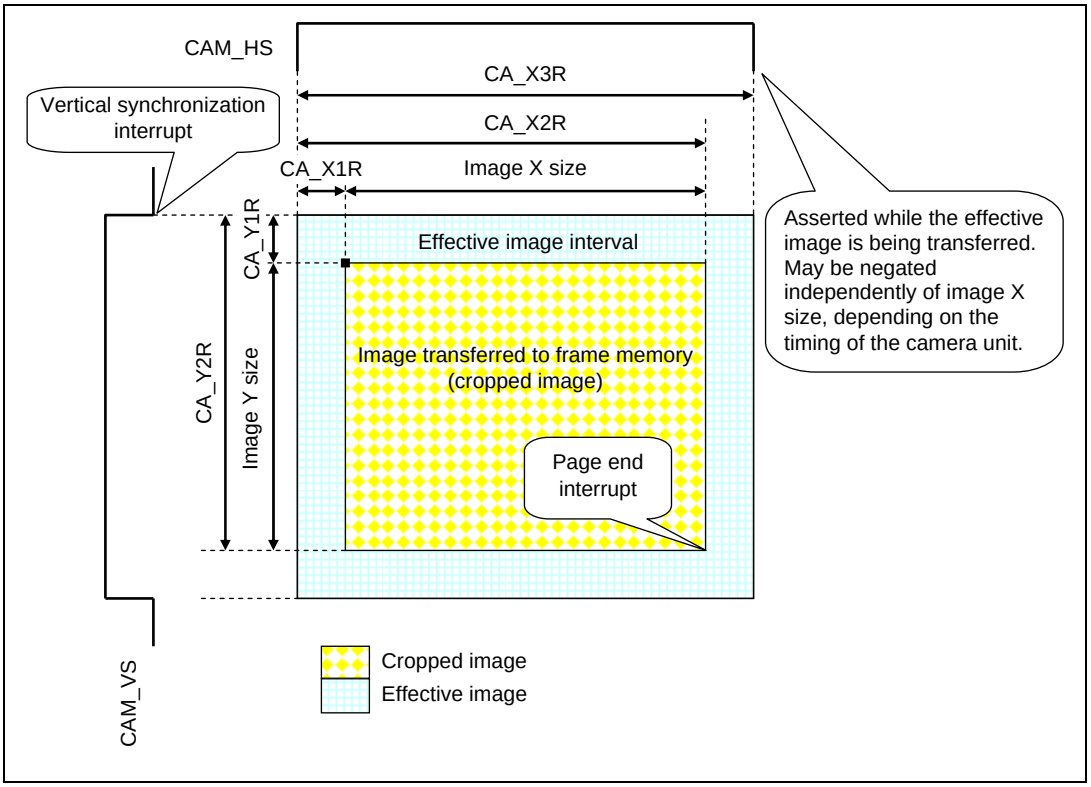
Register Name	Condition
CA_Y2R	CA_Y2R = Image Y size
CA_Y1R	CA_Y1R = 0
CA_X3R	CA_X3R = Image X size × 2 (rising or falling edge)
	CA_X3R = Image X size (rising and falling edges)
CA_X2R	CA_X2R = Image X size × 2 (rising or falling edge)
	CA_X2R = Image X size (rising and falling edges)
CA_X1R	CA_X1R = 0

Caution Be sure to set CA_X3R.

(2) Cropping

Any rectangle can be cropped from the effective image data input via the CAM interface and can be written to the frame memory.

Figure 4-18. Enable Signal Sampling (Cropping)



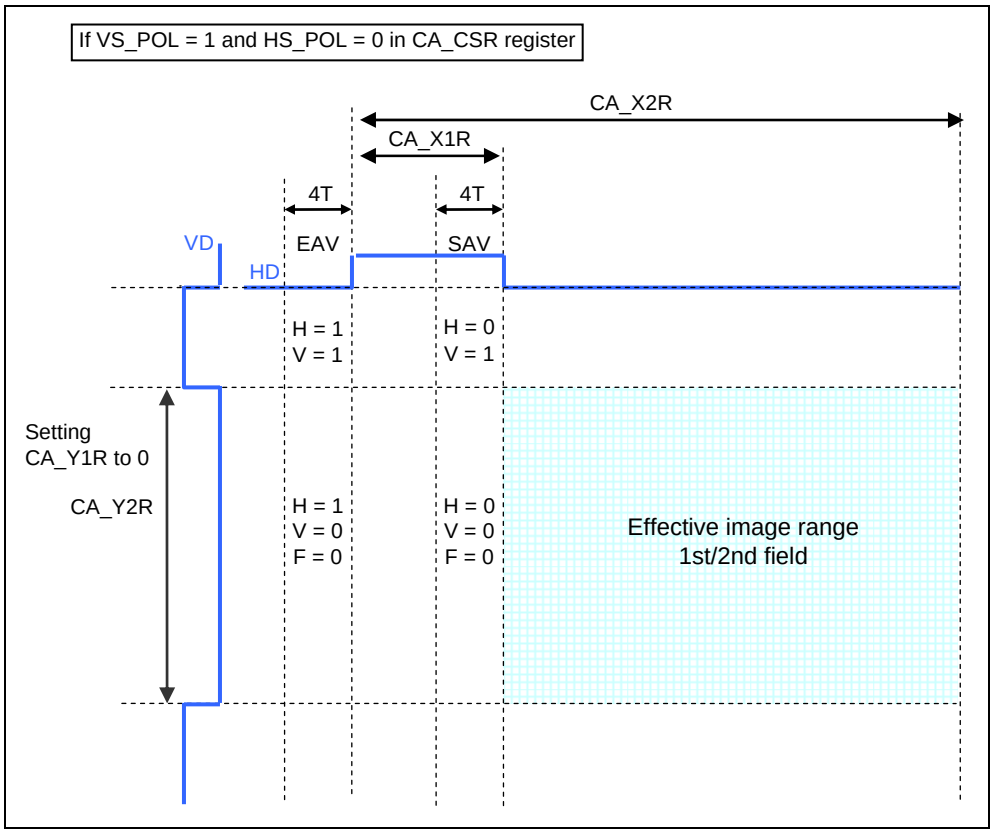
Set up the registers as follows.

Register Name	Condition
CA_Y2R	CA_Y2R = Cropped image Y size + CA_Y1R
CA_Y1R	CA_Y1R = Cropping starting line
CA_X3R	CA_X3R = Effective image X size × 2 (rising or falling edge)
	CA_X3R = Effective image X size (rising and falling edges)
CA_X2R	CA_X2R = Cropped image X size × 2 (rising or falling edge)
	CA_X2R = Cropped image X size (rising and falling edges)
CA_X1R	CA_X1R = Cropping starting pixel × 2 (rising or falling edge)
	CA_X1R = Cropping starting pixel (rising and falling edges)

Caution Be sure to set CA_X3R.

(3) ITU-R BT.656 signal sampling

Figure 4-19. Signal Sampling in ITU-R BT.656 Mode



To capture NTSC/PAL REC656 inputs, set VS_POL to 1 and HS_POL to 0 in the CA_CSR register, and specify the values shown in the following table for the effective image range setting registers.

Register	Register Values	
	NTSC	PAL
CA_Y2R	243	288
CA_Y1R	0	0
CA_X2R	1712	1724
CA_X1R	272	284

If values other than above need to be specified, follow the criterion shown on the following page.

It is recommended to set VS_POL to 1 and HS_POL to 0 in the CA_CSR register. Set CA_Y1R to 0, and then specify the effective image range by using the CA_X1R, CA_X2R, and CA_Y2R registers (see **Figure 4-19**).

Register	Condition
CA_Y2R	CA_Y2R = Image Y size + CA_Y1R CA_Y2R < Total number of lines in one frame/2[Note]
CA_Y1R	0 ≤ CA_Y1R (vertical blanking interval)
CA_X2R	CA_X2R = (Image X size × 2) + CA_X1R (rising or falling edge)
CA_X1R	0 ≤ CA_X1R (horizontal blanking interval)

Note The same values must be specified for the CA_Y1R, CA_Y2R, CA_X1R, and CA_X2R registers.
Cases where the image size in the 1st and 2nd fields differs are not supported.
The value set to CA_X3R is ignored.
If HS_POL is set to 1, add 1 to the values specified for the CA_Y1R and CA_Y2R registers while HS_POL is set to 0 and specify the obtained values for the CA_Y1R and CA_Y2R registers.

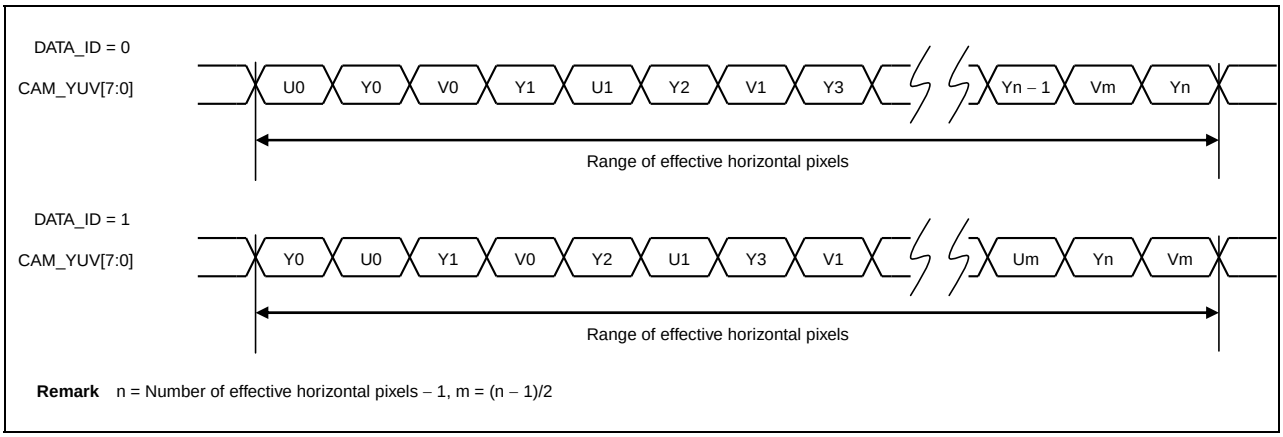
4.10 Data Format

4.10.1 Camera

Image data can be input from a camera in the two different orders, specified by setting the DATA_ID bit of the CA_CSR register.

Figure 4-20 shows the image data sequence when the DATA_ID bit is set to 0. Image data is output from a camera in the order of Y0, V, and Y1, starting with U0. If the DATA_ID bit is set to 1, image data is output from a camera in the order of U, Y1, and V, starting with Y0.

Figure 4-20. Camera Data Format



Remark n = Number of effective horizontal pixels – 1, m = (n – 1)/2

4.10.2 Memory mapping

(1) YUV420/422 Semi-Planar mode

Image data input from a camera is transferred to separate areas Y and UV in memory (these areas are respectively referred to as the Y plane and UV plane in the specification). Data is transferred to memory in 32-bit units. The endianess can be specified for the higher and lower 16 bits by setting the Y_UV_OD_ENDIAN bit of the CA_CSR register. The higher and lower bytes can be swapped. Figure 4-21 shows the memory format in big endian mode and Figure 4-22 shows the memory format in little endian mode.

Figure 4-21. Memory Format (Big Endian)

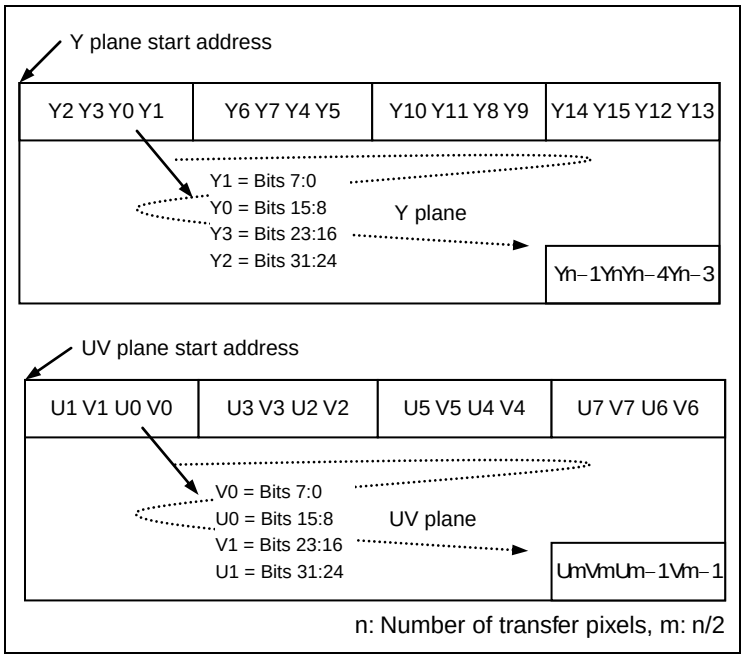
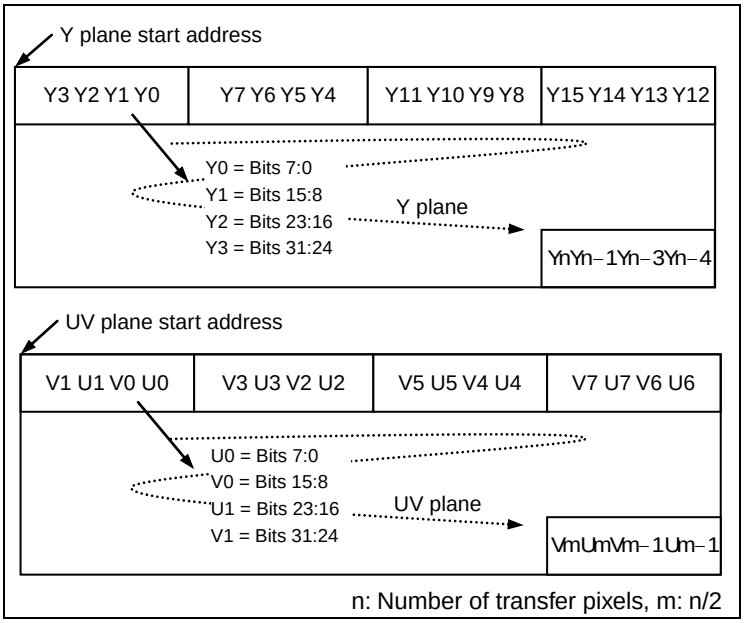


Figure 4-22. Memory Format (Little Endian)

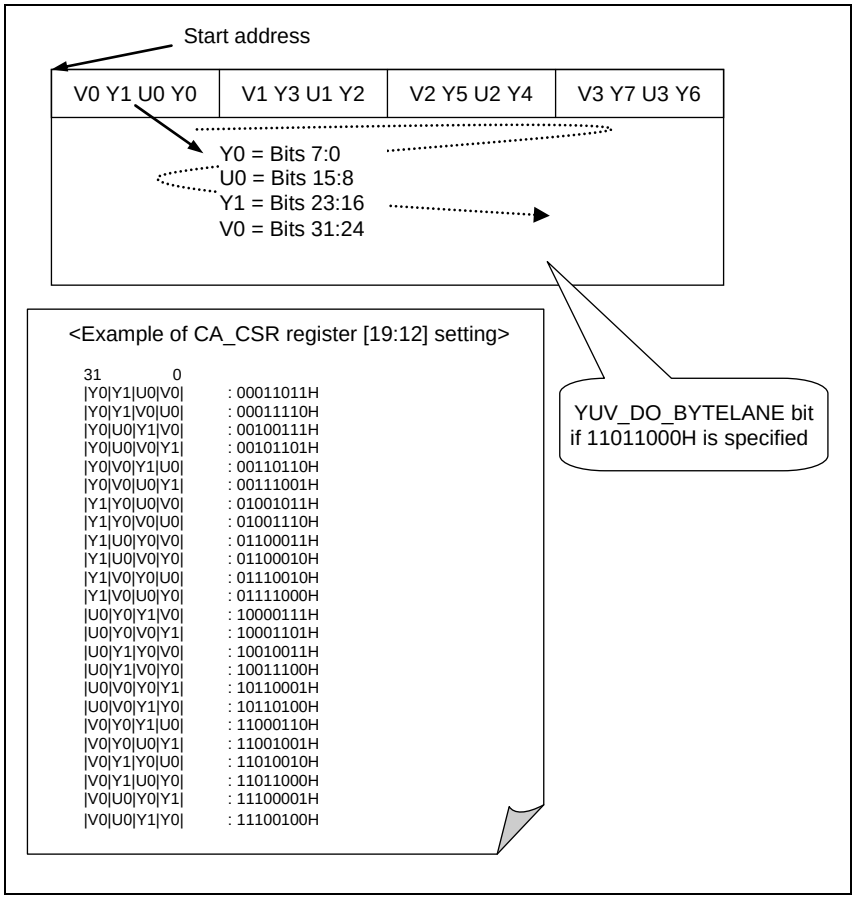


(2) YUV422 Interleave mode

In this mode, image data input from a camera is transferred to memory with Y0Y1U0V0 components (2 pixels) as a set. Data is transferred to memory in 32-bit units, and the output byte lane of each component can be specified by using the CA_OD_BYTELANE register. Figure 4-23 shows a setting example.

Specify the transfer address by using the CA_YPLANE_A/B registers (Y plane). Values specified by the CA_UVPLANE_A/B register (UV plane) are ignored.

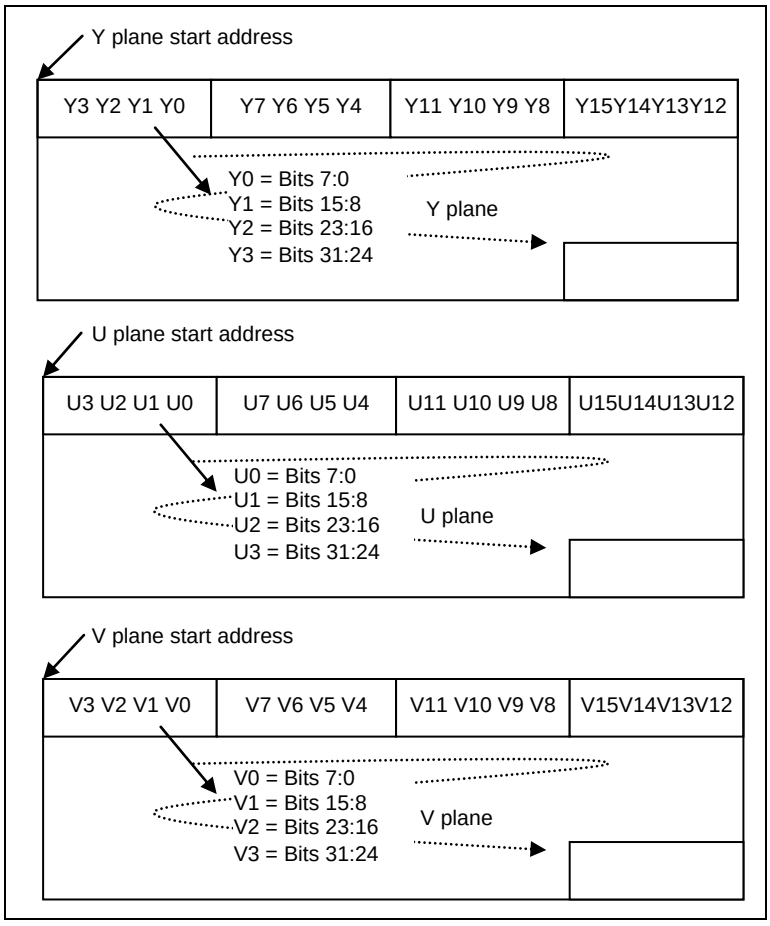
Figure 4-23. Example of YUV_OD_BYTELANE Setting



(3) YUV420/422 Planar mode

Image data input from a camera is transferred to separate areas Y, U, and V in memory (these areas are respectively referred to as the Y plane, U plane and V plane in the specification). Data is transferred to memory in 32-bit units, and the output byte lane of each component can be specified by using the CA_OD_BYTELANE2 register. Figure 4-24 shows the memory format.

Figure 4-24. YUV 420/422 Planar Memory Format

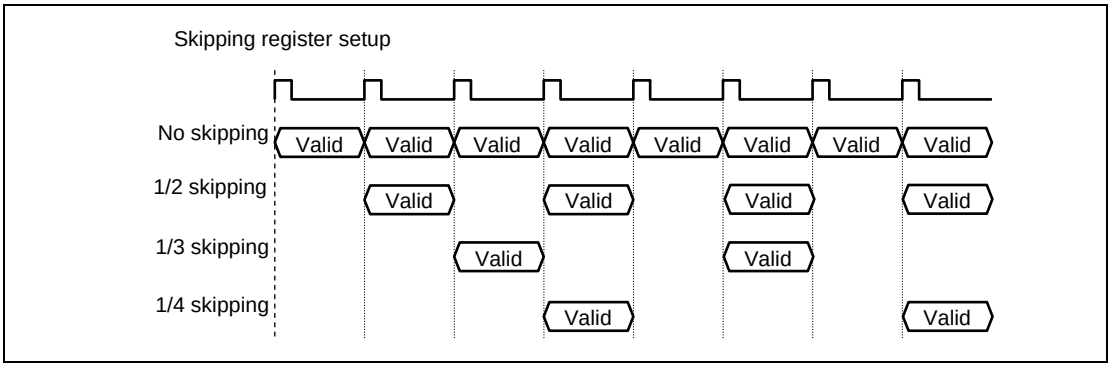


4.11 Transfer Processing

4.11.1 Frame skipping

The frame skipping bit of the transfer control register is used to set skipping of image data frames input from a camera. Figure 4-25 shows the relationship between skipping and effective transfer frames. Frame skipping is executed from the frame specified by the corresponding register.

Figure 4-25. Frame Skipping

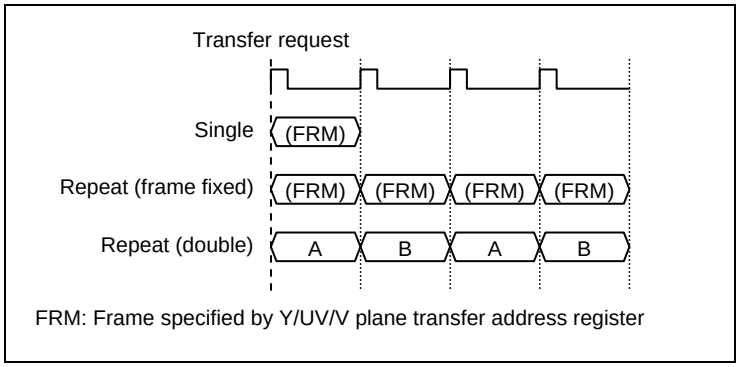


4.11.2 Transfer mode

The transfer mode bit of the transfer control register is used to specify the method of switching a transfer destination frame. Figure 4-26 shows the relationship between the transfer modes and the transfer destination frame. This figure shows the operations performed when no skipping is specified. If a skipping mode is specified, the transfer destination frame is switched for frames after skipping.

- Single transfer: Only one frame is transferred to a specified frame.
- Repeat transfer (frame fixed): Transfer to a specified frame is repeated.
- Repeat transfer (double): Transfer to the A and B frames is repeated alternately.

Figure 4-26. Transfer Mode



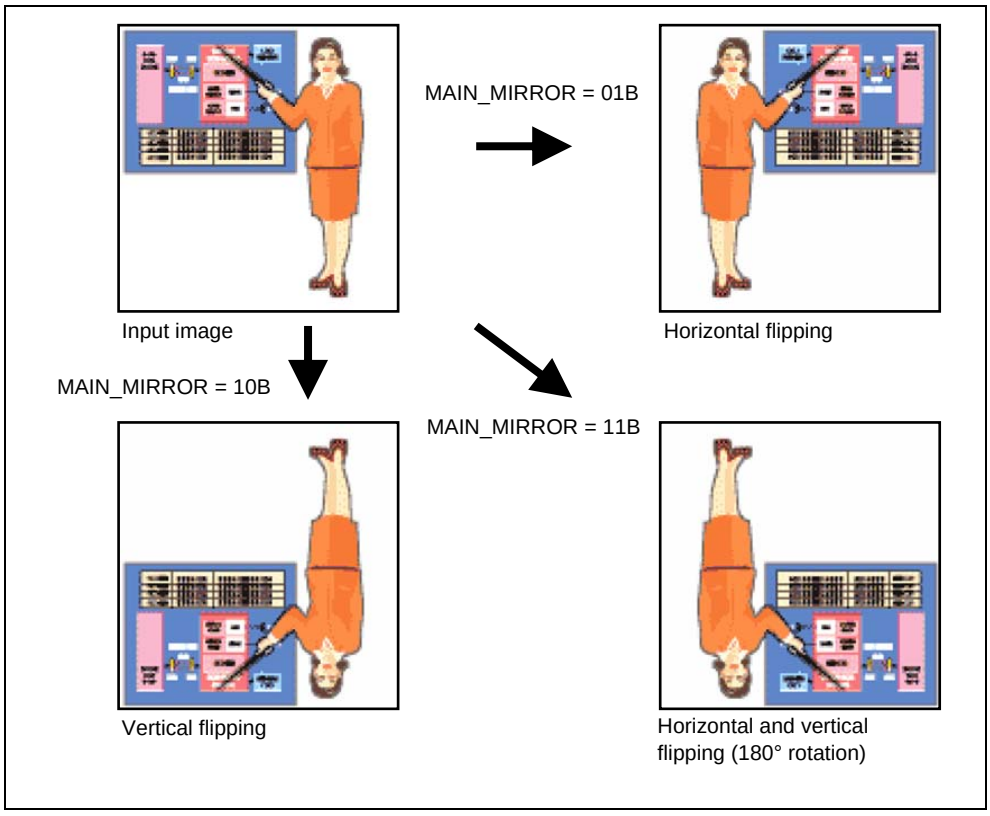
Caution When performing a repeat transfer (double), reset CAM immediately before transfer.

4.11.3 Horizontal/vertical flip control

The images can be flipped during DMA transfer by using the horizontal/vertical flip control register.

When flip control is performed, the frame memory area does not differ from the area used when flip control is not performed.

Figure 4-27. Flip Control



4.12 Frame Interval

The operation will not be performed correctly if the frame interval is too short. Make sure that the frame interval is sufficiently long.

If the register setting enable timing (CA_CSR) is the rising edge and if CAM_VS of the next frame will rise before transfer of one frame to the frame memory is completed, the register setting of the next frame at that point is enabled and the operation cannot be correctly performed.

Similarly, if the register setting enable timing (CA_CSR) is the falling edge, make sure that CAM_VS of the next frame does not fall before transfer of one frame to the frame memory is completed.

Figure 4-28. Frame Interval (Register Setting Enable Timing: Rising Edge)

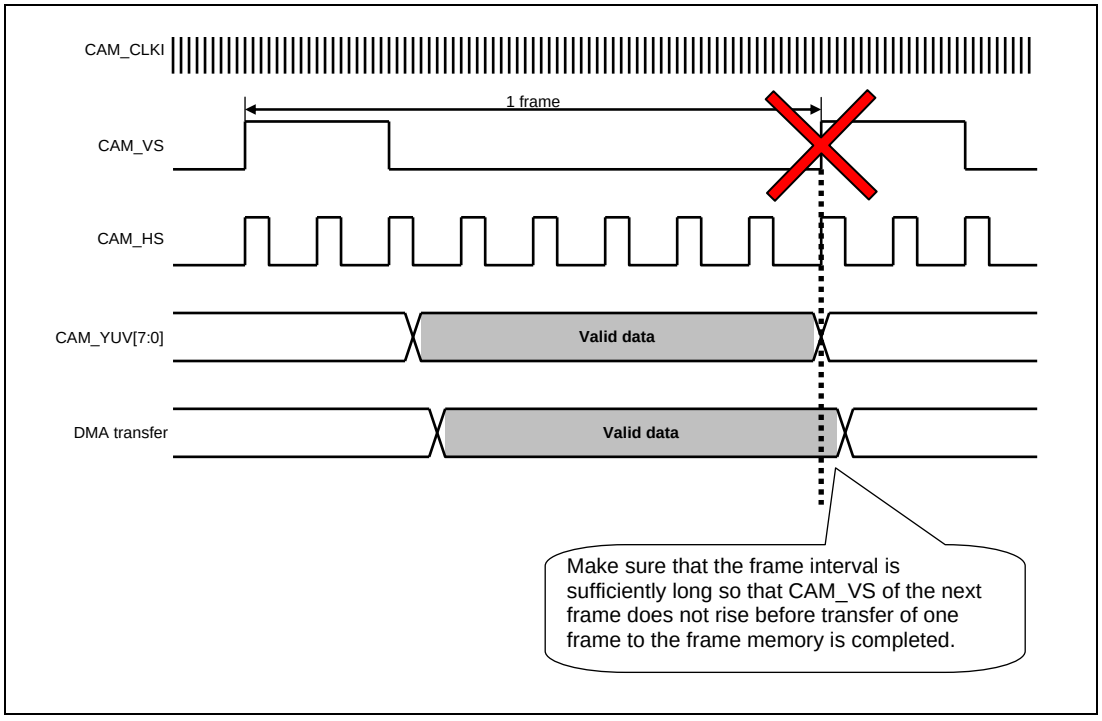
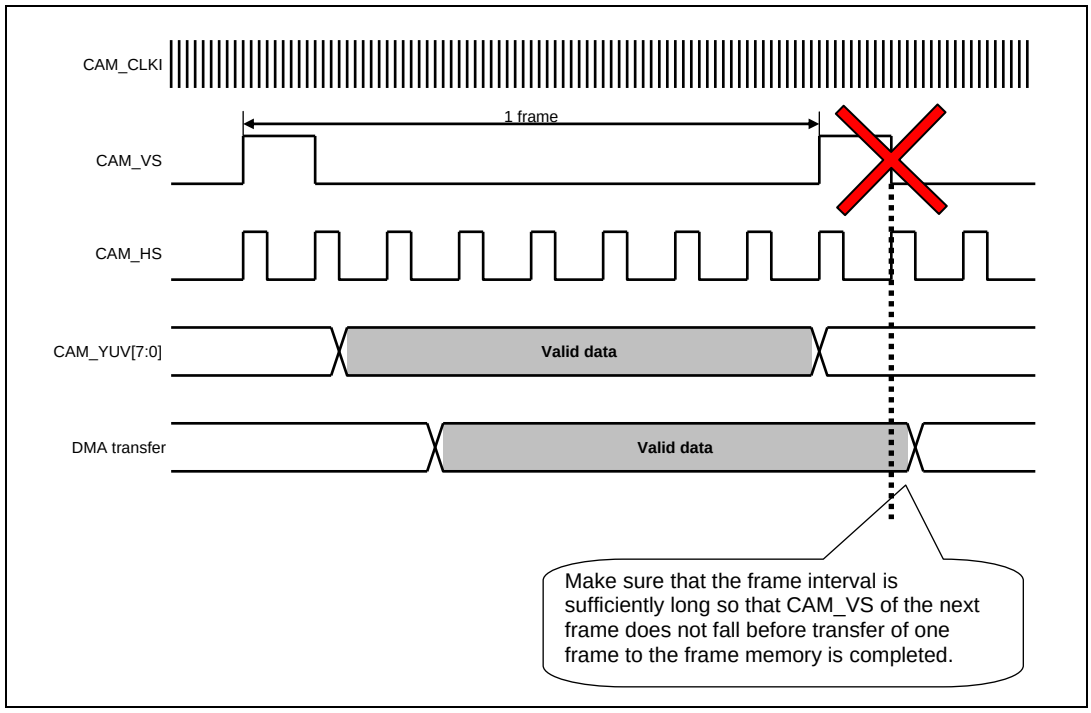


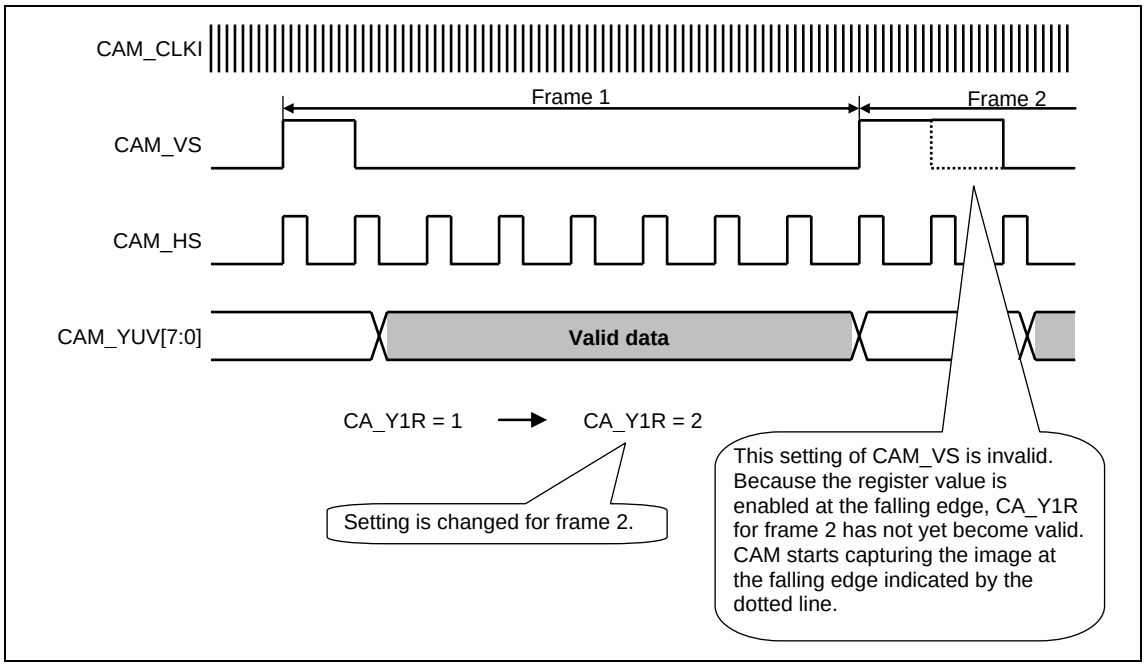
Figure 4-29. Frame Interval (Register Setting Enable Timing: Falling Edge)



4.13 Register Setting Enable Timing

If the register setting enable timing is the falling edge, note the values set to CA_X1R and CA_Y1R for the preceding frame. Depending on these values, the specified values may not become valid for the intended frame.

Figure 4-30. Register Setting Enable Timing: Falling Edge



CHAPTER 5 USAGE

5.1 Example of Setting Procedure

An example of operations from reset to image capturing is shown below.

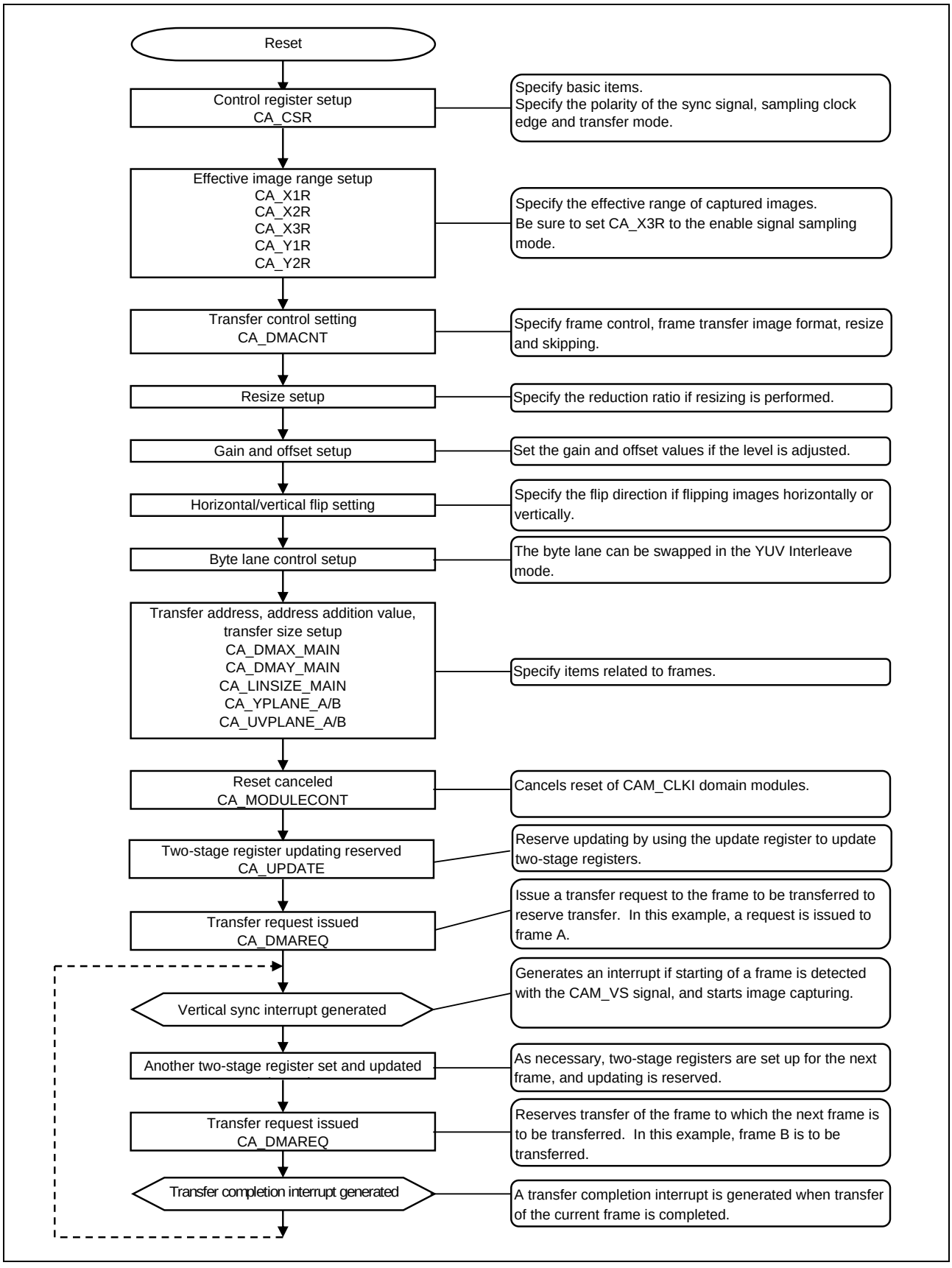
Be sure to satisfy the following timing conditions when releasing the reset state of the CAM_CLKI domain module; otherwise, the transfer request cannot be issued and thus transfer processing is not performed. Reset must be released:

<1> After completion of CA_CSR register setup.

<2> Before reservation of updating the two-stage register and before issuance of a transfer request.

To release masking of the vertical synchronization interrupt (CAM_VS_EN bit of CA_ENSET register), wait for at least 16 CAM_CLKI cycles after the reset state of the CAM_CLKI domain is released.

Figure 5-1. Example of Setting Procedure

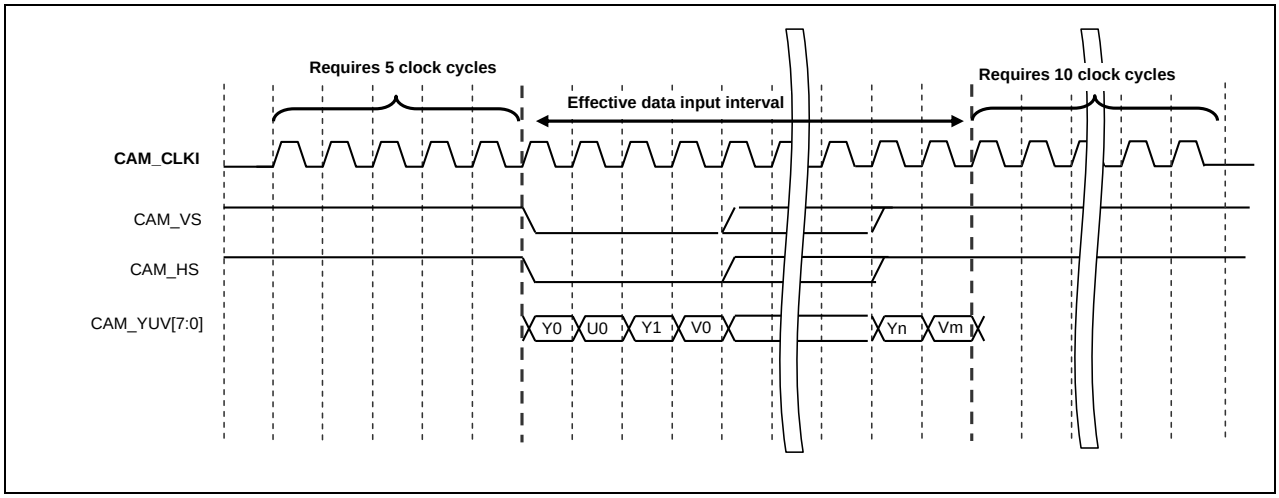


5.2 Restriction

There is a restriction regarding the timing of CAM_CLKI (the external clock), CAM_VS, CAM_HS, and CAMYUV[7:0] (input data).

CAM_CLKI must be supplied 5 clock cycles before effective data input and 10 clock cycles after effective data input. The former cycles are used to prepare for data capturing, and the latter cycles are used to pass the input data by using the AHB clock.

Figure 5-2. Relationship Between CAM_CLKI and Data



Revision History

Date	Revision	Comments
February 10, 2009	1.0	–
April 27, 2009	2.0	Incremental update from comments to the 1.0..

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