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RENESAS

User's Manual

Multimedia Processor for Mobile Applications

DMA Controller

EMMA Mobile1

Document No. S19255EJ3V0UM00 (3rd edition)
Date Published June 2009

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M8E 02. 11-1

PREFACE

Readers

This manual is intended for hardware/software application system designers who wish to understand and use the DMA controller functions of EMMA Mobile1 (EM1), a multimedia processor for mobile applications.

Purpose

This manual is intended to explain to users the hardware and software functions of the DMA controller of EM1, and be used as a reference material for developing hardware and software for systems that use EM1.

Organization

This manual consists of the following chapters.

- Chapter 1 Overview
- Chapter 2 Registers
- Chapter 3 Description of functions
- Chapter 4 Usage

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electricity, logic circuits, and microcontrollers.

To understand the functions of the DMA controller of EM1 in detail
→ Read this manual according to the **CONTENTS**.

To understand the other functions of EM1
→ Refer to the user's manual of the respective module.

To understand the electrical specifications of EM1
→ Refer to the Data Sheet.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH
Data type:	Word … 32 bits
	Halfword … 16 bits
	Byte … 8 bits

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name		Document No.
MC-10118A Data sheet		S19657E
μPD77630A Data Sheet		S19686E
User's manual	Audio/Voice and PWM Interfaces	S19253E
	DDR SDRAM Interface	S19254E
	DMA Controller	This manual
	I2C Interface	S19256E
	ITU-R BT.656 Interface	S19257E
	LCD Controller	S19258E
	MICROWIRE	S19259E
	NAND Flash Interface	S19260E
	SPI	S19261E
	UART Interface	S19262E
	Image Composer	S19263E
	Image Processor Unit	S19264E
	System Control/General-Purpose I/O Interface	S19265E
	Timer	S19266E
	Terrestrial Digital TV Interface	S19267E
	Camera Interface	S19285E
	USB Interface	S19359E
	SD Memory Card Interface	S19361E
	PDMA	S19373E
	One Chip (MC-10118A)	S19598E
	One Chip (μPD77630A)	S19687E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

CHAPTER 1 OVERVIEW

1.1 Overview

This document describes the DMA controller (DMAC) for EM1.

(1) Features

- Three physical channels (PCH0, PCH2, PCH3) and 26 logical channels (LCH) are incorporated. (PCH1 is a reserved channel).
  - PCH0 (LCH0 to LCH3): Memory-to-memory transfer
  - PCH2 (LCH0 to LCH14): Memory-to-peripheral transfer. (LCH6 to LCH8, and LCH11 are reserved.)
  - PCH3 (LCH0 to LCH14): Peripheral-to-memory transfer. (LCH6 to LCH8, and LCH11 are reserved.)
- Each physical channel (PCH) has one AHB bus master for reading and another AHB bus master for writing.
- Connected as an AHB master, to a total of six locations of internal bus slave interface (three locations for reading and another three locations for writing).
- The six AHB bus masters can operate concurrently.
- The DMAC internal registers are accessed via an APB. The APB can be accessed only in word units.
- PCH0 and PCH2 feature ring buffers in SRAM. PCH3 has a 16-entry FIFO (configured with FF).
  The size of the internal buffer of each physical channel is as follows.
  - PCH0: 256 words (256 bytes per LCH)
  - PCH2: 416 words (128 bytes per LCH)
  - PCH3: 16 words (4 bytes × 16 entries)
- Conforms to the AMBA™ system bus architecture (Rev. 2.0).
- Memory-to-peripheral transfer between the memory and PCM0 (executed by LCH9 of PCH2) uses PDMA or DMA exclusively for the same DMA channel (default: DMA). For details, see the **Multimedia Processor for Mobile Applications PDMA User's Manual**.

(2) Transfer operation

- The DMAC reads data from a source address (transfer source address), stores the data in the DMAC internal buffer, and writes that data to a destination address (transfer destination address).
- An interrupt signal is generated for each processor when transfer ends. (The four types of interrupt sources are available: length, block, error, and timeout.)
- Each AHB master has an arbitration circuit, which arbitrates among requests from the logical channels, using a round-robin algorithm.
- The DMAC operates at 166 MHz.
- The DMAC mainly performs the following two types of transfer.
  - Memory-to-memory transfer
  - Memory-to-peripheral transfer
- Both memory-to-memory AHB transfer and memory-to-peripheral AHB transfer support 8-, 16- and 32-bit bus width.
- Endian conversion. The read control block and write control block each have an endian conversion function. Byte lane of data loaded to a data buffer (FIFO) can be selected for each byte on the read side. Byte lane of data to be output to the AHB write bus can be selected for each byte on the write side.
- PCH0 supports reverse transfer in block units (implemented by setting the offset to the lower address direction).

CHAPTER 2 REGISTERS

2.1 Register Overview

The DMA controller registers are used to control transfers between memory and memory, and memory-to-peripheral and peripheral-to-memory transfers.

(1) Addresses of setting registers

Table 2-1. Address Assignment in Each Channel Parameter Setting Registers

Bits 15 to 12	Bits 11 to 8	Bits 7 to 0			
Physical Channels	Logical Channels	Register Functions			
				R/W	Bit Width
1: PCH0	0: LCH0	00:	Source address	R/W	32
3: PCH1 (Reserved)	1: LCH1	04:	Source address pointer	R	32
5: PCH2	2: LCH2	08:	Source address offset	R/W	16
7: PCH3	3: LCH3	0C:	Source block size (only available for PCH2)	R/W	16
	4: LCH4	10:	Source block count	R/W	4
	5: LCH5	20:	Destination address	R/W	32
	6: LCH6 (Reserved)	24:	Destination address pointer	R	32
	7: LCH7 (Reserved)	28:	Destination address offset	R/W	16
	8: LCH8 (Reserved)	2C:	Destination block size (only available for PCH3)	R/W	16
	9: LCH9	30:	Destination block count	R/W	4
	A: LCH10	40:	Length	R/W	24
	B: LCH11 (Reserved)	44:	Read length count	R	24
	C: LCH12	48:	Write length count	R	24
	D: LCH13	4C:	Block size (PCH0 only)	R/W	16
	E: LCH14	50:	Mode	R/W	–
		54:	Timer (only available for UART0 to UART2)	R/W	24
		58:	Timer count (only available for UART0 to UART2)	R	24

Table 2-2. Address Assignment in Each Channel Control and Interrupt Parameter Setting Registers

Bits 15 to 12	Bits 11 to 8	Bits 7 to 5	Bits 4 to 0		R/W	Bit Width
0: PCH0	0:	0:	00:	DMA control register	W	–
2: PCH1(Reserved)			04:	DMA status register	R	–
4: PCH2			08:	DMA end control register	W	–
6: PCH3	1: ACPU	0: LCH0 to LCH3	00:	Interrupt status	R	–
	4: ADSP	1: LCH4 to LCH7	04:	Interrupt raw status	R	
		2: LCH8 to LCH11	08:	Interrupt enable set	R/W	
		3: LCH12 to LCH15	0C:	Interrupt enable clear	R/W	
			10:	Interrupt source clear	W	
	8:	0:	00:	Interrupt output destination set	R/W	–

Table 2-3. Address Assignment in Other Setting Registers

Bits 15 to 8	Bits 7 to 0			
			R/W	Bit Width
80H:	00:	ACPU interrupt index	R	9
	04:	Reserved	R	9
	0C:	ADSP interrupt index	R	9
90H:	00:	ARM parameter register read switching	R/W	4
	08:	M2P parameter register read switching	R/W	15
	0C:	P2M parameter register read switching	R/W	15
91H:	00:	ARM parameter register forced update	W	4
	08:	M2P parameter register forced update	W	15
	0C:	P2M parameter register forced update	W	15

(2) Types of setting registers

The base address is 4009_0000H.

Table 2-4. DMAC Address Map Outline

(1/2)

Parameter	Address Range	Register Name
ACPU (PCH0)	0000H to 00FFH	ACPU control registers
	0100H to 0FFFH	ACPU interrupt registers
	1000H to 10FFH	ACPU LCH0 setting registers
	1100H to 11FFH	ACPU LCH1 setting registers
	1200H to 12FFH	ACPU LCH2 setting registers
	1300H to 13FFH	ACPU LCH3 setting registers
	1400H to 1FFFH	Reserved
M2P (PCH2)	4000H to 40FFH	M2P control registers
	4100H to 4FFFH	M2P interrupt registers
	5000H to 50FFH	M2P LCH0 setting registers
	5100H to 51FFH	M2P LCH1 setting registers

Table 2-4. DMAC Address Map Outline

(2/2)

Parameter	Address Range	Register Name
M2P (PCH2)	5200H to 52FFH	M2P LCH2 setting registers
	5300H to 53FFH	M2P LCH3 setting registers
	5400H to 54FFH	M2P LCH4 setting registers
	5500H to 55FFH	M2P LCH5 setting registers
	5600H to 56FFH	Reserved
	5700H to 57FFH	Reserved
	5800H to 58FFH	Reserved
	5900H to 59FFH	M2P LCH9 setting registers
	5A00H to 5AFFH	M2P LCH10 setting registers
	5B00H to 5BFFH	Reserved
	5C00H to 5CFFH	M2P LCH12 setting registers
	5D00H to 5DFFH	M2P LCH13 setting registers
	5E00H to 5EFFH	M2P LCH14 setting registers
	5F00H to 5FFFH	Reserved
P2M (PCH3)	6000H to 60FFH	P2M control registers
	6100H to 6FFFH	P2M interrupt registers
	7000H to 70FFH	P2M LCH0 setting registers
	7100H to 71FFH	P2M LCH1 setting registers
	7200H to 72FFH	P2M LCH2 setting registers
	7300H to 73FFH	P2M LCH3 setting registers
	7400H to 74FFH	P2M LCH4 setting registers
	7500H to 75FFH	P2M LCH5 setting registers
	7600H to 76FFH	Reserved
	7700H to 77FFH	Reserved
	7800H to 78FFH	Reserved
	7900H to 79FFH	P2M LCH9 setting registers
	7A00H to 7AFFH	P2M LCH10 setting registers
	7B00H to 7BFFH	Reserved
	7C00H to 7CFFH	P2M LCH12 setting registers
	7D00H to 7DFFH	P2M LCH13 setting registers
	7E00H to 7EFFH	P2M LCH14 setting registers
	7F00H to 7FFFH	Reserved
Interrupt index	8000H to 8FFFH	Interrupt index registers
Common to DMA controller	9000H to 9FFFH	Common register

2.2 Registers

Do not access reserved registers. An undefined value is returned for a read access.
Do not write any value other than 0 to reserved bits in each register.

2.2.1 ACPU registers

(1) ACPU DMA control registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
0000H	ACPU DMA start control register	DMA_ARM_CONT	W	0000_0000H
0004H	ACPU DMA control status register	DMA_ARM_CONTSTATUS	R	0000_0000H
0008H	ACPU DMA end control register	DMA_ARM_END	W	0000_0000H
000CH to 00FCH	Reserved	–	–	–

(2) ACPU and ADSP interrupt parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
0800H	ARM/DSP interrupt output destination setting register (LCH0 to LCH3)	DMA_ARM_LCH0LCH3_INT_SEL	R/W	0000_0000H
0804H to 0FFCH	Reserved	–	–	–
0100H	ACPU interrupt status register (LCH0 to LCH3)	DMA_ARM_PE0_LCH0LCH3_INT_CONT	R	0000_0000H
0104H	ACPU interrupt raw status register (LCH0 to LCH3)	DMA_ARM_PE0_LCH0LCH3_INT_RAW	R	0000_0000H
0108H	ACPU interrupt enable set register (LCH0 to LCH3)	DMA_ARM_PE0_LCH0LCH3_INT_ENABLE	R/W	0000_0000H
010CH	ACPU interrupt enable clear register (LCH0 to LCH3)	DMA_ARM_PE0_LCH0LCH3_INT_ENABLE_CL	W	0000_0000H
0110H	ACPU interrupt source clear register (LCH0 to LCH3)	DMA_ARM_PE0_LCH0LCH3_INT_REQ_CL	W	0000_0000H
0114H to 03FCH	Reserved	–	–	–
0400H	DSP interrupt status register (LCH0 to LCH3)	DMA_ARM_DSP_LCH0LCH3_INT_CONT	R	0000_0000H
0404H	DSP interrupt raw status register (LCH0 to LCH3)	DMA_ARM_DSP_LCH0LCH3_INT_RAW	R	0000_0000H
0408H	DSP interrupt enable set register (LCH0 to LCH3)	DMA_ARM_DSP_LCH0LCH3_INT_ENABLE	R/W	0000_0000H
040CH	DSP interrupt enable clear register (LCH0 to LCH3)	DMA_ARM_DSP_LCH0LCH3_INT_ENABLE_CL	W	0000_0000H
0410H	DSP interrupt source clear register (LCH0 to LCH3)	DMA_ARM_DSP_LCH0LCH3_INT_REQ_CL	W	0000_0000H
0414H to 07FCH	Reserved	–	–	–

(3) ACPU LCH0 parameter setting registers (memory-to-memory)

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
1000H	ACPU LCH0 source address register (start address)	DMA_ARM_LCH0_AADD	R/W	0000_0000H
1004H	ACPU LCH0 source address pointer register	DMA_ARM_LCH0_AADP	R	0000_0000H
1008H	ACPU LCH0 source address offset register	DMA_ARM_LCH0_AOFF	R/W	0000_0000H
100CH	Reserved	–	–	–
1010H	ACPU LCH0 source block count register	DMA_ARM_LCH0_ASIZE_ COUNT	R/W	0000_0000H
1014H to 101CH	Reserved	–	–	–
1020H	ACPU LCH0 destination address register (start address)	DMA_ARM_LCH0_BADD	R/W	0000_0000H
1024H	ACPU LCH0 destination address pointer register	DMA_ARM_LCH0_BADP	R	0000_0000H
1028H	ACPU LCH0 destination address offset register	DMA_ARM_LCH0_BOFF	R/W	0000_0000H
102CH	Reserved	–	–	–
1030H	ACPU LCH0 destination block count register	DMA_ARM_LCH0_BSIZE_ COUNT	R/W	0000_0000H
1034H to 103CH	Reserved	–	–	–
1040H	ACPU LCH0 length register	DMA_ARM_LCH0_LENG	R/W	0000_0000H
1044H	ACPU LCH0 read length count register	DMA_ARM_LCH0_LENG_ RCOUNT	R	0000_0000H
1048H	ACPU LCH0 write length count register	DMA_ARM_LCH0_LENG_ WCOUNT	R	0000_0000H
104CH	ACPU LCH0 block size register	DMA_ARM_LCH0_SIZE	R/W	0000_0000H
1050H	ACPU LCH0 mode register (read/write endian, repeat)	DMA_ARM_LCH0_MODE	R/W	E4E4_0000H
1054H to 10FCH	Reserved	–	–	–

(4) ACPU LCH1 parameter setting registers (memory-to-memory)

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
1100H	ACPU LCH1 source address register (start address)	DMA_ARM_LCH1_AADD	R/W	0000_0000H
1104H	ACPU LCH1 source address pointer register	DMA_ARM_LCH1_AADP	R	0000_0000H
1108H	ACPU LCH1 source address offset register	DMA_ARM_LCH1_AOFF	R/W	0000_0000H
110CH	Reserved	–	–	–
1110H	ACPU LCH1 source block count register	DMA_ARM_LCH1_ASIZE_COUNT	R/W	0000_0000H
1114H to 111CH	Reserved	–	–	–
1120H	ACPU LCH1 destination address register (start address)	DMA_ARM_LCH1_BADD	R/W	0000_0000H
1124H	ACPU LCH1 destination address pointer register	DMA_ARM_LCH1_BADP	R	0000_0000H
1128H	ACPU LCH1 destination address offset register	DMA_ARM_LCH1_BOFF	R/W	0000_0000H
112CH	Reserved	–	–	–
1130H	ACPU LCH1 destination block count register	DMA_ARM_LCH1_BSIZE_COUNT	R/W	0000_0000H
1134H to 113CH	Reserved	–	–	–
1140H	ACPU LCH1 length register	DMA_ARM_LCH1_LENG	R/W	0000_0000H
1144H	ACPU LCH1 read length count register	DMA_ARM_LCH1_LENG_RCOUNT	R	0000_0000H
1148H	ACPU LCH1 write length count register	DMA_ARM_LCH1_LENG_WCOUNT	R	0000_0000H
114CH	ACPU LCH1 block size register	DMA_ARM_LCH1_SIZE	R/W	0000_0000H
1150H	ACPU LCH1 mode register (read/write endian, repeat)	DMA_ARM_LCH1_MODE	R/W	E4E4_0000H
1154H to 11FCH	Reserved	–	–	–

(5) ACPU LCH2 parameter setting registers (memory-to-memory)

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
1200H	ACPU LCH2 source address register (start address)	DMA_ARM_LCH2_AADD	R/W	0000_0000H
1204H	ACPU LCH2 source address pointer register	DMA_ARM_LCH2_AADP	R	0000_0000H
1208H	ACPU LCH2 source address offset register	DMA_ARM_LCH2_AOFF	R/W	0000_0000H
120CH	Reserved	–	–	–
1210H	ACPU LCH2 source block count register	DMA_ARM_LCH2_ASIZE_ COUNT	R/W	0000_0000H
1214H to 121CH	Reserved	–	–	–
1220H	ACPU LCH2 destination address register (start address)	DMA_ARM_LCH2_BADD	R/W	0000_0000H
1224H	ACPU LCH2 destination address pointer register	DMA_ARM_LCH2_BADP	R	0000_0000H
1228H	ACPU LCH2 destination address offset register	DMA_ARM_LCH2_BOFF	R/W	0000_0000H
122CH	Reserved	–	–	–
1230H	ACPU LCH2 destination block count register	DMA_ARM_LCH2_BSIZE_ COUNT	R/W	0000_0000H
1234H to 123CH	Reserved	–	–	–
1240H	ACPU LCH2 length register	DMA_ARM_LCH2_LENG	R/W	0000_0000H
1244H	ACPU LCH2 read length count register	DMA_ARM_LCH2_LENG_ RCOUNT	R	0000_0000H
1248H	ACPU LCH2 write length count register	DMA_ARM_LCH2_LENG_ WCOUNT	R	0000_0000H
124CH	ACPU LCH2 block size register	DMA_ARM_LCH2_SIZE	R/W	0000_0000H
1250H	ACPU LCH2 mode register (read/write endian, repeat)	DMA_ARM_LCH2_MODE	R/W	E4E4_0000H
1254H to 12FCH	Reserved	–	–	–

(6) ACPU LCH3 parameter setting registers (memory-to-memory)

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
1300H	ACPU LCH3 source address register (start address)	DMA_ARM_LCH3_AADD	R/W	0000_0000H
1304H	ACPU LCH3 source address pointer register	DMA_ARM_LCH3_AADP	R	0000_0000H
1308H	ACPU LCH3 source address offset register	DMA_ARM_LCH3_AOFF	R/W	0000_0000H
130CH	Reserved	–	–	–
1310H	ACPU LCH3 source block count register	DMA_ARM_LCH3_ASIZE_COUNT	R/W	0000_0000H
1314H to 131CH	Reserved	–	–	–
1320H	ACPU LCH3 destination address register (start address)	DMA_ARM_LCH3_BADD	R/W	0000_0000H
1324H	ACPU LCH3 destination address pointer register	DMA_ARM_LCH3_BADP	R	0000_0000H
1328H	ACPU LCH3 destination address offset register	DMA_ARM_LCH3_BOFF	R/W	0000_0000H
132CH	Reserved	–	–	–
1330H	ACPU LCH3 destination block count register	DMA_ARM_LCH3_BSIZE_COUNT	R/W	0000_0000H
1334H to 133CH	Reserved	–	–	–
1340H	ACPU LCH3 length register	DMA_ARM_LCH3_LENG	R/W	0000_0000H
1344H	ACPU LCH3 read length count register	DMA_ARM_LCH3_LENG_RCOUNT	R	0000_0000H
1348H	ACPU LCH3 write length count register	DMA_ARM_LCH3_LENG_WCOUNT	R	0000_0000H
134CH	ACPU LCH3 block size register	DMA_ARM_LCH3_SIZE	R/W	0000_0000H
1350H	ACPU LCH3 mode register (read endian, repeat)	DMA_ARM_LCH3_MODE	R/W	E4E4_0000H
1354H to 13FCH	Reserved	–	–	–

2.2.2 M2P (memory-to-peripheral transfer) registers

Caution LCH6 and LCH8 are reserved channels, so there are no corresponding register bits.

(1) M2P DMA control registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
4000H	M2P DMA start control register	DMA_M2P_CONT	W	0000_0000H
4004H	M2P DMA control status register	DMA_M2P_CONTSTATUS	R	0000_0000H
4008H	M2P DMA end control register	DMA_M2P_END	W	0000_0000H
400CH to 40FCH	Reserved	–	–	–

(2) M2P interrupt parameter setting registers

Base address: 4009_0000H

(1/3)

Address	Register Name	Symbol	R/W	After Reset
4800H	M2P interrupt output destination setting register (LCH0 to LCH14)	DMA_M2P_LCH0LCH14_INT_SEL	R/W	0000_0000H
4804H to 4FFCH	Reserved	–	–	–
4100H	ACPU interrupt status register (LCH0 to LCH3)	DMA_M2P_PE0_LCH0LCH3_INT_CONT	R	0000_0000H
4104H	ACPU interrupt raw status register (LCH0 to LCH3)	DMA_M2P_PE0_LCH0LCH3_INT_RAW	R	0000_0000H
4108H	ACPU interrupt enable set register (LCH0 to LCH3)	DMA_M2P_PE0_LCH0LCH3_INT_ENABLE	R/W	0000_0000H
410CH	ACPU interrupt enable clear register (LCH0 to LCH3)	DMA_M2P_PE0_LCH0LCH3_INT_ENABLE_CL	W	0000_0000H
4110H	ACPU interrupt source clear register (LCH0 to LCH3)	DMA_M2P_PE0_LCH0LCH3_INT_REQ_CL	W	0000_0000H
4114H to 411CH	Reserved	–	–	–
4120H	ACPU interrupt status register (LCH4 to LCH5)	DMA_M2P_PE0_LCH4LCH5_INT_CONT	R	0000_0000H
4124H	ACPU interrupt raw status register (LCH4 to LCH5)	DMA_M2P_PE0_LCH4LCH5_INT_RAW	R	0000_0000H
4128H	ACPU interrupt enable set register (LCH4 to LCH5)	DMA_M2P_PE0_LCH4LCH5_INT_ENABLE	R/W	0000_0000H
412CH	ACPU interrupt enable clear register (LCH4 to LCH5)	DMA_M2P_PE0_LCH4LCH5_INT_ENABLE_CL	W	0000_0000H
4130H	ACPU interrupt source clear register (LCH4 to LCH5)	DMA_M2P_PE0_LCH4LCH5_INT_REQ_CL	W	0000_0000H
4134H to 413CH	Reserved	–	–	–

(2/3)

Address	Register Name	Symbol	R/W	After Reset
4140H	ACPU interrupt status register (LCH9 to LCH10)	DMA_M2P_PE0_LCH9LCH10_INT_CONT	R	0000_0000H
4144H	ACPU interrupt raw status register (LCH9 to LCH10)	DMA_M2P_PE0_LCH9LCH10_INT_RAW	R	0000_0000H
4148H	ACPU interrupt enable set register (LCH9 to LCH10)	DMA_M2P_PE0_LCH9LCH10_INT_ENABLE	R/W	0000_0000H
414CH	ACPU interrupt enable clear register (LCH9 to LCH10)	DMA_M2P_PE0_LCH9LCH10_INT_ENABLE_CL	W	0000_0000H
4150H	ACPU interrupt source clear register (LCH9 to LCH10)	DMA_M2P_PE0_LCH9LCH10_INT_REQ_CL	W	0000_0000H
4154H to 415CH	Reserved	–	–	–
4160H	ACPU interrupt status register (LCH12 to LCH14)	DMA_M2P_PE0_LCH12LCH14_INT_CONT	R	0000_0000H
4164H	ACPU interrupt raw status register (LCH12 to LCH14)	DMA_M2P_PE0_LCH12LCH14_INT_RAW	R	0000_0000H
4168H	ACPU interrupt enable set register (LCH12 to LCH14)	DMA_M2P_PE0_LCH12LCH14_INT_ENABLE	R/W	0000_0000H
416CH	ACPU interrupt enable clear register (LCH12 to LCH14)	DMA_M2P_PE0_LCH12LCH14_INT_ENABLE_CL	W	0000_0000H
4170H	ACPU interrupt source clear register (LCH12 to LCH14)	DMA_M2P_PE0_LCH12LCH14_INT_REQ_CL	W	0000_0000H
4174H to 43FCH	Reserved	–	–	–
4400H	DSP interrupt status register (LCH0 to LCH3)	DMA_M2P_DSP_LCH0LCH3_INT_CONT	R	0000_0000H
4404H	DSP interrupt raw status register (LCH0 to LCH3)	DMA_M2P_DSP_LCH0LCH3_INT_RAW	R	0000_0000H
4408H	DSP interrupt enable set register (LCH0 to LCH3)	DMA_M2P_DSP_LCH0LCH3_INT_ENABLE	R/W	0000_0000H
440CH	DSP interrupt enable clear register (LCH0 to LCH3)	DMA_M2P_DSP_LCH0LCH3_INT_ENABLE_CL	W	0000_0000H
4410H	DSP interrupt source clear register (LCH0 to LCH3)	DMA_M2P_DSP_LCH0LCH3_INT_REQ_CL	W	0000_0000H
4414H to 441CH	Reserved	–	–	–
4420H	DSP interrupt status register (LCH4 to LCH5)	DMA_M2P_DSP_LCH4LCH5_INT_CONT	R	0000_0000H
4424H	DSP interrupt raw status register (LCH4 to LCH5)	DMA_M2P_DSP_LCH4LCH5_INT_RAW	R	0000_0000H
4428H	DSP interrupt enable set register (LCH4 to LCH5)	DMA_M2P_DSP_LCH4LCH5_INT_ENABLE	R/W	0000_0000H
442CH	DSP interrupt enable clear register (LCH4 to LCH5)	DMA_M2P_DSP_LCH4LCH5_INT_ENABLE_CL	W	0000_0000H

(3/3)

Address	Register Name	Symbol	R/W	After Reset
4430H	DSP interrupt source clear register (LCH4 to LCH5)	DMA_M2P_DSP_LCH4LCH5_INT_REQ_CL	W	0000_0000H
4434H to 443CH	Reserved	–	–	–
4440H	DSP interrupt status register (LCH9 to LCH10)	DMA_M2P_DSP_LCH9LCH10_INT_CONT	R	0000_0000H
4444H	DSP interrupt raw status register (LCH9 to LCH10)	DMA_M2P_DSP_LCH9LCH10_INT_RAW	R	0000_0000H
4448H	DSP interrupt enable set register (LCH9 to LCH10)	DMA_M2P_DSP_LCH9LCH10_INT_ENABLE	R/W	0000_0000H
444CH	DSP interrupt enable clear register (LCH9 to LCH10)	DMA_M2P_DSP_LCH9LCH10_INT_ENABLE_CL	W	0000_0000H
4450H	DSP interrupt source clear register (LCH9 to LCH10)	DMA_M2P_DSP_LCH9LCH10_INT_REQ_CL	W	0000_0000H
4454H to 445CH	Reserved	–	–	–
4460H	DSP interrupt status register (LCH12 to LCH14)	DMA_M2P_DSP_LCH12LCH14_INT_CONT	R	0000_0000H
4464H	DSP interrupt raw status register (LCH12 to LCH14)	DMA_M2P_DSP_LCH12LCH14_INT_RAW	R	0000_0000H
4468H	DSP interrupt enable set register (LCH12 to LCH14)	DMA_M2P_DSP_LCH12LCH14_INT_ENABLE	R/W	0000_0000H
446CH	DSP interrupt enable clear register (LCH12 to LCH14)	DMA_M2P_DSP_LCH12LCH14_INT_ENABLE_CL	W	0000_0000H
4470H	DSP interrupt source clear register (LCH12 to LCH14)	DMA_M2P_DSP_LCH12LCH14_INT_REQ_CL	W	0000_0000H
4474H to 47FCH	Reserved	–	–	–

(3) M2P LCH0 parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
5000H	M2P LCH0 source address register (start address)	DMA_M2P_LCH0_AADD	R/W	0000_0000H
5004H	M2P LCH0 source address pointer register	DMA_M2P_LCH0_AADP	R	0000_0000H
5008H	M2P LCH0 source address offset register	DMA_M2P_LCH0_AOFF	R/W	0000_0000H
500CH	M2P LCH0 source block size register	DMA_M2P_LCH0_ASIZE	R/W	0000_0000H
5010H	M2P LCH0 source block count register	DMA_M2P_LCH0_ASIZE_COUNT	R/W	0000_0000H
5014H to 501CH	Reserved	–	–	–
5020H	M2P LCH0 destination address register	DMA_M2P_LCH0_BADD	R/W	0000_0000H
5024H to 503CH	Reserved	–	–	–
5040H	M2P LCH0 length register	DMA_M2P_LCH0_LENG	R/W	0000_0000H
5044H	M2P LCH0 read length count register	DMA_M2P_LCH0_LENG_RCOUNT	R	0000_0000H
5048H	M2P LCH0 write length count register	DMA_M2P_LCH0_LENG_WCOUNT	R	0000_0000H
504CH	Reserved	–	–	–
5050H	M2P LCH0 mode register (timer setting, bit width, read/write endian, repeat)	DMA_M2P_LCH0_MODE	R/W	E4E4_0000H
5054H	M2P LCH0 timer register	DMA_M2P_LCH0_TIME	R/W	0000_0000H
5058H	M2P LCH0 timer count register	DMA_M2P_LCH0_TIME_COUNT	R	0000_0000H
505CH to 50FCH	Reserved	–	–	–

Remark Set a memory address on the source side and a peripheral address on the destination side.

(4) M2P LCH1 parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
5100H	M2P LCH1 source address register (start address)	DMA_M2P_LCH1_AADD	R/W	0000_0000H
5104H	M2P LCH1 source address pointer register	DMA_M2P_LCH1_AADP	R	0000_0000H
5108H	M2P LCH1 source address offset register	DMA_M2P_LCH1_AOFF	R/W	0000_0000H
510CH	M2P LCH1 source block size register	DMA_M2P_LCH1_ASIZE	R/W	0000_0000H
5110H	M2P LCH1 source block count register	DMA_M2P_LCH1_ASIZE_COUNT	R/W	0000_0000H
5114H to 511CH	Reserved	–	–	–
5120H	M2P LCH1 destination address register	DMA_M2P_LCH1_BADD	R/W	0000_0000H
5124H to 513CH	Reserved	–	–	–
5140H	M2P LCH1 length register	DMA_M2P_LCH1_LENG	R/W	0000_0000H
5144H	M2P LCH1 read length count register	DMA_M2P_LCH1_LENG_RCOUNT	R	0000_0000H
5148H	M2P LCH1 write length count register	DMA_M2P_LCH1_LENG_WCOUNT	R	0000_0000H
514CH	Reserved	–	–	–
5150H	M2P LCH1 mode register (timer setting, bit width, read/write endian, repeat)	DMA_M2P_LCH1_MODE	R/W	E4E4_0000H
5154H	M2P LCH1 timer register	DMA_M2P_LCH1_TIME	R/W	0000_0000H
5158H	M2P LCH1 timer count register	DMA_M2P_LCH1_TIME_COUNT	R	0000_0000H
515CH to 51FCH	Reserved	–	–	–

Remark Set a memory address on the source side and a peripheral address on the destination side.

(5) M2P LCH2 parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
5200H	M2P LCH2 source address register (start address)	DMA_M2P_LCH2_AADD	R/W	0000_0000H
5204H	M2P LCH2 source address pointer register	DMA_M2P_LCH2_AADP	R	0000_0000H
5208H	M2P LCH2 source address offset register	DMA_M2P_LCH2_AOFF	R/W	0000_0000H
520CH	M2P LCH2 source block size register	DMA_M2P_LCH2_ASIZE	R/W	0000_0000H
5210H	M2P LCH2 source block count register	DMA_M2P_LCH2_ASIZE_ COUNT	R/W	0000_0000H
5214H to 521CH	Reserved	–	–	–
5220H	M2P LCH2 destination address register	DMA_M2P_LCH2_BADD	R/W	0000_0000H
5224H to 523CH	Reserved	–	–	–
5240H	M2P LCH2 length register	DMA_M2P_LCH2_LENG	R/W	0000_0000H
5244H	M2P LCH2 read length count register	DMA_M2P_LCH2_LENG_ RCOUNT	R	0000_0000H
5248H	M2P LCH2 write length count register	DMA_M2P_LCH2_LENG_ WCOUNT	R	0000_0000H
524CH	Reserved	–	–	–
5250H	M2P LCH2 mode register (timer setting, bit width, read/write endian, repeat)	DMA_M2P_LCH2_MODE	R/W	E4E4_0000H
5254H	M2P LCH2 timer register	DMA_M2P_LCH2_TIME	R/W	0000_0000H
5258H	M2P LCH2 timer count register	DMA_M2P_LCH2_TIME_ COUNT	R	0000_0000H
525CH to 52FCH	Reserved	–	–	–

Remark Set a memory address on the source side and a peripheral address on the destination side.

(6) M2P LCH3 parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
5300H	M2P LCH3 source address register (start address)	DMA_M2P_LCH3_AADD	R/W	0000_0000H
5304H	M2P LCH3 source address pointer register	DMA_M2P_LCH3_AADP	R	0000_0000H
5308H	M2P LCH3 source address offset register	DMA_M2P_LCH3_AOFF	R/W	0000_0000H
530CH	M2P LCH3 source block size register	DMA_M2P_LCH3_ASIZE	R/W	0000_0000H
5310H	M2P LCH3 source block count register	DMA_M2P_LCH3_ASIZE_COUNT	R/W	0000_0000H
5314H to 531CH	Reserved	–	–	–
5320H	M2P LCH3 destination address register	DMA_M2P_LCH3_BADD	R/W	0000_0000H
5324H to 533CH	Reserved	–	–	–
5340H	M2P LCH3 length register	DMA_M2P_LCH3_LENG	R/W	0000_0000H
5344H	M2P LCH3 read length count register	DMA_M2P_LCH3_LENG_RCOUNT	R	0000_0000H
5348H	M2P LCH3 write length count register	DMA_M2P_LCH3_LENG_WCOUNT	R	0000_0000H
534CH	Reserved	–	–	–
5350H	M2P LCH3 mode register (bit width, read/write endian, repeat)	DMA_M2P_LCH3_MODE	R/W	E4E4_0000H
5354H to 53FCH	Reserved	–	–	–

Remark Set a memory address on the source side and a peripheral address on the destination side.

(7) M2P LCH4 parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
5400H	M2P LCH4 source address register (start address)	DMA_M2P_LCH4_AADD	R/W	0000_0000H
5404H	M2P LCH4 source address pointer register	DMA_M2P_LCH4_AADP	R	0000_0000H
5408H	M2P LCH4 source address offset register	DMA_M2P_LCH4_AOFF	R/W	0000_0000H
540CH	M2P LCH4 source block size register	DMA_M2P_LCH4_ASIZE	R/W	0000_0000H
5410H	M2P LCH4 source block count register	DMA_M2P_LCH4_ASIZE_ COUNT	R/W	0000_0000H
5414H to 541CH	Reserved	–	–	–
5420H	M2P LCH4 destination address register	DMA_M2P_LCH4_BADD	R/W	0000_0000H
5424H to 543CH	Reserved	–	–	–
5440H	M2P LCH4 length register	DMA_M2P_LCH4_LENG	R/W	0000_0000H
5444H	M2P LCH4 read length count register	DMA_M2P_LCH4_LENG_ RCOUNT	R	0000_0000H
5448H	M2P LCH4 write length count register	DMA_M2P_LCH4_LENG_ WCOUNT	R	0000_0000H
544CH	Reserved	–	–	–
5450H	M2P LCH4 mode register (bit width, read/write endian, repeat)	DMA_M2P_LCH4_MODE	R/W	E4E4_0000H
5454H to 54FCH	Reserved	–	–	–

Remark Set a memory address on the source side and a peripheral address on the destination side.

(8) M2P LCH5 parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
5500H	M2P LCH5 source address register (start address)	DMA_M2P_LCH5_AADD	R/W	0000_0000H
5504H	M2P LCH5 source address pointer register	DMA_M2P_LCH5_AADP	R	0000_0000H
5508H	M2P LCH5 source address offset register	DMA_M2P_LCH5_AOFF	R/W	0000_0000H
550CH	M2P LCH5 source block size register	DMA_M2P_LCH5_ASIZE	R/W	0000_0000H
5510H	M2P LCH5 source block count register	DMA_M2P_LCH5_ASIZE_COUNT	R/W	0000_0000H
5514H to 551CH	Reserved	–	–	–
5520H	M2P LCH5 destination address register	DMA_M2P_LCH5_BADD	R/W	0000_0000H
5524H to 553CH	Reserved	–	–	–
5540H	M2P LCH5 length register	DMA_M2P_LCH5_LENG	R/W	0000_0000H
5544H	M2P LCH5 read length count register	DMA_M2P_LCH5_LENG_RCOUNT	R	0000_0000H
5548H	M2P LCH5 write length count register	DMA_M2P_LCH5_LENG_WCOUNT	R	0000_0000H
554CH	Reserved	–	–	–
5550H	M2P LCH5 mode register (bit width, read/write endian, repeat)	DMA_M2P_LCH5_MODE	R/W	E4E4_0000H
5554H to 56FCH	Reserved	–	–	–

Remark Set a memory address on the source side and a peripheral address on the destination side.

(9) M2P LCH9 parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
5900H	M2P LCH9 source address register (start address)	DMA_M2P_LCH9_AADD	R/W	0000_0000H
5904H	M2P LCH9 source address pointer register	DMA_M2P_LCH9_AADP	R	0000_0000H
5908H	M2P LCH9 source address offset register	DMA_M2P_LCH9_AOFF	R/W	0000_0000H
590CH	M2P LCH9 source block size register	DMA_M2P_LCH9_ASIZE	R/W	0000_0000H
5910H	M2P LCH9 source block count register	DMA_M2P_LCH9_ASIZE_ COUNT	R/W	0000_0000H
5914H to 591CH	Reserved	–	–	–
5920H	M2P LCH9 destination address register	DMA_M2P_LCH9_BADD	R/W	0000_0000H
5924H to 593CH	Reserved	–	–	–
5940H	M2P LCH9 length register	DMA_M2P_LCH9_LENG	R/W	0000_0000H
5944H	M2P LCH9 read length count register	DMA_M2P_LCH9_LENG_ RCOUNT	R	0000_0000H
5948H	M2P LCH9 write length count register	DMA_M2P_LCH9_LENG_ WCOUNT	R	0000_0000H
594CH	Reserved	–	–	–
5950H	M2P LCH9 mode register (bit width, read/write endian, repeat)	DMA_M2P_LCH9_MODE	R/W	E4E4_0000H
5954H to 59FCH	Reserved	–	–	–

Remark Set a memory address on the source side and a peripheral address on the destination side.

(10) M2P LCH10 parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
5A00H	M2P LCH10 source address register (start address)	DMA_M2P_LCH10_AADD	R/W	0000_0000H
5A04H	M2P LCH10 source address pointer register	DMA_M2P_LCH10_AADP	R	0000_0000H
5A08H	M2P LCH10 source address offset register	DMA_M2P_LCH10_AOFF	R/W	0000_0000H
5A0CH	M2P LCH10 source block size register	DMA_M2P_LCH10_ASIZE	R/W	0000_0000H
5A10H	M2P LCH10 source block count register	DMA_M2P_LCH10_ASIZE_COUNT	R/W	0000_0000H
5A14H to 5A1CH	Reserved	–	–	–
5A20H	M2P LCH10 destination address register	DMA_M2P_LCH10_BADD	R/W	0000_0000H
5A24H to 5A3CH	Reserved	–	–	–
5A40H	M2P LCH10 length register	DMA_M2P_LCH10_LENG	R/W	0000_0000H
5A44H	M2P LCH10 read length count register	DMA_M2P_LCH10_LENG_RCOUNT	R	0000_0000H
5A48H	M2P LCH10 write length count register	DMA_M2P_LCH10_LENG_WCOUNT	R	0000_0000H
5A4CH	Reserved	–	–	–
5A50H	M2P LCH10 mode register (bit width, read/write endian, repeat)	DMA_M2P_LCH10_MODE	R/W	E4E4_0000H
5A54H to 5AFCH	Reserved	–	–	–

Remark Set a memory address on the source side and a peripheral address on the destination side.

(11) M2P LCH12 parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
5C00H	M2P LCH12 source address register (start address)	DMA_M2P_LCH12_AADD	R/W	0000_0000H
5C04H	M2P LCH12 source address pointer register	DMA_M2P_LCH12_AADP	R	0000_0000H
5C08H	M2P LCH12 source address offset register	DMA_M2P_LCH12_AOFF	R/W	0000_0000H
5C0CH	M2P LCH12 source block size register	DMA_M2P_LCH12_ASIZE	R/W	0000_0000H
5C10H	M2P LCH12 source block count register	DMA_M2P_LCH12_ASIZE_COUNT	R/W	0000_0000H
5C14H to 5C1CH	Reserved	–	–	–
5C20H	M2P LCH12 destination address register	DMA_M2P_LCH12_BADD	R/W	0000_0000H
5C24H to 5C3CH	Reserved	–	–	–
5C40H	M2P LCH12 length register	DMA_M2P_LCH12_LENG	R/W	0000_0000H
5C44H	M2P LCH12 read length count register	DMA_M2P_LCH12_LENG_RCOUNT	R	0000_0000H
5C48H	M2P LCH12 write length count register	DMA_M2P_LCH12_LENG_WCOUNT	R	0000_0000H
5C4CH	Reserved	–	–	–
5C50H	M2P LCH12 mode register (bit width, read/write endian, repeat)	DMA_M2P_LCH12_MODE	R/W	E4E4_0000H
5C54H to 5CFCH	Reserved	–	–	–

Remark Set a memory address on the source side and a peripheral address on the destination side.

(12) M2P LCH13 parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
5D00H	M2P LCH13 source address register (start address)	DMA_M2P_LCH13_AADD	R/W	0000_0000H
5D04H	M2P LCH13 source address pointer register	DMA_M2P_LCH13_AADP	R	0000_0000H
5D08H	M2P LCH13 source address offset register	DMA_M2P_LCH13_AOFF	R/W	0000_0000H
5D0CH	M2P LCH13 source block size register	DMA_M2P_LCH13_ASIZE	R/W	0000_0000H
5D10H	M2P LCH13 source block count register	DMA_M2P_LCH13_ASIZE_COUNT	R/W	0000_0000H
5D14H to 5D1CH	Reserved	–	–	–
5D20H	M2P LCH13 destination address register	DMA_M2P_LCH13_BADD	R/W	0000_0000H
5D24H to 5D3CH	Reserved	–	–	–
5D40H	M2P LCH13 length register	DMA_M2P_LCH13_LENG	R/W	0000_0000H
5D44H	M2P LCH13 read length count register	DMA_M2P_LCH13_LENG_RCOUNT	R	0000_0000H
5D48H	M2P LCH13 write length count register	DMA_M2P_LCH13_LENG_WCOUNT	R	0000_0000H
5D4CH	Reserved	–	–	–
5D50H	M2P LCH13 mode register (bit width, read/write endian, repeat)	DMA_M2P_LCH13_MODE	R/W	E4E4_0000H
5D54H to 5DFCH	Reserved	–	–	–

Remark Set a memory address on the source side and a peripheral address on the destination side.

(13) M2P LCH14 parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
5E00H	M2P LCH14 source address register (start address)	DMA_M2P_LCH14_AADD	R/W	0000_0000H
5E04H	M2P LCH14 source address pointer register	DMA_M2P_LCH14_AADP	R	0000_0000H
5E08H	M2P LCH14 source address offset register	DMA_M2P_LCH14_AOFF	R/W	0000_0000H
5E0CH	M2P LCH14 source block size register	DMA_M2P_LCH14_ASIZE	R/W	0000_0000H
5E10H	M2P LCH14 source block count register	DMA_M2P_LCH14_ASIZE_COUNT	R/W	0000_0000H
5E14H to 5E1CH	Reserved	–	–	–
5E20H	M2P LCH14 destination address register	DMA_M2P_LCH14_BADD	R/W	0000_0000H
5E24H to 5E3CH	Reserved	–	–	–
5E40H	M2P LCH14 length register	DMA_M2P_LCH14_LENG	R/W	0000_0000H
5E44H	M2P LCH14 read length count register	DMA_M2P_LCH14_LENG_RCOUNT	R	0000_0000H
5E48H	M2P LCH14 write length count register	DMA_M2P_LCH14_LENG_WCOUNT	R	0000_0000H
5E4CH	Reserved	–	–	–
5E50H	M2P LCH14 mode register (bit width, read/write endian, repeat)	DMA_M2P_LCH14_MODE	R/W	E4E4_0000H
5E54H to 5EFCH	Reserved	–	–	–

Remark Set a memory address on the source side and a peripheral address on the destination side.

2.2.3 P2M (peripheral-to-memory transfer) registers

Caution LCH6 and LCH8 are reserved channels, so there are no corresponding register bits

(1) P2M DMA control registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
6000H	P2M DMA start control register	DMA_P2M_CONT	W	0000_0000H
6004H	P2M DMA control status register	DMA_P2M_CONTSTATUS	R	0000_0000H
6008H	P2M DMA end control register	DMA_P2M_END	W	0000_0000H
600CH to 60FCH	Reserved	–	–	–

(2) P2M interrupt parameter setting registers

Base address: 4009_0000H

(1/3)

Address	Register Name	Symbol	R/W	After Reset
6800H	P2M interrupt output destination setting register (LCH0 to LCH14)	DMA_P2M_LCH0LCH14_INT_SEL	R/W	0000_0000H
6804H to 6FFCH	Reserved	–	–	–
6100H	ACPU interrupt status register (LCH0 to LCH3)	DMA_P2M_PE0_LCH0LCH3_INT_CONT	R	0000_0000H
6104H	ACPU interrupt raw status register (LCH0 to LCH3)	DMA_P2M_PE0_LCH0LCH3_INT_RAW	R	0000_0000H
6108H	ACPU interrupt enable set register (LCH0 to LCH3)	DMA_P2M_PE0_LCH0LCH3_INT_ENABLE	R/W	0000_0000H
610CH	ACPU interrupt enable clear register (LCH0 to LCH3)	DMA_P2M_PE0_LCH0LCH3_INT_ENABLE_CL	W	0000_0000H
6110H	ACPU interrupt source clear register (LCH0 to LCH3)	DMA_P2M_PE0_LCH0LCH3_INT_REQ_CL	W	0000_0000H
6114H to 611CH	Reserved	–	–	–
6120H	ACPU interrupt status register (LCH4 to LCH5)	DMA_P2M_PE0_LCH4LCH5_INT_CONT	R	0000_0000H
6124H	ACPU interrupt raw status register (LCH4 to LCH5)	DMA_P2M_PE0_LCH4LCH5_INT_RAW	R	0000_0000H
6128H	ACPU interrupt enable set register (LCH4 to LCH5)	DMA_P2M_PE0_LCH4LCH5_INT_ENABLE	R/W	0000_0000H
612CH	ACPU interrupt enable clear register (LCH4 to LCH5)	DMA_P2M_PE0_LCH4LCH5_INT_ENABLE_CL	W	0000_0000H
6130H	ACPU interrupt source clear register (LCH4 to LCH5)	DMA_P2M_PE0_LCH4LCH5_INT_REQ_CL	W	0000_0000H
6134H to 613FH	Reserved	–	–	–

(2/3)

Address	Register Name	Symbol	R/W	After Reset
6140H	ACPU interrupt status register (LCH9 to LCH10)	DMA_P2M_PE0_LCH9LCH10_INT_CONT	R	0000_0000H
6144H	ACPU interrupt raw status register (LCH9 to LCH10)	DMA_P2M_PE0_LCH9LCH10_INT_RAW	R	0000_0000H
6148H	ACPU interrupt enable set register (LCH9 to LCH10)	DMA_P2M_PE0_LCH9LCH10_INT_ENABLE	R/W	0000_0000H
614CH	ACPU interrupt enable clear register (LCH9 to LCH10)	DMA_P2M_PE0_LCH9LCH10_INT_ENABLE_CL	W	0000_0000H
6150H	ACPU interrupt source clear register (LCH9 to LCH10)	DMA_P2M_PE0_LCH9LCH10_INT_REQ_CL	W	0000_0000H
6154H to 615CH	Reserved	–	–	–
6160H	ACPU interrupt status register (LCH12 to LCH14)	DMA_P2M_PE0_LCH12LCH14_INT_CONT	R	0000_0000H
6164H	ACPU interrupt raw status register (LCH12 to LCH14)	DMA_P2M_PE0_LCH12LCH14_INT_RAW	R	0000_0000H
6168H	ACPU interrupt enable set register (LCH12 to LCH14)	DMA_P2M_PE0_LCH12LCH14_INT_ENABLE	R/W	0000_0000H
616CH	ACPU interrupt enable clear register (LCH12 to LCH14)	DMA_P2M_PE0_LCH12LCH14_INT_ENABLE_CL	W	0000_0000H
6170H	ACPU interrupt source clear register (LCH12 to LCH14)	DMA_P2M_PE0_LCH12LCH14_INT_REQ_CL	W	0000_0000H
6174H to 63FCH	Reserved	–	–	–
6400H	DSP interrupt status register (LCH0 to LCH3)	DMA_P2M_DSP_LCH0LCH3_INT_CONT	R	0000_0000H
6404H	DSP interrupt raw status register (LCH0 to LCH3)	DMA_P2M_DSP_LCH0LCH3_INT_RAW	R	0000_0000H
6408H	DSP interrupt enable set register (LCH0 to LCH3)	DMA_P2M_DSP_LCH0LCH3_INT_ENABLE	R/W	0000_0000H
640CH	DSP interrupt enable clear register (LCH0 to LCH3)	DMA_P2M_DSP_LCH0LCH3_INT_ENABLE_CL	W	0000_0000H
6410H	DSP interrupt source clear register (LCH0 to LCH3)	DMA_P2M_DSP_LCH0LCH3_INT_REQ_CL	W	0000_0000H
6414H to 641CH	Reserved	–	–	–
6420H	DSP interrupt status register (LCH4 to LCH5)	DMA_P2M_DSP_LCH4LCH5_INT_CONT	R	0000_0000H
6424H	DSP interrupt raw status register (LCH4 to LCH5)	DMA_P2M_DSP_LCH4LCH5_INT_RAW	R	0000_0000H
6428H	DSP interrupt enable set register (LCH4 to LCH5)	DMA_P2M_DSP_LCH4LCH5_INT_ENABLE	R/W	0000_0000H
642CH	DSP interrupt enable clear register (LCH4 to LCH5)	DMA_P2M_DSP_LCH4LCH5_INT_ENABLE_CL	W	0000_0000H

(3/3)

Address	Register Name	Symbol	R/W	After Reset
6430H	DSP interrupt source clear register (LCH4 to LCH5)	DMA_P2M_DSP_LCH4LCH5_INT_REQ_CL	W	0000_0000H
6434H to 643CH	Reserved	–	–	–
6440H	DSP interrupt status register (LCH9 to LCH10)	DMA_P2M_DSP_LCH9LCH10_INT_CONT	R	0000_0000H
6444H	DSP interrupt raw status register (LCH9 to LCH10)	DMA_P2M_DSP_LCH9LCH10_INT_RAW	R	0000_0000H
6448H	DSP interrupt enable set register (LCH9 to LCH10)	DMA_P2M_DSP_LCH9LCH10_INT_ENABLE	R/W	0000_0000H
644CH	DSP interrupt enable clear register (LCH9 to LCH10)	DMA_P2M_DSP_LCH9LCH10_INT_ENABLE_CL	W	0000_0000H
6450H	DSP interrupt source clear register (LCH9 to LCH10)	DMA_P2M_DSP_LCH9LCH10_INT_REQ_CL	W	0000_0000H
6454H to 645CH	Reserved	–	–	–
6460H	DSP interrupt status register (LCH12 to LCH14)	DMA_P2M_DSP_LCH12LCH14_INT_CONT	R	0000_0000H
6464H	DSP interrupt raw status register (LCH12 to LCH14)	DMA_P2M_DSP_LCH12LCH14_INT_RAW	R	0000_0000H
6468H	DSP interrupt enable set register (LCH12 to LCH14)	DMA_P2M_DSP_LCH12LCH14_INT_ENABLE	R/W	0000_0000H
646CH	DSP interrupt enable clear register (LCH12 to LCH14)	DMA_P2M_DSP_LCH12LCH14_INT_ENABLE_CL	W	0000_0000H
6470H	DSP interrupt source clear register (LCH12 to LCH14)	DMA_P2M_DSP_LCH12LCH14_INT_REQ_CL	W	0000_0000H
6474H to 67FCH	Reserved	–	–	–

(3) P2M LCH0 parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
7000H	P2M LCH0 source address register	DMA_P2M_LCH0_AADD	R/W	0000_0000H
7004H to 701CH	Reserved	–	–	–
7020H	P2M LCH0 destination address register (start address)	DMA_P2M_LCH0_BADD	R/W	0000_0000H
7024H	P2M LCH0 destination address pointer register	DMA_P2M_LCH0_BADP	R	0000_0000H
7028H	P2M LCH0 destination address offset register	DMA_P2M_LCH0_BOFF	R/W	0000_0000H
702CH	P2M LCH0 destination block size register	DMA_P2M_LCH0_BSIZE	R/W	0000_0000H
7030H	P2M LCH0 destination block count register	DMA_P2M_LCH0_BSIZE_COUNT	R/W	0000_0000H
7034H to 703CH	Reserved	–	–	–
7040H	P2M LCH0 length register	DMA_P2M_LCH0_LENG	R/W	0000_0000H
7044H	P2M LCH0 read length count register	DMA_P2M_LCH0_LENG_RCOUNT	R	0000_0000H
7048H	P2M LCH0 write length count register	DMA_P2M_LCH0_LENG_WCOUNT	R	0000_0000H
704CH	Reserved	–	–	–
7050H	P2M LCH0 mode register (timer setting, bit width, read/write endian, repeat)	DMA_P2M_LCH0_MODE	R/W	E4E4_0000H
7054H	P2M LCH0 timer register	DMA_P2M_LCH0_TIME	R/W	0000_0000H
7058H	P2M LCH0 timer count register	DMA_P2M_LCH0_TIME_COUNT	R	0000_0000H
705CH to 70FCH	Reserved	–	–	–

Remark Set a peripheral address on the source side and a memory address on the destination side.

(4) P2M LCH1 parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
7100H	P2M LCH1 source address register	DMA_P2M_LCH1_AADD	R/W	0000_0000H
7104H to 711CH	Reserved	–	–	–
7120H	P2M LCH1 destination address register (start address)	DMA_P2M_LCH1_BADD	R/W	0000_0000H
7124H	P2M LCH1 destination address pointer register	DMA_P2M_LCH1_BADP	R	0000_0000H
7128H	P2M LCH1 destination address offset register	DMA_P2M_LCH1_BOFF	R/W	0000_0000H
712CH	P2M LCH1 destination block size register	DMA_P2M_LCH1_BSIZE	R/W	0000_0000H
7130H	P2M LCH1 destination block count register	DMA_P2M_LCH1_BSIZE_COUNT	R/W	0000_0000H
7134H to 713CH	Reserved	–	–	–
7140H	P2M LCH1 length register	DMA_P2M_LCH1_LENG	R/W	0000_0000H
7144H	P2M LCH1 read length count register	DMA_P2M_LCH1_LENG_RCOUNT	R	0000_0000H
7148H	P2M LCH1 write length count register	DMA_P2M_LCH1_LENG_WCOUNT	R	0000_0000H
714CH	Reserved	–	–	–
7150H	P2M LCH1 mode register (timer setting, bit width, read/write endian, repeat)	DMA_P2M_LCH1_MODE	R/W	E4E4_0000H
7154H	P2M LCH1 timer register	DMA_P2M_LCH1_TIME	R/W	0000_0000H
7158H	P2M LCH1 timer count register	DMA_P2M_LCH1_TIME_COUNT	R	0000_0000H
715CH to 71FCH	Reserved	–	–	–

Remark Set a peripheral address on the source side and a memory address on the destination side.

(5) P2M LCH2 parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
7200H	P2M LCH2 source address register	DMA_P2M_LCH2_AADD	R/W	0000_0000H
7204H to 721CH	Reserved	–	–	–
7220H	P2M LCH2 destination address register (start address)	DMA_P2M_LCH2_BADD	R/W	0000_0000H
7224H	P2M LCH2 destination address pointer register	DMA_P2M_LCH2_BADP	R	0000_0000H
7228H	P2M LCH2 destination address offset register	DMA_P2M_LCH2_BOFF	R/W	0000_0000H
722CH	P2M LCH2 destination block size register	DMA_P2M_LCH2_BSIZE	R/W	0000_0000H
7230H	P2M LCH2 destination block count register	DMA_P2M_LCH2_BSIZE_COUNT	R/W	0000_0000H
7234H to 723CH	Reserved	–	–	–
7240H	P2M LCH2 length register	DMA_P2M_LCH2_LENG	R/W	0000_0000H
7244H	P2M LCH2 read length count register	DMA_P2M_LCH2_LENG_RCOUNT	R	0000_0000H
7248H	P2M LCH2 write length count register	DMA_P2M_LCH2_LENG_WCOUNT	R	0000_0000H
724CH	Reserved	–	–	–
7250H	P2M LCH2 mode register (timer setting, bit width, read/write endian, repeat)	DMA_P2M_LCH2_MODE	R/W	E4E4_0000H
7254H	P2M LCH2 timer register	DMA_P2M_LCH2_TIME	R/W	0000_0000H
7258H	P2M LCH2 timer count register	DMA_P2M_LCH2_TIME_COUNT	R	0000_0000H
725CH to 72FCH	Reserved	–	–	–

Remark Set a peripheral address on the source side and a memory address on the destination side.

(6) P2M LCH3 parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
7300H	P2M LCH3 source address register	DMA_P2M_LCH3_AADD	R/W	0000_0000H
7304H to 731CH	Reserved	–	–	–
7320H	P2M LCH3 destination address register (start address)	DMA_P2M_LCH3_BADD	R/W	0000_0000H
7324H	P2M LCH3 destination address pointer register	DMA_P2M_LCH3_BADP	R	0000_0000H
7328H	P2M LCH3 destination address offset register	DMA_P2M_LCH3_BOFF	R/W	0000_0000H
732CH	P2M LCH3 destination block size register	DMA_P2M_LCH3_BSIZE	R/W	0000_0000H
7330H	P2M LCH3 destination block count register	DMA_P2M_LCH3_BSIZE_COUNT	R/W	0000_0000H
7334H to 733CH	Reserved	–	–	–
7340H	P2M LCH3 length register	DMA_P2M_LCH3_LENG	R/W	0000_0000H
7344H	P2M LCH3 read length count register	DMA_P2M_LCH3_LENG_RCOUNT	R	0000_0000H
7348H	P2M LCH3 write length count register	DMA_P2M_LCH3_LENG_WCOUNT	R	0000_0000H
734CH	Reserved	–	–	–
7350H	P2M LCH3 mode register (bit width, read/write endian, repeat)	DMA_P2M_LCH3_MODE	R/W	E4E4_0000H
7354H to 73FCH	Reserved	–	–	–

Remark Set a peripheral address on the source side and a memory address on the destination side.

(7) P2M LCH4 parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
7400H	P2M LCH4 source address register	DMA_P2M_LCH4_AADD	R/W	0000_0000H
7404H to 741CH	Reserved	–	–	–
7420H	P2M LCH4 destination address register (start address)	DMA_P2M_LCH4_BADD	R/W	0000_0000H
7424H	P2M LCH4 destination address pointer register	DMA_P2M_LCH4_BADP	R	0000_0000H
7428H	P2M LCH4 destination address offset register	DMA_P2M_LCH4_BOFF	R/W	0000_0000H
742CH	P2M LCH4 destination block size register	DMA_P2M_LCH4_BSIZE	R/W	0000_0000H
7430H	P2M LCH4 destination block count register	DMA_P2M_LCH4_BSIZE_COUNT	R/W	0000_0000H
7434H to 743CH	Reserved	–	–	–
7440H	P2M LCH4 length register	DMA_P2M_LCH4_LENG	R/W	0000_0000H
7444H	P2M LCH4 read length count register	DMA_P2M_LCH4_LENG_RCOUNT	R	0000_0000H
7448H	P2M LCH4 write length count register	DMA_P2M_LCH4_LENG_WCOUNT	R	0000_0000H
744CH	Reserved	–	–	–
7450H	P2M LCH4 mode register (bit width, read/write endian, repeat)	DMA_P2M_LCH4_MODE	R/W	E4E4_0000H
7454H to 74FCH	Reserved	–	–	–

Remark Set a peripheral address on the source side and a memory address on the destination side.

(8) P2M LCH5 parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
7500H	P2M LCH5 source address register	DMA_P2M_LCH5_AADD	R/W	0000_0000H
7504H to 751CH	Reserved	–	–	–
7520H	P2M LCH5 destination address register (start address)	DMA_P2M_LCH5_BADD	R/W	0000_0000H
7524H	P2M LCH5 destination address pointer register	DMA_P2M_LCH5_BADP	R	0000_0000H
7528H	P2M LCH5 destination address offset register	DMA_P2M_LCH5_BOFF	R/W	0000_0000H
752CH	P2M LCH5 destination block size register	DMA_P2M_LCH5_BSIZE	R/W	0000_0000H
7530H	P2M LCH5 destination block count register	DMA_P2M_LCH5_BSIZE_COUNT	R/W	0000_0000H
7534H to 753CH	Reserved	–	–	–
7540H	P2M LCH5 length register	DMA_P2M_LCH5_LENG	R/W	0000_0000H
7544H	P2M LCH5 read length count register	DMA_P2M_LCH5_LENG_RCOUNT	R	0000_0000H
7548H	P2M LCH5 write length count register	DMA_P2M_LCH5_LENG_WCOUNT	R	0000_0000H
754CH	Reserved	–	–	–
7550H	P2M LCH5 mode register (bit width, read/write endian, repeat)	DMA_P2M_LCH5_MODE	R/W	E4E4_0000H
7554H to 76FCH	Reserved	–	–	–

Remark Set a peripheral address on the source side and a memory address on the destination side.

(9) P2M LCH9 parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
7900H	P2M LCH9 source address register	DMA_P2M_LCH9_AADD	R/W	0000_0000H
7904H to 791CH	Reserved	–	–	–
7920H	P2M LCH9 destination address register (start address)	DMA_P2M_LCH9_BADD	R/W	0000_0000H
7924H	P2M LCH9 destination address pointer register	DMA_P2M_LCH9_BADP	R	0000_0000H
7928H	P2M LCH9 destination address offset register	DMA_P2M_LCH9_BOFF	R/W	0000_0000H
792CH	P2M LCH9 destination block size register	DMA_P2M_LCH9_BSIZE	R/W	0000_0000H
7930H	P2M LCH9 destination block count register	DMA_P2M_LCH9_BSIZE_COUNT	R/W	0000_0000H
7934H to 793CH	Reserved	–	–	–
7940H	P2M LCH9 length register	DMA_P2M_LCH9_LENG	R/W	0000_0000H
7944H	P2M LCH9 read length count register	DMA_P2M_LCH9_LENG_RCOUNT	R	0000_0000H
7948H	P2M LCH9 write length count register	DMA_P2M_LCH9_LENG_WCOUNT	R	0000_0000H
794CH	Reserved	–	–	–
7950H	P2M LCH9 mode register (bit width, read/write endian, repeat)	DMA_P2M_LCH9_MODE	R/W	E4E4_0000H
7954H to 79FCH	Reserved	–	–	–

Remark Set a peripheral address on the source side and a memory address on the destination side.

(11) P2M LCH10 parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
7A00H	P2M LCH10 source address register	DMA_P2M_LCH10_AADD	R/W	0000_0000H
7A04H to 7A1CH	Reserved	–	–	–
7A20H	P2M LCH10 destination address register (start address)	DMA_P2M_LCH10_BADD	R/W	0000_0000H
7A24H	P2M LCH10 destination address pointer register	DMA_P2M_LCH10_BADP	R	0000_0000H
7A28H	P2M LCH10 destination address offset register	DMA_P2M_LCH10_BOFF	R/W	0000_0000H
7A2CH	P2M LCH10 destination block size register	DMA_P2M_LCH10_BSIZE	R/W	0000_0000H
7A30H	P2M LCH10 destination block count register	DMA_P2M_LCH10_BSIZE_COUNT	R/W	0000_0000H
7A34H to 7A3CH	Reserved	–	–	–
7A40H	P2M LCH10 length register	DMA_P2M_LCH10_LENG	R/W	0000_0000H
7A44H	P2M LCH10 read length count register	DMA_P2M_LCH10_LENG_RCOUNT	R	0000_0000H
7A48H	P2M LCH10 write length count register	DMA_P2M_LCH10_LENG_WCOUNT	R	0000_0000H
7A4CH	Reserved	–	–	–
7A50H	P2M LCH10 mode register (bit width, read/write endian, repeat)	DMA_P2M_LCH10_MODE	R/W	E4E4_0000H
7A54H to 7AFCH	Reserved	–	–	–

Remark Set a peripheral address on the source side and a memory address on the destination side.

(11) P2M LCH12 parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
7C00H	P2M LCH12 source address register	DMA_P2M_LCH12_AADD	R/W	0000_0000H
7C04H to 7C1CH	Reserved	–	–	–
7C20H	P2M LCH12 destination address register (start address)	DMA_P2M_LCH12_BADD	R/W	0000_0000H
7C24H	P2M LCH12 destination address pointer register	DMA_P2M_LCH12_BADP	R	0000_0000H
7C28H	P2M LCH12 destination address offset register	DMA_P2M_LCH12_BOFF	R/W	0000_0000H
7C2CH	P2M LCH12 destination block size register	DMA_P2M_LCH12_BSIZE	R/W	0000_0000H
7C30H	P2M LCH12 destination block count register	DMA_P2M_LCH12_BSIZE_COUNT	R/W	0000_0000H
7C34H to 7C3CH	Reserved	–	–	–
7C40H	P2M LCH12 length register	DMA_P2M_LCH12_LENG	R/W	0000_0000H
7C44H	P2M LCH12 read length count register	DMA_P2M_LCH12_LENG_RCOUNT	R	0000_0000H
7C48H	P2M LCH12 write length count register	DMA_P2M_LCH12_LENG_WCOUNT	R	0000_0000H
7C4CH	Reserved	–	–	–
7C50H	P2M LCH12 mode register (bit width, read/write endian, repeat)	DMA_P2M_LCH12_MODE	R/W	E4E4_0000H
7C54H to 7C5FH	Reserved	–	–	–

Remark Set a peripheral address on the source side and a memory address on the destination side.

(12) P2M LCH13 parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
7D00H	P2M LCH13 source address register	DMA_P2M_LCH13_AADD	R/W	0000_0000H
7D04H to 7D1CH	Reserved	–	–	–
7D20H	P2M LCH13 destination address register (start address)	DMA_P2M_LCH13_BADD	R/W	0000_0000H
7D24H	P2M LCH13 destination address pointer register	DMA_P2M_LCH13_BADP	R	0000_0000H
7D28H	P2M LCH13 destination address offset register	DMA_P2M_LCH13_BOFF	R/W	0000_0000H
7D2CH	P2M LCH13 destination block size register	DMA_P2M_LCH13_BSIZE	R/W	0000_0000H
7D30H	P2M LCH13 destination block count register	DMA_P2M_LCH13_BSIZE_COUNT	R/W	0000_0000H
7D34H to 7D3CH	Reserved	–	–	–
7D40H	P2M LCH13 length register	DMA_P2M_LCH13_LENG	R/W	0000_0000H
7D44H	P2M LCH13 read length count register	DMA_P2M_LCH13_LENG_RCOUNT	R	0000_0000H
7D48H	P2M LCH13 write length count register	DMA_P2M_LCH13_LENG_WCOUNT	R	0000_0000H
7D4CH	Reserved	–	–	–
7D50H	P2M LCH13 mode register (bit width, read/write endian, repeat)	DMA_P2M_LCH13_MODE	R/W	E4E4_0000H
7D54H to 7DFCH	Reserved	–	–	–

Remark Set a peripheral address on the source side and a memory address on the destination side.

(13) P2M LCH14 parameter setting registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
7E00H	P2M LCH14 source address register	DMA_P2M_LCH14_AADD	R/W	0000_0000H
7E04H to 7E1CH	Reserved	–	–	–
7E20H	P2M LCH14 destination address register (start address)	DMA_P2M_LCH14_BADD	R/W	0000_0000H
7E24H	P2M LCH14 destination address pointer register	DMA_P2M_LCH14_BADP	R	0000_0000H
7E28H	P2M LCH14 destination address offset register	DMA_P2M_LCH14_BOFF	R/W	0000_0000H
7E2CH	P2M LCH14 destination block size register	DMA_P2M_LCH14_BSIZE	R/W	0000_0000H
7E30H	P2M LCH14 destination block count register	DMA_P2M_LCH14_BSIZE_COUNT	R/W	0000_0000H
7E34H to 7E3CH	Reserved	–	–	–
7E40H	P2M LCH14 length register	DMA_P2M_LCH14_LENG	R/W	0000_0000H
7E44H	P2M LCH14 read length count register	DMA_P2M_LCH14_LENG_RCOUNT	R	0000_0000H
7E48H	P2M LCH14 write length count register	DMA_P2M_LCH14_LENG_WCOUNT	R	0000_0000H
7E4CH	Reserved	–	–	–
7E50H	P2M LCH14 mode register (bit width, read/write endian, repeat)	DMA_P2M_LCH14_MODE	R/W	E4E4_0000H
7E54H to 7EFCH	Reserved	–	–	–

Remark Set a peripheral address on the source side and a memory address on the destination side.

2.2.4 Interrupt index registers

Base address: 4009_0000H

Address	Register Name	Symbol	R/W	After Reset
8000H	ACPU interrupt index register	DMA_PE0_INT_INDEX	R	0000_0000H
8004H to 8008H	Reserved	–	–	–
800CH	ADSP interrupt index register	DMA_DSP_INT_INDEX	R	0000_0000H
8010H to 80FCH	Reserved	–	–	–
8100H	ACPU interrupt index 2 register (LCH is assigned per bit)	DMA_PE0_INT_INDEX2	R	0000_0000H
8104H to 8108H	Reserved	–	–	–
810CH	ADSP interrupt index 2 register (LCH is assigned per bit)	DMA_DSP_INT_INDEX2	R	0000_0000H
8110H to 8FFCH	Reserved	–	–	–

2.3 Register Functions

2.3.1 ACPU DMA control/status registers

(1) ACPU DMA start control register

This register (DMA_ARM_CONT: 4009_0000H) controls whether to start DMA transfer on a per-logical channel basis.

If this register is set up while the ARM_LCHx_RESERVE bit of the ACPU DMA start control status register is set to 0, the subsequent transfer starts immediately after the current transfer ends (simple reservation). A transfer parameter for the subsequent transfer must be set before using simple reservation. For details, see **3.4.3 Continuous transfer**.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				ARM_LCH3_CONT	ARM_LCH2_CONT	ARM_LCH1_CONT	ARM_LCH0_CONT

Name	R/W	Bit	After Reset	Function
Reserved	R	31:4	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCH3_CONT	W	3	0	Controls whether to start DMA transfer on ACPU LCH3. (1: Starts DMA transfer.)
ARM_LCH2_CONT	W	2	0	Controls whether to start DMA transfer on ACPU LCH2. (1: Starts DMA transfer.)
ARM_LCH1_CONT	W	1	0	Controls whether to start DMA transfer on ACPU LCH1. (1: Starts DMA transfer.)
ARM_LCH0_CONT	W	0	0	Controls whether to start DMA transfer on ACPU LCH0. (1: Starts DMA transfer.)

(2) ACPU DMA control status register

This register (DMA_ARM_CONTSTATUS: 4009_0004H) indicates the status of the DMA controller.

The DMA start reservation status register indicates whether DMA transfer has been reserved. If a bit is set to 1, the corresponding LCH has already been reserved for the next transfer, so another reservation cannot be made.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved				ARM_LCH3_RESERVE	ARM_LCH2_RESERVE	ARM_LCH1_RESERVE	ARM_LCH0_RESERVE
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				ARM_LCH3_CONTSTATUS	ARM_LCH2_CONTSTATUS	ARM_LCH1_CONTSTATUS	ARM_LCH0_CONTSTATUS

Name	R/W	Bit	After Reset	Function
Reserved	R	31:20	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCH3_RESERVE	R	19	0	Indicates the status of DMA transfer reservation on ACPU LCH3. 0: Not reserved, 1: Reserved
ARM_LCH2_RESERVE	R	18	0	Indicates the status of DMA transfer reservation on ACPU LCH2. 0: Not reserved, 1: Reserved
ARM_LCH1_RESERVE	R	17	0	Indicates the status of DMA transfer reservation on ACPU LCH1. 0: Not reserved, 1: Reserved
ARM_LCH0_RESERVE	R	16	0	Indicates the status of DMA transfer reservation on ACPU LCH0. 0: Not reserved, 1: Reserved
Reserved	R	15:4	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCH3_CONTSTATUS	R	3	0	Indicates the status of DMA transfer on ACPU LCH3. 0: DMA is inactive, 1: DMA is active
ARM_LCH2_CONTSTATUS	R	2	0	Indicates the status of DMA transfer on ACPU LCH2. 0: DMA is inactive, 1: DMA is active
ARM_LCH1_CONTSTATUS	R	1	0	Indicates the status of DMA transfer on ACPU LCH1. 0: DMA is inactive, 1: DMA is active
ARM_LCH0_CONTSTATUS	R	0	0	Indicates the status of DMA transfer on ACPU LCH0. 0: DMA is inactive, 1: DMA is active

(3) ACPU DMA end control register

This register (DMA_ARM_END: 4009_0008H) controls whether to force DMA transfer to end.

If DMA transfer is forcibly terminated, a reservation for the next transfer becomes invalid. If this register is set up, forced termination takes effect when the current AHB transaction is completed. Therefore, DMA transfer cannot be restarted until the AHB transaction ends. If DMA transfer is forcibly stopped, be sure to read the relevant DMA control register to confirm that the relevant DMA status bit has been cleared to 0 before restarting DMA by setting the DMA transfer start bit.

Once DMA starts, at least one DMA write transfer transaction must be performed before executing forced termination; otherwise, parameters are not updated in the internal circuits and thus DMA transfer is not executed correctly.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				ARM_LCH3_END	ARM_LCH2_END	ARM_LCH1_END	ARM_LCH0_END

Name	R/W	Bit	After Reset	Function
Reserved	R	31:4	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCH3_END	W	3	0	Forcibly stops LCH3 DMA transfer for the ACPU.
ARM_LCH2_END	W	2	0	Forcibly stops LCH2 DMA transfer for the ACPU.
ARM_LCH1_END	W	1	0	Forcibly stops LCH1 DMA transfer for the ACPU.
ARM_LCH0_END	W	0	0	Forcibly stops LCH0 DMA transfer for the ACPU.

Remark 0: Retains the current status, 1: Forces DMA transfer to end

2.3.2 ACPU and ADSP interrupt parameter setting registers

These registers specify the parameters for three types of interrupts - length transfer end, block transfer end, and error end.

(1) ACPU and ADSP interrupt status register

These registers (DMA_ARM_XXX_LCH0LCH3_INT_CONT) indicate the interrupt source statuses.
Separate source registers are provided for the AHB write side (*_W_*) and the AHB read side (*_R_*).

Remark The ACPU and ADSP each have their dedicated registers, and the ARM_LCHx_INT_SEL register is used to select which processor to use.

- DMA_ARM_PE0_LCH0LCH3_INT_CONT: 4009_0100H (ACPU)
- DMA_ARM_DSP_LCH0LCH3_INT_CONT: 4009_0400H (ADSP)

31	30	29	28	27	26	25	24
Reserved	ARM_LCH3_INT_ERROR_W_CONT	ARM_LCH3_INT_BLOCK_W_CONT	ARM_LCH3_INT_LENG_W_CONT	Reserved	ARM_LCH3_INT_ERROR_R_CONT	Reserved	

23	22	21	20	19	18	17	16
Reserved	ARM_LCH2_INT_ERROR_W_CONT	ARM_LCH2_INT_BLOCK_W_CONT	ARM_LCH2_INT_LENG_W_CONT	Reserved	ARM_LCH2_INT_ERROR_R_CONT	Reserved	

15	14	13	12	11	10	9	8
Reserved	ARM_LCH1_INT_ERROR_W_CONT	ARM_LCH1_INT_BLOCK_W_CONT	ARM_LCH1_INT_LENG_W_CONT	Reserved	ARM_LCH1_INT_ERROR_R_CONT	Reserved	

7	6	5	4	3	2	1	0
Reserved	ARM_LCH0_INT_ERROR_W_CONT	ARM_LCH0_INT_BLOCK_W_CONT	ARM_LCH0_INT_LENG_W_CONT	Reserved	ARM_LCH0_INT_ERROR_R_CONT	Reserved	

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	–	31	–	Reserved. When this bit is read, 0 is returned.
ARM_LCH3_INT_ERROR_W_CONT	R	30	0	Indicates the status of the interrupt source generated upon an ACPU and ADSP LCH3 error.
ARM_LCH3_INT_BLOCK_W_CONT	R	29	0	Indicates the status of the interrupt source generated upon completion of ACPU and ADSP LCH3 block transfer.
ARM_LCH3_INT_LENG_W_CONT	R	28	0	Indicates the status of the interrupt source generated upon completion of ACPU and ADSP LCH3 length transfer.
Reserved	–	27	–	Reserved. When this bit is read, 0 is returned.
ARM_LCH3_INT_ERROR_R_CONT	R	26	0	Indicates the status of the interrupt source generated upon an ACPU and ADSP LCH3 error.

Remark 0: No interrupt source (default), 1: Interrupt source occurred

(2/2)

Name	R/W	Bit	After Reset	Function
Reserved	–	25:23	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCH2_INT_ ERROR_W_CONT	R	22	0	Indicates the status of the interrupt source generated upon an ACPU and ADSP LCH2 error.
ARM_LCH2_INT_ BLOCK_W_CONT	R	21	0	Indicates the status of the interrupt source generated upon completion of ACPU and ADSP LCH2 block transfer.
ARM_LCH2_INT_ LENG_W_CONT	R	20	0	Indicates the status of the interrupt source generated upon completion of ACPU and ADSP LCH2 length transfer.
Reserved	–	19	–	Reserved. When this bit is read, 0 is returned.
ARM_LCH2_INT_ ERROR_R_CONT	R	18	0	Indicates the status of the interrupt source generated upon an ACPU and ADSP LCH2 error.
Reserved	–	17:15	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCH1_INT_ ERROR_W_CONT	R	14	0	Indicates the status of the interrupt source generated upon an ACPU and ADSP LCH1 error.
ARM_LCH1_INT_ BLOCK_W_CONT	R	13	0	Indicates the status of the interrupt source generated upon completion of ACPU and ADSP LCH1 block transfer.
ARM_LCH1_INT_ LENG_W_CONT	R	12	0	Indicates the status of the interrupt source generated upon completion of ACPU and ADSP LCH1 length transfer.
Reserved	–	11	–	Reserved. When this bit is read, 0 is returned.
ARM_LCH1_INT_ ERROR_R_CONT	R	10	0	Indicates the status of the interrupt source generated upon an ACPU and ADSP LCH1 error.
Reserved	–	9:7	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCH0_INT_ ERROR_W_CONT	R	6	0	Indicates the status of the interrupt source generated upon an ACPU and ADSP LCH0 error.
ARM_LCH0_INT_ BLOCK_W_CONT	R	5	0	Indicates the status of the interrupt source generated upon completion of ACPU and ADSP LCH0 block transfer.
ARM_LCH0_INT_ LENG_W_CONT	R	4	0	Indicates the status of the interrupt source generated upon completion of ACPU and ADSP LCH0 length transfer.
Reserved	–	3	–	Reserved. When this bit is read, 0 is returned.
ARM_LCH0_INT_ ERROR_R_CONT	R	2	0	Indicates the status of the interrupt source generated upon an ACPU and ADSP LCH0 error.
Reserved	–	1:0	–	Reserved. When these bits are read, 0 is returned for each bit.

Remark 0: No interrupt source (default), 1: Interrupt source occurred

(2) ACPU and ADSP interrupt raw status register

These registers (DMA_ARM_XXX_LCH0LCH3_INT_RAW) can be used to read the status of the interrupt sources regardless of the settings of the interrupt enable set register and the interrupt enable clear register. Separate source registers are provided for the AHB write side (*_W_*) and the AHB read side (*_R_*).

Remark The ACPU and ADSP each have their dedicated registers, and the ARM_LCHx_INT_SEL register is used to select which processor to use.

- DMA_ARM_PE0_LCH0LCH3_INT_RAW: 4009_0104H (ACPU)
- DMA_ARM_DSP_LCH0LCH3_INT_RAW: 4009_0404H (ADSP)

31	30	29	28	27	26	25	24
Reserved	ARM_LCH3_INT_ERROR_W_RAW	ARM_LCH3_INT_BLOCK_W_RAW	ARM_LCH3_INT_LENG_W_RAW	Reserved	ARM_LCH3_INT_ERROR_R_RAW	Reserved	
23	22	21	20	19	18	17	16
Reserved	ARM_LCH2_INT_ERROR_W_RAW	ARM_LCH2_INT_BLOCK_W_RAW	ARM_LCH2_INT_LENG_W_RAW	Reserved	ARM_LCH2_INT_ERROR_R_RAW	Reserved	
15	14	13	12	11	10	9	8
Reserved	ARM_LCH1_INT_ERROR_W_RAW	ARM_LCH1_INT_BLOCK_W_RAW	ARM_LCH1_INT_LENG_W_RAW	Reserved	ARM_LCH1_INT_ERROR_R_RAW	Reserved	
7	6	5	4	3	2	1	0
Reserved	ARM_LCH0_INT_ERROR_W_RAW	ARM_LCH0_INT_BLOCK_W_RAW	ARM_LCH0_INT_LENG_W_RAW	Reserved	ARM_LCH0_INT_ERROR_R_RAW	Reserved	

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	–	31	–	Reserved. When this bit is read, 0 is returned.
ARM_LCH3_INT_ERROR_W_RAW	R	30	0	Indicates the status of the interrupt source generated upon an ACPU and ADSP LCH3 error.
ARM_LCH3_INT_BLOCK_W_RAW	R	29	0	Indicates the status of the interrupt source generated upon completion of ACPU and ADSP LCH3 block transfer.
ARM_LCH3_INT_LENG_W_RAW	R	28	0	Indicates the status of the interrupt source generated upon completion of ACPU and ADSP LCH3 length transfer.
Reserved	–	27	–	Reserved. When this bit is read, 0 is returned.
ARM_LCH3_INT_ERROR_R_RAW	R	26	0	Indicates the status of the interrupt source generated upon an ACPU and ADSP LCH3 error.
Reserved	–	25:23	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCH2_INT_ERROR_W_RAW	R	22	0	Indicates the status of the interrupt source generated upon an ACPU and ADSP LCH2 error.

Remark 0: No interrupt source (default), 1: Interrupt source occurred

(2/2)

Name	R/W	Bit	After Reset	Function
ARM_LCH2_INT_ BLOCK_W_RAW	R	21	0	Indicates the status of the interrupt source generated upon completion of ACPU and ADSP LCH2 block transfer.
ARM_LCH2_INT_ LENG_W_RAW	R	20	0	Indicates the status of the interrupt source generated upon completion of ACPU and ADSP LCH2 length transfer.
Reserved	–	19	–	Reserved. When this bit is read, 0 is returned.
ARM_LCH2_INT_ ERROR_R_RAW	R	18	0	Indicates the status of the interrupt source generated upon an ACPU and ADSP LCH2 error.
Reserved	–	17:15	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCH1_INT_ ERROR_W_RAW	R	14	0	Indicates the status of the interrupt source generated upon an ACPU and ADSP LCH1 error.
ARM_LCH1_INT_ BLOCK_W_RAW	R	13	0	Indicates the status of the interrupt source generated upon completion of ACPU and ADSP LCH1 block transfer.
ARM_LCH1_INT_ LENG_W_RAW	R	12	0	Indicates the status of the interrupt source generated upon completion of ACPU and ADSP LCH1 length transfer.
Reserved	–	11	–	Reserved. When this bit is read, 0 is returned.
ARM_LCH1_INT_ ERROR_R_RAW	R	10	0	Indicates the status of the interrupt source generated upon an ACPU and ADSP LCH1 error.
Reserved	–	9:7	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCH0_INT_ ERROR_W_RAW	R	6	0	Indicates the status of the interrupt source generated upon an ACPU and ADSP LCH0 error.
ARM_LCH0_INT_ BLOCK_W_RAW	R	5	0	Indicates the status of the interrupt source generated upon completion of ACPU and ADSP LCH0 block transfer.
ARM_LCH0_INT_ LENG_W_RAW	R	4	0	Indicates the status of the interrupt source generated upon completion of ACPU and ADSP LCH0 length transfer.
Reserved	–	3	–	Reserved. When this bit is read, 0 is returned.
ARM_LCH0_INT_ ERROR_R_RAW	R	2	0	Indicates the status of the interrupt source generated upon an ACPU and ADSP LCH0 error.
Reserved	–	1:0	–	Reserved. When these bits are read, 0 is returned for each bit.

Remark 0: No interrupt source (default), 1: Interrupt source occurred

(3) ACPU and ADSP interrupt enable set register

These registers (DMA_ARM_*XXX*_LCH0LCH3_INT_ENABLE) enable interrupt sources. Only data of bits to which 1 is written is updated. Masking of interrupt sources corresponding to bits to which 1 is written is cancelled.

The interrupt enable status can be checked by reading this register. Writing 0 to this register does not affect the setting.

To mask an interrupt source, set the corresponding bit of the interrupt enable clear register to 1.

Remark The ACPU and ADSP each have their dedicated registers, and the ARM_LCHx_INT_SEL register is used to select which processor to use.

- DMA_ARM_PE0_LCH0LCH3_INT_ENABLE: 4009_0108H (ACPU)
- DMA_ARM_DSP_LCH0LCH3_INT_ENABLE: 4009_0408H (ADSP)

31	30	29	28	27	26	25	24
Reserved					ARM_LCH3_INT_ERROR_ENABLE	ARM_LCH3_INT_BLOCK_ENABLE	ARM_LCH3_INT_LENG_ENABLE

23	22	21	20	19	18	17	16
Reserved					ARM_LCH2_INT_ERROR_ENABLE	ARM_LCH2_INT_BLOCK_ENABLE	ARM_LCH2_INT_LENG_ENABLE

15	14	13	12	11	10	9	8
Reserved					ARM_LCH1_INT_ERROR_ENABLE	ARM_LCH1_INT_BLOCK_ENABLE	ARM_LCH1_INT_LENG_ENABLE

7	6	5	4	3	2	1	0
Reserved					ARM_LCH0_INT_ERROR_ENABLE	ARM_LCH0_INT_BLOCK_ENABLE	ARM_LCH0_INT_LENG_ENABLE

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	–	31:27	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCH3_INT_ERROR_ENABLE	R/W	26	0	Enables the ACPU and ADSP LCH3 error interrupt source.
ARM_LCH3_INT_BLOCK_ENABLE	R/W	25	0	Enables the ACPU and ADSP LCH3 block interrupt source.
ARM_LCH3_INT_LENG_ENABLE	R/W	24	0	Enables the ACPU and ADSP LCH3 length interrupt source.
Reserved	–	23:19	–	Reserved. When these bits are read, 0 is returned for each bit.

Remark 0: Disables the interrupt source (default), 1: Enables the interrupt source

(2/2)

Name	R/W	Bit	After Reset	Function
ARM_LCH2_INT_ ERROR_ENABLE	R/W	18	0	Enables the ACPU and ADSP LCH2 error interrupt source.
ARM_LCH2_INT_ BLOCK_ENABLE	R/W	17	0	Enables the ACPU and ADSP LCH2 block interrupt source.
ARM_LCH2_INT_ LENG_ENABLE	R/W	16	0	Enables the ACPU and ADSP LCH2 length interrupt source.
Reserved	–	15:11	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCH1_INT_ ERROR_ENABLE	R/W	10	0	Enables the ACPU and ADSP LCH1 error interrupt source.
ARM_LCH1_INT_ B LOCK_ENABLE	R/W	9	0	Enables the ACPU and ADSP LCH1 block interrupt source.
ARM_LCH1_INT_ LENG_ENABLE	R/W	8	0	Enables the ACPU and ADSP LCH1 length interrupt source.
Reserved	–	7:3	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCH0_INT_ ERROR_ENABLE	R/W	2	0	Enables the ACPU and ADSP LCH0 error interrupt source.
ARM_LCH0_INT_ BLOCK_ENABLE	R/W	1	0	Enables the ACPU and ADSP LCH0 block interrupt source.
ARM_LCH0_INT_ LENG_ENABLE	R/W	0	0	Enables the ACPU and ADSP LCH0 length interrupt source.

Remark 0: Disables the interrupt source (default), 1: Enables the interrupt source

(4) ACPU and ADSP interrupt enable clear registers

These registers (DMA_ARM_*XXX*_LCH0LCH3_INT_ENABLE_CL) mask interrupt sources.

If a bit of these registers is set to 1, the corresponding interrupt source is disabled. The bits to which 0 is written retain the current settings.

If interrupt sources are disabled in these registers, the corresponding bits in the ARM interrupt enable set register is set to 0 (masks the interrupt sources).

Remark The ACPU and ADSP each have their dedicated registers, and the ARM_LCHx_INT_SEL register is used to select which processor to use.

- DMA_ARM_PE0_LCH0LCH3_INT_ENABLE_CL: 4009_010CH (ACPU)
- DMA_ARM_DSP_LCH0LCH3_INT_ENABLE_CL: 4009_040CH (ADSP)

31	30	29	28	27	26	25	24
Reserved					ARM_LCH3_INT_ERROR_ENABLE_CL	ARM_LCH3_INT_BLOCK_ENABLE_CL	ARM_LCH3_INT_LENG_ENABLE_CL

23	22	21	20	19	18	17	16
Reserved					ARM_LCH2_INT_ERROR_ENABLE_CL	ARM_LCH2_INT_BLOCK_ENABLE_CL	ARM_LCH2_INT_LENG_ENABLE_CL

15	14	13	12	11	10	9	8
Reserved					ARM_LCH1_INT_ERROR_ENABLE_CL	ARM_LCH1_INT_BLOCK_ENABLE_CL	ARM_LCH1_INT_LENG_ENABLE_CL

7	6	5	4	3	2	1	0
Reserved					ARM_LCH0_INT_ERROR_ENABLE_CL	ARM_LCH0_INT_BLOCK_ENABLE_CL	ARM_LCH0_INT_LENG_ENABLE_CL

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	–	31:27	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCH3_INT_ERROR_ENABLE_CL	W	26	0	Disables the ACPU and ADSP LCH3 error interrupt source.
ARM_LCH3_INT_BLOCK_ENABLE_CL	W	25	0	Disables the ACPU and ADSP LCH3 block interrupt source.
ARM_LCH3_INT_LENG_ENABLE_CL	W	24	0	Disables the ACPU and ADSP LCH3 length interrupt source.
Reserved	–	23:19	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCH2_INT_ERROR_ENABLE_CL	W	18	0	Disables the ACPU and ADSP LCH2 error interrupt source.

(2/2)

Name	R/W	Bit	After Reset	Function
ARM_LCH2_INT_ BLOCK_ENABLE_CL	W	17	0	Disables the ACPU and ADSP LCH2 block interrupt source.
ARM_LCH2_INT_ LENG_ENABLE_CL	W	16	0	Disables the ACPU and ADSP LCH2 length interrupt source.
Reserved	–	15:11	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCH1_INT_ ERROR_ENABLE_CL	W	10	0	Disables the ACPU and ADSP LCH1 error interrupt source.
ARM_LCH1_INT_ BLOCK_ENABLE_CL	W	9	0	Disables the ACPU and ADSP LCH1 block interrupt source.
ARM_LCH1_INT_ LENG_ENABLE_CL	W	8	0	Disables the ACPU and ADSP LCH1 length interrupt source.
Reserved	–	7:3	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCH0_INT_ ERROR_ENABLE_CL	W	2	0	Disables the ACPU and ADSP LCH0 error interrupt source.
ARM_LCH0_INT_ BLOCK_ENABLE_CL	W	1	0	Disables the ACPU and ADSP LCH0 block interrupt source.
ARM_LCH0_INT_ LENG_ENABLE_CL	W	0	0	Disables the ACPU and ADSP LCH0 length interrupt source.

Remark 0: Enables the interrupt source (default), 1: Disables the interrupt source

(5) ACPU and ADSP interrupt source clear registers

These registers (DMA_ARM_*XXX*_LCH0LCH3_INT_REQ_CL) clear the interrupt sources. Only data of bits to which 1 is written is updated.

Separate source registers are provided for the AHB write side (*_W_*) and the AHB read side (*_R_*).

Remark The ACPU and ADSP each have their dedicated registers, and the ARM_LCHx_INT_SEL register is used to select which processor to use.

- DMA_ARM_PE0_LCH0LCH3_INT_REQ_CL: 4009_0110H (ACPU)
- DMA_ARM_DSP_LCH0LCH3_INT_REQ_CL: 4009_0410H (ADSP)

31	30	29	28	27	26	25	24
Reserved	ARM_LCH3_INT_ERROR_W_REQ_CL	ARM_LCH3_INT_BLOCK_W_REQ_CL	ARM_LCH3_INT_LENG_W_REQ_CL	Reserved	ARM_LCH3_INT_ERROR_R_REQ_CL	Reserved	

23	22	21	20	19	18	17	16
Reserved	ARM_LCH2_INT_ERROR_W_REQ_CL	ARM_LCH2_INT_BLOCK_W_REQ_CL	ARM_LCH2_INT_LENG_W_REQ_CL	Reserved	ARM_LCH2_INT_ERROR_R_REQ_CL	Reserved	

15	14	13	12	11	10	9	8
Reserved	ARM_LCH1_INT_ERROR_W_REQ_CL	ARM_LCH1_INT_BLOCK_W_REQ_CL	ARM_LCH1_INT_LENG_W_REQ_CL	Reserved	ARM_LCH1_INT_ERROR_R_REQ_CL	Reserved	

7	6	5	4	3	2	1	0
Reserved	ARM_LCH0_INT_ERROR_W_REQ_CL	ARM_LCH0 INT_BLOCK_W_REQ_CL	ARM_LCH0 INT_LENG_W_REQ_CL	Reserved	ARM_LCH0_INT_ERROR_R_REQ_CL	Reserved	

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	–	31	–	Reserved. When this bit is read, 0 is returned.
ARM_LCH3_INT_ERROR_W_REQ_CL	W	30	0	Clears the ACPU and ADSP LCH3 error interrupt source.
ARM_LCH3_INT_BLOCK_W_REQ_CL	W	29	0	Clears the ACPU and ADSP LCH3 block interrupt source.
ARM_LCH3_INT_LENG_W_REQ_CL	W	28	0	Clears the ACPU and ADSP LCH3 length interrupt source.
Reserved	–	27	–	Reserved. When this bit is read, 0 is returned.
ARM_LCH3_INT_ERROR_R_REQ_CL	W	26	0	Clears the ACPU and ADSP LCH3 error interrupt source.
Reserved	–	25:23	–	Reserved. When these bits are read, 0 is returned for each bit.

Remark 0: No operation (retains the current setting), 1: Clears the interrupt source

(2/2)

Name	R/W	Bit	After Reset	Function
ARM_LCH2_INT_ ERROR_W_REQ_CL	W	22	0	Clears the ACPU and ADSP LCH2 error interrupt source.
ARM_LCH2_INT_ BLOCK_W_REQ_CL	W	21	0	Clears the ACPU and ADSP LCH2 block interrupt source.
ARM_LCH2_INT_ LENG_W_REQ_CL	W	20	0	Clears the ACPU and ADSP LCH2 length interrupt source.
Reserved	–	19	–	Reserved. When this bit is read, 0 is returned.
ARM_LCH2_INT_ ERROR_R_REQ_CL	W	18	0	Clears the ACPU and ADSP LCH2 error interrupt source.
Reserved	–	17:15	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCH1_INT_ ERROR_W_REQ_CL	W	14	0	Clears the ACPU and ADSP LCH1 error interrupt source.
ARM_LCH1_INT_ BLOCK_W_REQ_CL	W	13	0	Clears the ACPU and ADSP LCH1 block interrupt source.
ARM_LCH1_INT_ LENG_W_REQ_CL	W	12	0	Clears the ACPU and ADSP LCH1 length interrupt source.
Reserved	–	11	–	Reserved. When this bit is read, 0 is returned.
ARM_LCH1_INT_ ERROR_R_REQ_CL	W	10	0	Clears the ACPU and ADSP LCH1 error interrupt source.
Reserved	–	9:7	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCH0_INT_ ERROR_W_REQ_CL	W	6	0	Clears the ACPU and ADSP LCH0 error interrupt source.
ARM_LCH0_INT_ BLOCK_W_REQ_CL	W	5	0	Clears the ACPU and ADSP LCH0 block interrupt source.
ARM_LCH0_INT_ LENG_W_REQ_CL	W	4	0	Clears the ACPU and ADSP LCH0 length interrupt source.
Reserved	–	3	–	Reserved. When this bit is read, 0 is returned.
ARM_LCH0_INT_ ERROR_R_REQ_CL	W	2	0	Clears the ACPU and ADSP LCH0 error interrupt source.
Reserved	–	1:0	–	Reserved. When these bits are read, 0 is returned for each bit.

Remark 0: No operation (retains the current setting), 1: Clears the interrupt source

(6) ACPU and ADSP interrupt output destination setting register

This register (DMA_ARM_LCH0LCH3_INT_SEL: 4009_0800H) specifies the destinations to which interrupt signals are output.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
ARM_LCH3_INT_SEL		ARM_LCH2_INT_SEL		ARM_LCH1_INT_SEL		ARM_LCH0_INT_SEL	

Name	R/W	Bit	After Reset	Function
Reserved	–	31:8	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCH3_INT_SEL	R/W	7:6	0	Specifies the ACPU and ADSP LCH3 interrupt output destination.
ARM_LCH2_INT_SEL	R/W	5:4	0	Specifies the ACPU and ADSP LCH2 interrupt output destination.
ARM_LCH1_INT_SEL	R/W	3:2	0	Specifies the ACPU and ADSP LCH1 interrupt output destination.
ARM_LCH0_INT_SEL	R/W	1:0	0	Specifies the ACPU and ADSP LCH0 interrupt output destination.

Remark 00: ACPU (default), 01: Reserved, 10: Reserved (interrupts are not output), 11: ADSP

2.3.3 ACPU LCHx parameter setting registers

These registers define the settings for each ACPU logical channel. The letter “x” in LCHx represents a channel number, which ranges from 0 to 3.

(1) ACPU LCHx source address registers

These registers (DMA_ARM_LCHx_AADD) specify the transfer source start addresses in byte units.

- DMA_ARM_LCH0_AADD: 4009_1000H (LCH0)
- DMA_ARM_LCH1_AADD: 4009_1100H (LCH1)
- DMA_ARM_LCH2_AADD: 4009_1200H (LCH2)
- DMA_ARM_LCH3_AADD: 4009_1300H (LCH3)

31	30	29	28	27	26	25	24
ARM_LCHx_AADD							
23	22	21	20	19	18	17	16
ARM_LCHx_AADD							
15	14	13	12	11	10	9	8
ARM_LCHx_AADD							
7	6	5	4	3	2	1	0
ARM_LCHx_AADD							

Name	R/W	Bit	After Reset	Function
ARM_LCHx_AADD	R/W	31:0	0	Specifies the ACPU LCHx source address (start address).

(2) ACPU LCHx source address pointer registers

These registers (DMA_ARM_LCHx_AADP) store the transfer source addresses being accessed.

- DMA_ARM_LCH0_AADP: 4009_1004H (LCH0)
- DMA_ARM_LCH1_AADP: 4009_1104H (LCH1)
- DMA_ARM_LCH2_AADP: 4009_1204H (LCH2)
- DMA_ARM_LCH3_AADP: 4009_1304H (LCH3)

31	30	29	28	27	26	25	24
ARM_LCHx_AADP							

23	22	21	20	19	18	17	16
ARM_LCHx_AADP							

15	14	13	12	11	10	9	8
ARM_LCHx_AADP							

7	6	5	4	3	2	1	0
ARM_LCHx_AADP							

Name	R/W	Bit	After Reset	Function
ARM_LCHx_AADP	R	31:0	0	Stores the source address being accessed during transfer via ACPU LCHx.

(3) ACPU LCHx source address offset registers

These registers (DMA_ARM_LCHx_AOFF) specify the offset between blocks on the source side, in byte units. Bit 16 is a sign bit. Setting this bit to 0 adds the specified value and setting this bit to 1 subtracts the specified value.

Up to 65,535 bytes can be specified.

- DMA_ARM_LCH0_AOFF: 4009_1008H (LCH0)
- DMA_ARM_LCH1_AOFF: 4009_1108H (LCH1)
- DMA_ARM_LCH2_AOFF: 4009_1208H (LCH2)
- DMA_ARM_LCH3_AOFF: 4009_1308H (LCH3)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							ARM_LCHx_ASIGN
15	14	13	12	11	10	9	8
ARM_LCHx_AOFF							
7	6	5	4	3	2	1	0
ARM_LCHx_AOFF							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:17	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCHx_ASIGN	R/W	16	0	Specifies an offset added/subtracted to/from the ACPU LCHx on the source side. 0: Adds the address size specified by ARM_LCHx_AOFF to the start address. 1: Subtracts the address size specified by ARM_LCHx_AOFF from the start address.
ARM_LCHx_AOFF	R/W	15:0	0	Indicates the offset (absolute value) between blocks on the ACPU LCHx source side in byte units. 00000000_00000000: 0 bytes (no offset) 00000000_00000001: 1 byte 00000000_00000010: 2 bytes (halfword) 00000000_00000011: 3 bytes 00000000_00000100: 4 bytes (1 word) 00000000_00000101: 5 bytes : 11111111_11111111: 65,535 bytes

(4) ACPU LCHx source block count registers

These registers (DMA_ARM_LCHx_ASIZE_COUNT) operate differently when read and written.

When these registers are written, the number of blocks transferred in a loop during repeat transfer is set. When these registers are read, the remaining number of transfer blocks on the source side is read out. The specified number of blocks is decremented each time block transfer ends, and the remaining count is shown in this register. To perform repeat transfer, the offset must be set to 0 (one-dimensional transfer).

- DMA_ARM_LCH0_ASIZE_COUNT: 4009_1010H (LCH0)
- DMA_ARM_LCH1_ASIZE_COUNT: 4009_1110H (LCH1)
- DMA_ARM_LCH2_ASIZE_COUNT: 4009_1210H (LCH2)
- DMA_ARM_LCH3_ASIZE_COUNT: 4009_1310H (LCH3)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				ARM_LCHx_ASIZE_COUNT			

Name	R/W	Bit	After Reset	Function
Reserved	–	31:6	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCHx_ASIZE_COUNT	R/W	5:0	0	When written: Specifies the number of blocks to be transferred in a loop during repeat transfer on the source side. 000000: 1 block 000001: 2 blocks 000010: 3 blocks 000011: 4 blocks 000100: 5 blocks 000101: 6 blocks 000110: 7 blocks 000111: 8 blocks 001000: 9 blocks : 111111: 64 blocks When read: Indicates the number of remaining transfer blocks on the source side. The value written to this register is set when DMA is started, and the value is decremented each time block transfer ends.

(5) ACPU LCHx destination address registers

These registers (DMA_ARM_LCHx_BADD) specify the transfer destination start addresses in byte units.

- DMA_ARM_LCH0_BADD: 4009_1020H (LCH0)
- DMA_ARM_LCH1_BADD: 4009_1120H (LCH1)
- DMA_ARM_LCH2_BADD: 4009_1220H (LCH2)
- DMA_ARM_LCH3_BADD: 4009_1320H (LCH3)

31	30	29	28	27	26	25	24
ARM_LCHx_BADD							
23	22	21	20	19	18	17	16
ARM_LCHx_BADD							
15	14	13	12	11	10	9	8
ARM_LCHx_BADD							
7	6	5	4	3	2	1	0
ARM_LCHx_BADD							

Name	R/W	Bit	After Reset	Function
ARM_LCHx_BADD	R/W	31:0	0	Specifies the ACPU LCHx destination address (start address).

(6) ACPU LCHx destination address pointer register

These registers (DMA_ARM_LCHx_BADP) store the transfer destination addresses being accessed.

- DMA_ARM_LCH0_BADP: 4009_1024H (LCH0)
- DMA_ARM_LCH1_BADP: 4009_1124H (LCH1)
- DMA_ARM_LCH2_BADP: 4009_1224H (LCH2)
- DMA_ARM_LCH3_BADP: 4009_1324H (LCH3)

31	30	29	28	27	26	25	24
ARM_LCHx_BADP							
23	22	21	20	19	18	17	16
ARM_LCHx_BADP							
15	14	13	12	11	10	9	8
ARM_LCHx_BADP							
7	6	5	4	3	2	1	0
ARM_LCHx_BADP							

Name	R/W	Bit	After Reset	Function
ARM_LCHx_BADP	R	31:0	0	Stores the destination address being accessed during transfer via ACPU LCHx.

(7) ACPU LCHx destination address offset registers

These registers (DMA_ARM_LCHx_BOFF) specify the offset between blocks on the destination side, in byte units. Bit 16 is a sign bit. Setting this bit to 0 adds the specified value and setting this bit to 1 subtracts the specified value.

Up to 65,535 bytes can be specified.

- DMA_ARM_LCH0_BOFF: 4009_1028H (LCH0)
- DMA_ARM_LCH1_BOFF: 4009_1128H (LCH1)
- DMA_ARM_LCH2_BOFF: 4009_1228H (LCH2)
- DMA_ARM_LCH3_BOFF: 4009_1328H (LCH3)

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							ARM_LCHx_BSIGN

15	14	13	12	11	10	9	8
ARM_LCHx_BOFF							

7	6	5	4	3	2	1	0
ARM_LCHx_BOFF							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:17	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCHx_BSIGN	R/W	16	0	Specifies an offset added/subtracted to/from the ACPU LCHx on the destination side. 0: Adds the address size specified by ARM_LCHx_BOFF to the start address. 1: Subtracts the address size specified by ARM_LCHx_BOFF from the start address.
ARM_LCHx_BOFF	R/W	15:0	0	Indicates the offset between blocks on the ACPU LCHx destination side in byte units. 00000000_00000000: 0 bytes (no offset) 00000000_00000001: 1 byte 00000000_00000010: 2 bytes (halfword) 00000000_00000011: 3 bytes 00000000_00000100: 4 bytes (1 word) 00000000_00000101: 5 bytes : 11111111_11111111: 65,535 bytes

(8) ACPU LCHx destination block count registers

These registers (DMA_ARM_LCHx_BSIZE_COUNT) operate differently when read and written.

When these registers are written, the number of blocks transferred in a loop during repeat transfer is set. When these registers are read, the remaining number of transfer blocks on the destination side is read out. The specified number of blocks is decremented each time block transfer ends, and the remaining count is shown in this register. To perform repeat transfer, the offset must be set to 0 (one-dimensional transfer).

- DMA_ARM_LCH0_BSIZE_COUNT: 4009_1030H (LCH0)
- DMA_ARM_LCH1_BSIZE_COUNT: 4009_1130H (LCH1)
- DMA_ARM_LCH2_BSIZE_COUNT: 4009_1230H (LCH2)
- DMA_ARM_LCH3_BSIZE_COUNT: 4009_1330H (LCH3)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved				ARM_LCHx_BSIZE_COUNT			

Name	R/W	Bit	After Reset	Function
Reserved	–	31:6	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCHx_BSIZE_COUNT	R/W	5:0	0	When written: Specifies the number of blocks to be transferred in a loop during repeat transfer on the destination side. 000000: 1 block 000001: 2 blocks 000010: 3 blocks 000011: 4 blocks 000100: 5 blocks 000101: 6 blocks 000110: 7 blocks 000111: 8 blocks 001000: 9 blocks : 111111: 64 blocks When read: Indicates the number of remaining transfer blocks on the destination side. The value written to this register is set when DMA is started, and the value is decremented each time block transfer ends.

(9) ACPU LCHx length registers

These registers (DMA_ARM_LCHx_LENG) specify the total amount of transfer data, in byte units. Up to 16,777,215 bytes can be specified.

If repeat mode is specified in the relevant mode register, infinite-length transfer is specified by setting the corresponding length register to 0.

Do not set these registers to 0 if the repeat mode is not specified. Specifying an offset for infinite-length transfer is prohibited.

- DMA_ARM_LCH0_LENG: 4009_1040H (LCH0)
- DMA_ARM_LCH1_LENG: 4009_1140H (LCH1)
- DMA_ARM_LCH2_LENG: 4009_1240H (LCH2)
- DMA_ARM_LCH3_LENG: 4009_1340H (LCH3)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
ARM_LCHx_LENG							
15	14	13	12	11	10	9	8
ARM_LCHx_LENG							
7	6	5	4	3	2	1	0
ARM_LCHx_LENG							

Name	R/W	Bit	After Reset	Function
Reserved	–	31:24	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCHx_LENG	R/W	23:0	0	Specifies the total amount of data transferred via ACPU LCHx, in byte units. 00000000_00000000_00000000: Infinite-length transfer 00000000_00000000_00000001: 1 byte 00000000_00000000_00000010: 2 bytes 00000000_00000000_00000011: 3 bytes 00000000_00000000_00000100: 4 bytes : 11111111_11111111_11111111: 16,777,215 bytes

(10) ACPU LCHx read length count registers

These registers (DMA_ARM_LCHx_LENG_RCOUNT) store the total amount of transfer data on the source side. The total transfer length is decremented from the length specified by the corresponding length register to indicate the remaining transfer amount.

- DMA_ARM_LCH0_LENG_RCOUNT: 4009_1044H (LCH0)
- DMA_ARM_LCH1_LENG_RCOUNT: 4009_1144H (LCH1)
- DMA_ARM_LCH2_LENG_RCOUNT: 4009_1244H (LCH2)
- DMA_ARM_LCH3_LENG_RCOUNT: 4009_1344H (LCH3)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
ARM_LCHx_LENG_RCOUNT							
15	14	13	12	11	10	9	8
ARM_LCHx_LENG_RCOUNT							
7	6	5	4	3	2	1	0
ARM_LCHx_LENG_RCOUNT							

Name	R/W	Bit	After Reset	Function
Reserved	–	31:24	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCHx_LENG_RCOUNT	R	23:0	0	Specifies the total amount of data transferred via ACPU LCHx, in byte units. 00000000_00000000_00000000: 0 bytes 00000000_00000000_00000001: 1 byte 00000000_00000000_00000010: 2 bytes 00000000_00000000_00000011: 3 bytes 00000000_00000000_00000100: 4 bytes : 11111111_11111111_11111111: 16,777,215 bytes

(11) ACPU LCHx write length count registers

These registers (DMA_ARM_LCHx_LENG_WCOUNT) store the total amount of transfer data on the destination side. The total transfer length is decremented from the length specified by the corresponding length register to indicate the remaining transfer amount.

- DMA_ARM_LCH0_LENG_WCOUNT: 4009_1048H (LCH0)
- DMA_ARM_LCH1_LENG_WCOUNT: 4009_1148H (LCH1)
- DMA_ARM_LCH2_LENG_WCOUNT: 4009_1248H (LCH2)
- DMA_ARM_LCH3_LENG_WCOUNT: 4009_1348H (LCH3)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
ARM_LCHx_LENG_WCOUNT							
15	14	13	12	11	10	9	8
ARM_LCHx_LENG_WCOUNT							
7	6	5	4	3	2	1	0
ARM_LCHx_LENG_WCOUNT							

Name	R/W	Bit	After Reset	Function
Reserved	–	31:24	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCHx_LENG_ WCOUNT	R	23:0	0	Specifies the total amount of data transferred via ACPU LCHx, in byte units. 00000000_00000000_00000000: 0 bytes 00000000_00000000_00000001: 1 byte 00000000_00000000_00000010: 2 bytes 00000000_00000000_00000011: 3 bytes 00000000_00000000_00000100: 4 bytes : 11111111_11111111_11111111: 16,777,215 bytes

(12) ACPU LCHx block size registers

These registers (DMA_ARM_LCHx_SIZE) specify the block size in byte units. Up to 65,535 bytes can be specified.

- DMA_ARM_LCH0_SIZE: 4009_104CH (LCH0)
- DMA_ARM_LCH1_SIZE: 4009_114CH (LCH1)
- DMA_ARM_LCH2_SIZE: 4009_124CH (LCH2)
- DMA_ARM_LCH3_SIZE: 4009_134CH (LCH3)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
ARM_LCHx_SIZE							
7	6	5	4	3	2	1	0
ARM_LCHx_SIZE							

Name	R/W	Bit	After Reset	Function
Reserved	–	31:16	–	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCHx_SIZE	R/W	15:0	0	Specifies the ACPU LCHx transfer block size. 00000000_00000000: Setting prohibited 00000000_00000001: 1 byte 00000000_00000010: 2 bytes (halfword) 00000000_00000011: 3 bytes 00000000_00000100: 4 bytes (1 word) 00000000_00000101: 5 bytes : 11111111_11111111: 65,535 bytes

Cautions 1. Setting “0” in this register may cause a block interrupt to occur continuously. In this case, the normal DMA operation is not guaranteed.

2. To prevent a block interrupt from occurring for each block size, set the block size to the same value as the length. (In this case, a block interrupt and a length interrupt occur simultaneously when DMA transfer is completed.)

(13) ACPU LCHx mode registers

These registers (DMA_ARM_LCHx_MODE) specify transfer modes (endian and repeat).

To perform repeat transfer, the offset must be set to 0 (one-dimensional transfer).

- DMA_ARM_LCH0_MODE: 4009_1050H (LCH0)
- DMA_ARM_LCH1_MODE: 4009_1150H (LCH1)
- DMA_ARM_LCH2_MODE: 4009_1250H (LCH2)
- DMA_ARM_LCH3_MODE: 4009_1350H (LCH3)

31 30	29 28	27 26	25 24
ARM_LCHx_MODE_ ENDI_W_HH	ARM_LCHx_MODE_ ENDI_W_HL	ARM_LCHx_MODE_ ENDI_W_LH	ARM_LCHx_MODE_ ENDI_W_LL

23 22	21 20	19 18	17 16
ARM_LCHx_MODE_ ENDI_R_HH	ARM_LCHx_MODE_ ENDI_R_HL	ARM_LCHx_MODE_ ENDI_R_LH	ARM_LCHx_MODE_ ENDI_R_LL

15 14 13 12 11 10 9	8
Reserved	ARM_LCHx_ BMODE_ REPEAT

7 6 5 4 3 2 1	0
Reserved	ARM_LCHx_ AMODE_ REPEAT

(1/2)

Name	R/W	Bit	After Reset	Function
ARM_LCHx_MODE_ ENDI_W_HH	R/W	31:30	E4H	Specifies the byte lane for writing data to the transfer destination. 00: Byte 0 01: Byte 1 10: Byte 2 11: Byte 3
ARM_LCHx_MODE_ ENDI_W_HL		29:28		
ARM_LCHx_MODE_ ENDI_W_LH		27:26		
ARM_LCHx_MODE_ ENDI_W_LL		25:24		
ARM_LCHx_MODE_ ENDI_R_HH	R/W	23:22	E4H	Specifies the byte lane for reading transfer data from the source side. 00: Byte 0 01: Byte 1 10: Byte 2 11: Byte 3
ARM_LCHx_MODE_ ENDI_R_HL		21:20		
ARM_LCHx_MODE_ ENDI_R_LH		19:18		
ARM_LCHx_MODE_ ENDI_R_LL		17:16		
Reserved	–	15:9	0	Reserved. When these bits are read, 0 is returned for each bit.

(2/2)

Name	R/W	Bit	After Reset	Function
ARM_LCHx_BMODE_REPEAT	R/W	8	0	Specifies the transfer destination to repeat mode. 0: Does not specify repeat mode. 1: Specifies repeat mode.
Reserved	–	7:1	0	Reserved. When these bits are read, 0 is returned for each bit.
ARM_LCHx_AMODE_REPEAT	R/W	0	0	Specifies the transfer source to repeat mode. 0: Does not specify repeat mode. 1: Specifies repeat mode.

2.3.4 M2P DMA control/status registers

(1) M2P DMA start control register

This register (DMA_M2P_CONT: 4009_4000H) controls whether to start DMA transfer on a per-logical channel basis.

If this register is set up while the M2P_LCHx_RESERVE bit of the M2P DMA start control status register is set to 0, the subsequent transfer starts immediately after the current transfer ends (simple reservation). A transfer parameter for the subsequent transfer must be set before using simple reservation. For details, see **3.4.3 Continuous transfer**.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved	M2P_LCH14_CONT	M2P_LCH13_CONT	M2P_LCH12_CONT	Reserved	M2P_LCH10_CONT	M2P_LCH9_CONT	Reserved

7	6	5	4	3	2	1	0
Reserved		M2P_LCH5_CONT	M2P_LCH4_CONT	M2P_LCH3_CONT	M2P_LCH2_CONT	M2P_LCH1_CONT	M2P_LCH0_CONT

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31:15	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH14_CONT	W	14	0	Specifies whether to start DMA transfer on M2P LCH14. (1: Starts DMA transfer.)
M2P_LCH13_CONT	W	13	0	Specifies whether to start DMA transfer on M2P LCH13. (1: Starts DMA transfer.)
M2P_LCH12_CONT	W	12	0	Specifies whether to start DMA transfer on M2P LCH12. (1: Starts DMA transfer.)
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH10_CONT	W	10	0	Specifies whether to start DMA transfer on M2P LCH10. (1: Starts DMA transfer.)
M2P_LCH9_CONT	W	9	0	Specifies whether to start DMA transfer on M2P LCH9. (1: Starts DMA transfer.)
Reserved	W	8:6	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH5_CONT	W	5	0	Specifies whether to start DMA transfer on M2P LCH5. (1: Starts DMA transfer.)
M2P_LCH4_CONT	W	4	0	Specifies whether to start DMA transfer on M2P LCH4. (1: Starts DMA transfer.)
M2P_LCH3_CONT	W	3	0	Specifies whether to start DMA transfer on M2P LCH3. (1: Starts DMA transfer.)

(2/2)

Name	R/W	Bit	After Reset	Function
M2P_LCH2_CONT	W	2	0	Specifies whether to start DMA transfer on M2P LCH2. (1: Starts DMA transfer.)
M2P_LCH1_CONT	W	1	0	Specifies whether to start DMA transfer on M2P LCH1. (1: Starts DMA transfer.)
M2P_LCH0_CONT	W	0	0	Specifies whether to start DMA transfer on M2P LCH0. (1: Starts DMA transfer.)

(2) M2P DMA control status register

This register (DMA_M2P_CONTSTATUS: 4009_4004H) indicates the status of the DMA controller.

The DMA start reservation status register indicates whether DMA transfer has been reserved. If a bit is set to 1, the corresponding LCH has already been reserved for the next transfer, so another reservation cannot be made.

31	30	29	28	27	26	25	24
Reserved	M2P_LCH14_RESERVE	M2P_LCH13_RESERVE	M2P_LCH12_RESERVE	Reserved	M2P_LCH10_RESERVE	M2P_LCH9_RESERVE	Reserved

23	22	21	20	19	18	17	16
Reserved		M2P_LCH5_RESERVE	M2P_LCH4_RESERVE	M2P_LCH3_RESERVE	M2P_LCH2_RESERVE	M2P_LCH1_RESERVE	M2P_LCH0_RESERVE

15	14	13	12	11	10	9	8
Reserved	M2P_LCH14_CONTSTATUS	M2P_LCH13_CONTSTATUS	M2P_LCH12_CONTSTATUS	Reserved	M2P_LCH10_CONTSTATUS	M2P_LCH9_CONTSTATUS	Reserved

7	6	5	4	3	2	1	0
Reserved		M2P_LCH5_CONTSTATUS	M2P_LCH4_CONTSTATUS	M2P_LCH3_CONTSTATUS	M2P_LCH2_CONTSTATUS	M2P_LCH1_CONTSTATUS	M2P_LCH0_CONTSTATUS

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH14_RESERVE	R	30	0	Indicates the status of DMA transfer reservation on M2P LCH14. 0: Not reserved, 1: Reserved
M2P_LCH13_RESERVE	R	29	0	Indicates the status of DMA transfer reservation on M2P LCH13. 0: Not reserved, 1: Reserved
M2P_LCH12_RESERVE	R	28	0	Indicates the status of DMA transfer reservation on M2P LCH12. 0: Not reserved, 1: Reserved
Reserved	R	27	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH10_RESERVE	R	26	0	Indicates the status of DMA transfer reservation on M2P LCH10. 0: Not reserved, 1: Reserved
M2P_LCH9_RESERVE	R	25	0	Indicates the status of DMA transfer reservation on M2P LCH9. 0: Not reserved, 1: Reserved
Reserved	R	24:22	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH5_RESERVE	R	21	0	Indicates the status of DMA transfer reservation on M2P LCH5. 0: Not reserved, 1: Reserved
M2P_LCH4_RESERVE	R	20	0	Indicates the status of DMA transfer reservation on M2P LCH4. 0: Not reserved, 1: Reserved
M2P_LCH3_RESERVE	R	19	0	Indicates the status of DMA transfer reservation on M2P LCH3. 0: Not reserved, 1: Reserved
M2P_LCH2_RESERVE	R	18	0	Indicates the status of DMA transfer reservation on M2P LCH2. 0: Not reserved, 1: Reserved
M2P_LCH1_RESERVE	R	17	0	Indicates the status of DMA transfer reservation on M2P LCH1. 0: Not reserved, 1: Reserved

(2/2)

Name	R/W	Bit	After Reset	Function
M2P_LCH0_RESERVE	R	16	0	Indicates the status of DMA transfer reservation on M2P LCH0. 0: Not reserved, 1: Reserved
Reserved	R	15	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH14_CONTSTATUS	R	14	0	Indicates the status of DMA transfer on M2P LCH14. 0: DMA is inactive, 1: DMA is active
M2P_LCH13_CONTSTATUS	R	13	0	Indicates the status of DMA transfer on M2P LCH13. 0: DMA is inactive, 1: DMA is active
M2P_LCH12_CONTSTATUS	R	12	0	Indicates the status of DMA transfer on M2P LCH12. 0: DMA is inactive, 1: DMA is active
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH10_CONTSTATUS	R	10	0	Indicates the status of DMA transfer on M2P LCH10. 0: DMA is inactive, 1: DMA is active
M2P_LCH9_CONTSTATUS	R	9	0	Indicates the status of DMA transfer on M2P LCH9. 0: DMA is inactive, 1: DMA is active
Reserved	R	8:6	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH5_CONTSTATUS	R	5	0	Indicates the status of DMA transfer on M2P LCH5. 0: DMA is inactive, 1: DMA is active
M2P_LCH4_CONTSTATUS	R	4	0	Indicates the status of DMA transfer on M2P LCH4. 0: DMA is inactive, 1: DMA is active
M2P_LCH3_CONTSTATUS	R	3	0	Indicates the status of DMA transfer on M2P LCH3. 0: DMA is inactive, 1: DMA is active)
M2P_LCH2_CONTSTATUS	R	2	0	Indicates the status of DMA transfer on M2P LCH2. 0: DMA is inactive, 1: DMA is active
M2P_LCH1_CONTSTATUS	R	1	0	Indicates the status of DMA transfer on M2P LCH1. 0: DMA is inactive, 1: DMA is active
M2P_LCH0_CONTSTATUS	R	0	0	Indicates the status of DMA transfer on M2P LCH0. 0: DMA is inactive, 1: DMA is active

(3) M2P DMA end control register

This register (DMA_M2P_END: 4009_4008H) controls whether to force DMA transfer to end.

If DMA transfer is forcibly terminated, a reservation for the next transfer becomes invalid. If this register is set up, forced termination takes effect when the current AHB transaction is completed. Therefore, DMA transfer cannot be restarted until the AHB transaction ends.

Once DMA starts, at least one DMA write transfer transaction must be performed before executing forced termination; otherwise, parameters are not updated in the internal circuits and thus DMA transfer is not executed correctly.

If DMA transfer is forcibly stopped, be sure to read the relevant DMA control register to confirm that the relevant DMA status bit has been cleared to 0 before restarting DMA by setting the DMA transfer start bit.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved	M2P_LCH14_END	M2P_LCH13_END	M2P_LCH12_END	Reserved	M2P_LCH10_END	M2P_LCH9_END	Reserved
7	6	5	4	3	2	1	0
Reserved		M2P_LCH5_END	M2P_LCH4_END	M2P_LCH3_END	M2P_LCH2_END	M2P_LCH1_END	M2P_LCH0_END

Name	R/W	Bit	After Reset	Function
Reserved	R	31:15	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH14_END	W	14	0	Specifies whether to force DMA transfer on M2P LCH14 to end.
M2P_LCH13_END	W	13	0	Specifies whether to force DMA transfer on M2P LCH13 to end.
M2P_LCH12_END	W	12	0	Specifies whether to force DMA transfer on M2P LCH12 to end.
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH10_END	W	10	0	Specifies whether to force DMA transfer on M2P LCH10 to end.
M2P_LCH9_END	W	9	0	Specifies whether to force DMA transfer on M2P LCH9 to end.
Reserved	R	8:6	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH5_END	W	5	0	Specifies whether to force DMA transfer on M2P LCH5 to end.
M2P_LCH4_END	W	4	0	Specifies whether to force DMA transfer on M2P LCH4 to end.
M2P_LCH3_END	W	3	0	Specifies whether to force DMA transfer on M2P LCH3 to end.
M2P_LCH2_END	W	2	0	Specifies whether to force DMA transfer on M2P LCH2 to end.
M2P_LCH1_END	W	1	0	Specifies whether to force DMA transfer on M2P LCH1 to end.
M2P_LCH0_END	W	0	0	Specifies whether to force DMA transfer on M2P LCH0 to end.

Remark 0: Retains the current status, 1: Forces DMA transfer to end

2.3.5 M2P interrupt parameter setting registers

These registers set the parameters for four types of interrupts - length transfer end, block transfer end, error end, and timeout.

(1) M2P interrupt status registers

These registers (DMA_M2P_*XXX*_LCHx_INT_CONT) indicate the interrupt source statuses.
Separate source registers are provided for the AHB write side (*_W_*) and the AHB read side (*_R_*).

Remark The ACPU and ADSP each have their dedicated registers, and the M2P_LCHx_INT_SEL register is used to select which processor to use.

- DMA_M2P_PE0_LCH0LCH3_INT_CONT: 4009_4100H (ACPU, LCH0 to LCH3)
- DMA_M2P_DSP_LCH0LCH3_INT_CONT: 4009_4400H (ADSP, LCH0 to LCH3)
- DMA_M2P_PE0_LCH4LCH5_INT_CONT: 4009_4120H (ACPU, LCH4 to LCH5)
- DMA_M2P_DSP_LCH4LCH5_INT_CONT: 4009_4420H (ADSP, LCH4 to LCH5)
- DMA_M2P_PE0_LCH9LCH10_INT_CONT: 4009_4140H (ACPU, LCH9 to LCH10)
- DMA_M2P_DSP_LCH9LCH10_INT_CONT: 4009_4440H (ADSP, LCH9 to LCH10)
- DMA_M2P_PE0_LCH12LCH14_INT_CONT: 4009_4160H (ACPU, LCH12 to LCH14)
- DMA_M2P_DSP_LCH12LCH14_INT_CONT: 4009_4460H (ADSP, LCH12 to LCH14)

The bit assignment for LCH0 to LCH3 is shown below. The other channels have the same structure. However, the timeout interrupt (INT_TIME) occurs only on LCH0 to LCH2, so the bits assigned to the timeout interrupt are not available for other channels (i.e., they are reserved).

31	30	29	28	27	26	25	24
M2P_LCH3_INT_TIME_W_CONT	M2P_LCH3_INT_ERROR_W_CONT	Reserved	M2P_LCH3_INT_LENG_W_CONT	Reserved	M2P_LCH3_INT_ERROR_R_CONT	Reserved	
23	22	21	20	19	18	17	16
M2P_LCH2_INT_TIME_W_CONT	M2P_LCH2_INT_ERROR_W_CONT	Reserved	M2P_LCH2_INT_LENG_W_CONT	Reserved	M2P_LCH2_INT_ERROR_R_CONT	Reserved	
15	14	13	12	11	10	9	8
M2P_LCH1_INT_TIME_W_CONT	M2P_LCH1_INT_ERROR_W_CONT	Reserved	M2P_LCH1_INT_LENG_W_CONT	Reserved	M2P_LCH1_INT_ERROR_R_CONT	Reserved	
7	6	5	4	3	2	1	0
M2P_LCH0_INT_TIME_W_CONT	M2P_LCH0_INT_ERROR_W_CONT	Reserved	M2P_LCH0_INT_LENG_W_CONT	Reserved	M2P_LCH0_INT_ERROR_R_CONT	Reserved	

Name	R/W	Bit	After Reset	Function
M2P_LCH3_INT_ TIME_W_CONT	R	31	0	Indicates the status of the interrupt source generated upon M2P LCH3 timeout.
M2P_LCH3_INT_ ERROR_W_CONT	R	30	0	Indicates the status of the interrupt source generated upon an M2P LCH3 error.
Reserved	–	29	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH3_INT_ LENG_W_CONT	R	28	0	Indicates the status of the interrupt source generated upon completion of M2P LCH3 length transfer.
Reserved	–	27	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH3_INT_ ERROR_R_CONT	R	26	0	Indicates the status of the interrupt source generated upon an M2P LCH3 error.
Reserved	–	25:24	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH2_INT_ TIME_W_CONT	R	23	0	Indicates the status of the interrupt source generated upon M2P LCH2 timeout.
M2P_LCH2_INT_ ERROR_W_CONT	R	22	0	Indicates the status of the interrupt source generated upon an M2P LCH2 error.
Reserved	–	21	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH2_INT_ LENG_W_CONT	R	20	0	Indicates the status of the interrupt source generated upon completion of M2P LCH2 length transfer.
Reserved	–	19	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH2_INT_ ERROR_R_CONT	R	18	0	Indicates the status of the interrupt source generated upon an M2P LCH2 error.
Reserved	–	17:16	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH1_INT_ TIME_W_CONT	R	15	0	Indicates the status of the interrupt source generated upon M2P LCH1 timeout.
M2P_LCH1_INT_ ERROR_W_CONT	R	14	0	Indicates the status of the interrupt source generated upon an M2P LCH1 error.
Reserved	–	13	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH1_INT_ LENG_W_CONT	R	12	0	Indicates the status of the interrupt source generated upon completion of M2P LCH1 length transfer.
Reserved	–	11	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH1_INT_ ERROR_R_CONT	R	10	0	Indicates the status of the interrupt source generated upon an M2P LCH1 error.
Reserved	–	9:8	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH0_INT_ TIME_W_CONT	R	7	0	Indicates the status of the interrupt source generated upon M2P LCH0 timeout.
M2P_LCH0_INT_ ERROR_W_CONT	R	6	0	Indicates the status of the interrupt source generated upon an M2P LCH0 error.
Reserved	–	5	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH0_INT_ LENG_W_CONT	R	4	0	Indicates the status of the interrupt source generated upon completion of M2P LCH0 length transfer.
Reserved	–	3	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH0_INT_ ERROR_R_CONT	R	2	0	Indicates the status of the interrupt source generated upon an M2P LCH0 error.
Reserved	–	1:0	–	Reserved. When these bits are read, 0 is returned for each bit.

Remark 0: No interrupt source (default), 1: Interrupt source occurred

(2) M2P interrupt raw status registers

These registers (DMA_M2P_*XXX*_LCHx_INT_RAW) can be used to read the status of the interrupt sources regardless of the settings of the interrupt enable set register and the interrupt enable clear register.
Separate source registers are provided for the AHB write side (*_W_*) and the AHB read side (*_R_*).

Remark The ACPU and ADSP each have their dedicated registers, and the M2P_LCHx_INT_SEL register is used to select which processor to use.

- DMA_M2P_PE0_LCH0LCH3_INT_RAW: 4009_4104H (ACPU, LCH0 to LCH3)
- DMA_M2P_DSP_LCH0LCH3_INT_RAW: 4009_4404H (ADSP, LCH0 to LCH3)
- DMA_M2P_PE0_LCH4LCH5_INT_RAW: 4009_4124H (ACPU, LCH4 to LCH5)
- DMA_M2P_DSP_LCH4LCH5_INT_RAW: 4009_4424H (ADSP, LCH4 to LCH5)
- DMA_M2P_PE0_LCH9LCH10_INT_RAW: 4009_4144H (ACPU, LCH9 to LCH10)
- DMA_M2P_DSP_LCH9LCH10_INT_RAW: 4009_4444H (ADSP, LCH9 to LCH10)
- DMA_M2P_PE0_LCH12LCH14_INT_RAW: 4009_4164H (ACPU, LCH12 to LCH14)
- DMA_M2P_DSP_LCH12LCH14_INT_RAW: 4009_4464H (ADSP, LCH12 to LCH14)

The bit assignment for LCH0 to LCH3 is shown below. The other channels have the same structure. However, the timeout interrupt (INT_TIME) occurs only on LCH0 to LCH2, so the bits assigned to the timeout interrupt are not available for other channels (i.e., they are reserved).

31	30	29	28	27	26	25	24
M2P_LCH3_INT_TIME_W_RAW	M2P_LCH3_INT_ERROR_W_RAW	Reserved	M2P_LCH3_INT_LENG_W_RAW	Reserved	M2P_LCH3_INT_ERROR_R_RAW	Reserved	
23	22	21	20	19	18	17	16
M2P_LCH2_INT_TIME_W_RAW	M2P_LCH2_INT_ERROR_W_RAW	Reserved	M2P_LCH2_INT_LENG_W_RAW	Reserved	M2P_LCH2_INT_ERROR_R_RAW	Reserved	
15	14	13	12	11	10	9	8
M2P_LCH1_INT_TIME_W_RAW	M2P_LCH1_INT_ERROR_W_RAW	Reserved	M2P_LCH1_INT_LENG_W_RAW	Reserved	M2P_LCH1_INT_ERROR_R_RAW	Reserved	
7	6	5	4	3	2	1	0
M2P_LCH0_INT_TIME_W_RAW	M2P_LCH0_INT_ERROR_W_RAW	Reserved	M2P_LCH0_INT_LENG_W_RAW	Reserved	M2P_LCH0_INT_ERROR_R_RAW	Reserved	

Name	R/W	Bit	After Reset	Function
M2P_LCH3_INT_ TIME_W_RAW	R	31	0	Indicates the status of the interrupt source generated upon M2P LCH3 timeout.
M2P_LCH3_INT_ ERROR_W_RAW	R	30	0	Indicates the status of the interrupt source generated upon an M2P LCH3 error.
Reserved	–	29	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH3_INT_ LENG_W_RAW	R	28	0	Indicates the status of the interrupt source generated upon completion of M2P LCH3 length transfer.
Reserved	–	27	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH3_INT_ ERROR_R_RAW	R	26	0	Indicates the status of the interrupt source generated upon an M2P LCH3 error.
Reserved	–	25:24	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH2_INT_ TIME_W_RAW	R	23	0	Indicates the status of the interrupt source generated upon M2P LCH2 timeout.
M2P_LCH2_INT_ ERROR_W_RAW	R	22	0	Indicates the status of the interrupt source generated upon an M2P LCH2 error.
Reserved	–	21	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH2_INT_LEN G_W_RAW	R	20	0	Indicates the status of the interrupt source generated upon completion of M2P LCH2 length transfer.
Reserved	–	19	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH2_INT_ ERROR_R_RAW	R	18	0	Indicates the status of the interrupt source generated upon an M2P LCH2 error.
Reserved	–	17:16	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH1_INT_ TIME_W_RAW	R	15	0	Indicates the status of the interrupt source generated upon M2P LCH1 timeout.
M2P_LCH1_INT_ ERROR_W_RAW	R	14	0	Indicates the status of the interrupt source generated upon an M2P LCH1 error.
Reserved	–	13	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH1_INT_ LENG_W_RAW	R	12	0	Indicates the status of the interrupt source generated upon completion of M2P LCH1 length transfer.
Reserved	–	11		Reserved. When this bit is read, 0 is returned.
M2P_LCH1_INT_ ERROR_R_RAW	R	10	0	Indicates the status of the interrupt source generated upon an M2P LCH1 error.
Reserved	–	9:8	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH0_INT_ TIME_W_RAW	R	7	0	Indicates the status of the interrupt source generated upon M2P LCH0 timeout.
M2P_LCH0_INT_ ERROR_W_RAW	R	6	0	Indicates the status of the interrupt source generated upon an M2P LCH0 error.
Reserved	–	5	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH0_INT_ LENG_W_RAW	R	4	0	Indicates the status of the interrupt source generated upon completion of M2P LCH0 length transfer.
Reserved	–	3	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH0_INT_ ERROR_R_RAW	R	2	0	Indicates the status of the interrupt source generated upon an M2P LCH0 error.
Reserved	–	1:0	–	Reserved. When these bits are read, 0 is returned for each bit.

Remark 0: No interrupt source (default), 1: Interrupt source occurred

(3) M2P interrupt enable set registers

These registers (DMA_M2P_*XXX*_LCHx_INT_ENABLE) enable interrupt sources. Only data of bits to which 1 is written is updated.

Masking of interrupt sources corresponding to bits to which 1 is written is cancelled. The interrupt enable status can be checked by reading this register. Writing 0 to this register does not affect the setting.

To mask an interrupt source, set the corresponding bit of the interrupt enable clear register to 1.

Remark The ACPU and ADSP each have their dedicated registers, and the M2P_LCHx_INT_SEL register is used to select which processor to use.

- DMA_M2P_PE0_LCH0LCH3_INT_ENABLE: 4009_4108H (ACPU, LCH0 to LCH3)
- DMA_M2P_DSP_LCH0LCH3_INT_ENABLE: 4009_4408H (ADSP, LCH0 to LCH3)
- DMA_M2P_PE0_LCH4LCH5_INT_ENABLE: 4009_4128H (ACPU, LCH4 to LCH5)
- DMA_M2P_DSP_LCH4LCH5_INT_ENABLE: 4009_4428H (ADSP, LCH4 to LCH5)
- DMA_M2P_PE0_LCH9LCH10_INT_ENABLE: 4009_4148H (ACPU, LCH9 to LCH10)
- DMA_M2P_DSP_LCH9LCH10_INT_ENABLE: 4009_4448H (ADSP, LCH9 to LCH10)
- DMA_M2P_PE0_LCH12LCH14_INT_ENABLE: 4009_4168H (ACPU, LCH12 to LCH14)
- DMA_M2P_DSP_LCH12LCH14_INT_ENABLE: 4009_4468H (ADSP, LCH12 to LCH14)

The bit assignment for LCH0 to LCH3 is shown below. The other channels have the same structure. However, the timeout interrupt (INT_TIME) occurs only on LCH0 to LCH3 and LCH7, so the bits assigned to the timeout interrupt are not available for other channels (i.e., they are reserved).

31	30	29	28	27	26	25	24
Reserved				M2P_LCH3_INT_TIME_ENABLE	M2P_LCH3_INT_ERROR_ENABLE	M2P_LCH3_INT_BLOCK_ENABLE	M2P_LCH3_INT_LENG_ENABLE

23	22	21	20	19	18	17	16
Reserved				M2P_LCH2_INT_TIME_ENABLE	M2P_LCH2_INT_ERROR_ENABLE	M2P_LCH2_INT_BLOCK_ENABLE	M2P_LCH2_INT_LENG_ENABLE

15	14	13	12	11	10	9	8
Reserved				M2P_LCH1_INT_TIME_ENABLE	M2P_LCH1_INT_ERROR_ENABLE	M2P_LCH1_INT_BLOCK_ENABLE	M2P_LCH1_INT_LENG_ENABLE

7	6	5	4	3	2	1	0
Reserved				M2P_LCH0_INT_TIME_ENABLE	M2P_LCH0_INT_ERROR_ENABLE	M2P_LCH0_INT_BLOCK_ENABLE	M2P_LCH0_INT_LENG_ENABLE

Name	R/W	Bit	After Reset	Function
Reserved	–	31:28	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH3_INT_ TIME_ENABLE	R/W	27	0	Enables the M2P LCH3 timeout interrupt source.
M2P_LCH3_INT_ ERROR_ENABLE	R/W	26	0	Enables the M2P LCH3 error interrupt source.
M2P_LCH3_INT_ BLOCK_ENABLE	R/W	25	0	Enables the M2P LCH3 block interrupt source.
M2P_LCH3_INT_ LENG_ENABLE	R/W	24	0	Enables the M2P LCH3 length interrupt source.
Reserved	–	23:20	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH2_INT_ TIME_ENABLE	R/W	19	0	Enables the M2P LCH2 timeout interrupt source.
M2P_LCH2_INT_ ERROR_ENABLE	R/W	18	0	Enables the M2P LCH2 error interrupt source.
M2P_LCH2_INT_ BLOCK_ENABLE	R/W	17	0	Enables the M2P LCH2 block interrupt source.
M2P_LCH2_INT_ LENG_ENABLE	R/W	16	0	Enables the M2P LCH2 length interrupt source.
Reserved	–	15:12	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH1_INT_ TIME_ENABLE	R/W	11	0	Enables the M2P LCH1 timeout interrupt source.
M2P_LCH1_INT_ ERROR_ENABLE	R/W	10	0	Enables the M2P LCH1 error interrupt source.
M2P_LCH1_INT_ BLOCK_ENABLE	R/W	9	0	Enables the M2P LCH1 block interrupt source.
M2P_LCH1_INT_ LENG_ENABLE	R/W	8	0	Enables the M2P LCH1 length interrupt source.
Reserved	–	7:4	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH0_INT_ TIME_ENABLE	R/W	3	0	Enables the M2P LCH0 timeout interrupt source.
M2P_LCH0_INT_ ERROR_ENABLE	R/W	2	0	Enables the M2P LCH0 error interrupt source.
M2P_LCH0_INT_ BLOCK_ENABLE	R/W	1	0	Enables the M2P LCH0 block interrupt source.
M2P_LCH0_INT_ LENG_ENABLE	R/W	0	0	Enables the M2P LCH0 length interrupt source.

Remark 0: Disables the interrupt source (default), 1: Enables the interrupt source

(4) M2P interrupt enable clear registers

These registers (DMA_M2P_*XXX*_LCHx_INT_ENABLE_CL) mask interrupt sources.

If a bit of these registers is set to 1, the corresponding interrupt source is disabled. The bits to which 0 is written retain the current settings.

If interrupt sources are disabled in these registers, the corresponding bits in the ARM interrupt enable set register is set to 0 (masks the interrupt sources).

Remark The ACPU and ADSP each have their dedicated registers, and the M2P_LCHx_INT_SEL register is used to select which processor to use.

- DMA_M2P_PE0_LCH0LCH3_INT_ENABLE_CL: 4009_410CH (ACPU, LCH0 to LCH3)
- DMA_M2P_DSP_LCH0LCH3_INT_ENABLE_CL: 4009_440CH (ADSP, LCH0 to LCH3)
- DMA_M2P_PE0_LCH4LCH5_INT_ENABLE_CL: 4009_412CH (ACPU, LCH4 to LCH5)
- DMA_M2P_DSP_LCH4LCH5_INT_ENABLE_CL: 4009_442CH (ADSP, LCH4 to LCH5)
- DMA_M2P_PE0_LCH9LCH10_INT_ENABLE_CL: 4009_414CH (ACPU, LCH9 to LCH10)
- DMA_M2P_DSP_LCH9LCH10_INT_ENABLE_CL: 4009_444CH (ADSP, LCH9 to LCH10)
- DMA_M2P_PE0_LCH12LCH14_INT_ENABLE_CL: 4009_416CH (ACPU, LCH12 to LCH14)
- MA_M2P_DSP_LCH12LCH14_INT_ENABLE_CL: 4009_446CH (ADSP, LCH12 to LCH14)

The bit assignment for LCH0 to LCH3 is shown below. The other channels have the same structure. However, the timeout interrupt (INT_TIME) occurs only on LCH0 to LCH3 and LCH7, so the bits assigned to the timeout interrupt are not available for other channels (i.e., they are reserved).

31	30	29	28	27	26	25	24
Reserved				M2P_LCH3_INT_TIME_ENABLE_CL	M2P_LCH3_INT_ERROR_ENABLE_CL	M2P_LCH3_INT_BLOCK_ENABLE_CL	M2P_LCH3_INT_LENG_ENABLE_CL

23	22	21	20	19	18	17	16
Reserved				M2P_LCH2_INT_TIME_ENABLE_CL	M2P_LCH2_INT_ERROR_ENABLE_CL	M2P_LCH2_INT_BLOCK_ENABLE_CL	M2P_LCH2_INT_LENG_ENABLE_CL

15	14	13	12	11	10	9	8
Reserved				M2P_LCH1_INT_TIME_ENABLE_CL	M2P_LCH1_INT_ERROR_ENABLE_CL	M2P_LCH1_INT_BLOCK_ENABLE_CL	M2P_LCH1_INT_LENG_ENABLE_CL

7	6	5	4	3	2	1	0
Reserved				M2P_LCH0_INT_TIME_ENABLE_CL	M2P_LCH0_INT_ERROR_ENABLE_CL	M2P_LCH0_INT_BLOCK_ENABLE_CL	M2P_LCH0_INT_LENG_ENABLE_CL

Name	R/W	Bit	After Reset	Function
Reserved	–	31:28	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH3_INT_ TIME_ENABLE_CL	W	27	0	Disables the M2P LCH3 timeout interrupt source.
M2P_LCH3_INT_ ERROR_ENABLE_CL	W	26	0	Disables the M2P LCH3 error interrupt source.
M2P_LCH3_INT_ BLOCK_ENABLE_CL	W	25	0	Disables the M2P LCH3 block interrupt source.
M2P_LCH3_INT_ LENG_ENABLE_CL	W	24	0	Disables the M2P LCH3 length interrupt source.
Reserved	–	23:20	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH2_INT_ TIME_ENABLE_CL	W	19	0	Disables the M2P LCH2 timeout interrupt source.
M2P_LCH2_INT_ ERROR_ENABLE_CL	W	18	0	Disables the M2P LCH2 error interrupt source.
M2P_LCH2_INT_ BLOCK_ENABLE_CL	W	17	0	Disables the M2P LCH2 block interrupt source.
M2P_LCH2_INT_LEN G_ENABLE_CL	W	16	0	Disables the M2P LCH2 length interrupt source.
Reserved	–	15:12	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH1_INT_TIM E_ENABLE_CL	W	11	0	Disables the M2P LCH1 timeout interrupt source.
M2P_LCH1_INT_ ERROR_ENABLE_CL	W	10	0	Disables the M2P LCH1 error interrupt source.
M2P_LCH1_INT_ BLOCK_ENABLE_CL	W	9	0	Disables the M2P LCH1 block interrupt source.
M2P_LCH1_INT_ LENG_ENABLE_CL	W	8	0	Disables the M2P LCH1 length interrupt source.
Reserved	–	7:4	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH0_INT_ TIME_ENABLE_CL	W	3	0	Disables the M2P LCH0 timeout interrupt source.
M2P_LCH0_INT_ ERROR_ENABLE_CL	W	2	0	Disables the M2P LCH0 error interrupt source.
M2P_LCH0_INT_ BLOCK_ENABLE_CL	W	1	0	Disables the M2P LCH0 block interrupt source.
M2P_LCH0_INT_ LENG_ENABLE_CL	W	0	0	Disables the M2P LCH0 length interrupt source.

Remark 0: Disables the interrupt source (default), 1: Enables the interrupt source

(5) M2P interrupt source clear registers

These registers (DMA_M2P_*XXX*_LCHx_INT_REQ_CL) request clearing of interrupt sources. Only data of bits to which 1 is written is updated.

Separate source registers are provided for the AHB write side (*_W_*) and the AHB read side (*_R_*).

Remark The ACPU and ADSP each have their dedicated registers, and the M2P_LCHx_INT_SEL register is used to select which processor to use.

- DMA_M2P_PE0_LCH0LCH3_INT_REQ_CL: 4009_4110H (ACPU, LCH0 to LCH3)
- DMA_M2P_DSP_LCH0LCH3_INT_REQ_CL: 4009_4410H (ADSP, LCH0 to LCH3)
- DMA_M2P_PE0_LCH4LCH5_INT_REQ_CL: 4009_4130H (ACPU, LCH4 to LCH5)
- DMA_M2P_DSP_LCH4LCH5_INT_REQ_CL: 4009_4430H (ADSP, LCH4 to LCH5)
- DMA_M2P_PE0_LCH9LCH10_INT_REQ_CL: 4009_4150H (ACPU, LCH9 to LCH10)
- DMA_M2P_DSP_LCH9LCH10_INT_REQ_CL: 4009_4450H (ADSP, LCH9 to LCH10)
- DMA_M2P_PE0_LCH12LCH14_INT_REQ_CL: 4009_4170H (ACPU, LCH12 to LCH14)
- DMA_M2P_DSP_LCH12LCH14_INT_REQ_CL: 4009_4470H (ADSP, LCH12 to LCH14)

The bit assignment for LCH0 to LCH3 is shown below. The other channels have the same structure. However, the timeout interrupt (INT_TIME) occurs only on LCH0 to LCH3 and LCH7, so the bits assigned to the timeout interrupt are not available for other channels (i.e., they are reserved).

31	30	29	28	27	26	25	24
M2P_LCH3_INT_TIME_W_REQ_CL	M2P_LCH3_INT_ERROR_W_REQ_CL	Reserved	M2P_LCH3_INT_LENG_W_REQ_CL	Reserved	M2P_LCH3_INT_ERROR_R_REQ_CL	Reserved	

23	22	21	20	19	18	17	16
M2P_LCH2_INT_TIME_W_REQ_CL	M2P_LCH2_INT_ERROR_W_REQ_CL	Reserved	M2P_LCH2_INT_LENG_W_REQ_CL	Reserved	M2P_LCH2_INT_ERROR_R_REQ_CL	Reserved	

15	14	13	12	11	10	9	8
M2P_LCH1_INT_TIME_W_REQ_CL	M2P_LCH1_INT_ERROR_W_REQ_CL	Reserved	M2P_LCH1_INT_LENG_W_REQ_CL	Reserved	M2P_LCH1_INT_ERROR_R_REQ_CL	Reserved	

7	6	5	4	3	2	1	0
M2P_LCH0_INT_TIME_W_REQ_CL	M2P_LCH0_INT_ERROR_W_REQ_CL	Reserved	M2P_LCH0_INT_LENG_W_REQ_CL	Reserved	M2P_LCH0_INT_ERROR_R_REQ_CL	Reserved	

(1/2)

Name	R/W	Bit	After Reset	Function
M2P_LCH3_INT_ TIME_W_REQ_CL	W	31	0	Clears the M2P LCH3 timeout interrupt source.
M2P_LCH3_INT_ ERROR_W_REQ_CL	W	30	0	Clears the M2P LCH3 error interrupt source.
Reserved	–	29	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH3_INT_ LENG_W_REQ_CL	W	28	0	Clears the M2P LCH3 length interrupt source.
Reserved	–	27	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH3_INT_ ERROR_R_REQ_CL	W	26	0	Clears the M2P LCH3 error interrupt source.
Reserved	–	25:24	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH2_INT_ TIME_W_REQ_CL	W	23	0	Clears the M2P LCH2 timeout interrupt source.
M2P_LCH2_INT_ ERROR_W_REQ_CL	W	22	0	Clears the M2P LCH2 error interrupt source.
Reserved	–	21	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH2_INT_ LENG_W_REQ_CL	W	20	0	Clears the M2P LCH2 length interrupt source.
Reserved	–	19	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH2_INT_ ERROR_R_REQ_CL	W	18	0	Clears the M2P LCH2 error interrupt source.
Reserved	–	17:16	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH1_INT_ TIME_W_REQ_CL	W	15	0	Clears the M2P LCH1 timeout interrupt source.
M2P_LCH1_INT_ ERROR_W_REQ_CL	W	14	0	Clears the M2P LCH1 error interrupt source.
Reserved	–	13	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH1_INT_ LENG_W_REQ_CL	W	12	0	Clears the M2P LCH1 length interrupt source.
Reserved	–	11	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH1_INT_ ERROR_R_REQ_CL	W	10	0	Clears the M2P LCH1 error interrupt source.
Reserved	–	9:8	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH0_INT_ TIME_W_REQ_CL	W	7	0	Clears the M2P LCH0 timeout interrupt source.
M2P_LCH0_INT_ ERROR_W_REQ_CL	W	6	0	Clears the M2P LCH0 error interrupt source.
Reserved	–	5	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH0_INT_ LENG_W_REQ_CL	W	4	0	Clears the M2P LCH0 length interrupt source.

Remark 0: No operation (retains the current setting), 1: Clears the interrupt source

(2/2)

Name	R/W	Bit	After Reset	Function
Reserved	–	3	–	Reserved. When this bit is read, 0 is returned.
M2P_LCH0_INT_ ERROR_R_REQ_CL	W	2	0	Clears the M2P LCH0 error interrupt source.
Reserved	–	1:0	–	Reserved. When these bits are read, 0 is returned for each bit.

Remark 0: No operation (retains the current setting), 1: Clears the interrupt source

(6) M2P interrupt output destination setting register

This register (DMA_M2P_LCH0LCH14_INT_SEL: 4009_4800H) specifies the destinations to which interrupt signals are output.

31	30	29	28	27	26	25	24
Reserved		M2P_LCH14_INT_SEL		M2P_LCH13_INT_SEL		M2P_LCH12_INT_SEL	
23	22	21	20	19	18	17	16
Reserved		M2P_LCH10_INT_SEL		M2P_LCH9_INT_SEL		Reserved	
15	14	13	12	11	10	9	8
Reserved				M2P_LCH5_INT_SEL		M2P_LCH4_INT_SEL	
7	6	5	4	3	2	1	0
M2P_LCH3 INT_SEL		M2P_LCH2_INT_SEL		M2P_LCH1_INT_SEL		M2P_LCH0_INT_SEL	

Name	R/W	Bit	After Reset	Function
Reserved	–	31:30	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH14_INT_SEL	R/W	29:28	0	Specifies the M2P LCH14 interrupt output destination.
M2P_LCH13_INT_SEL	R/W	27:26	0	Specifies the M2P LCH13 interrupt output destination.
M2P_LCH12_INT_SEL	R/W	25:24	0	Specifies the M2P LCH12 interrupt output destination.
Reserved	–	23:22	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH10_INT_SEL	R/W	21:20	0	Specifies the M2P LCH10 interrupt output destination.
M2P_LCH9_INT_SEL	R/W	19:18	0	Specifies the M2P LCH9 interrupt output destination.
Reserved	–	17:12	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCH5_INT_SEL	R/W	11:10	0	Specifies the M2P LCH5 interrupt output destination.
M2P_LCH4_INT_SEL	R/W	9:8	0	Specifies the M2P LCH4 interrupt output destination.
M2P_LCH3_INT_SEL	R/W	7:6	–	Specifies the M2P LCH3 interrupt output destination.
M2P_LCH2_INT_SEL	R/W	5:4	0	Specifies the M2P LCH2 interrupt output destination.
M2P_LCH1_INT_SEL	R/W	3:2	–	Specifies the M2P LCH1 interrupt output destination.
M2P_LCH0_INT_SEL	R/W	1:0	0	Specifies the M2P LCH0 interrupt output destination.

Remark 00: ACPU (default), 01: Reserved, 10: Reserved, 11: ADSP

2.3.6 M2P LCHx parameter setting registers

These registers define the settings for each M2P logical channel. The letter “x” in LCHx represents a channel number, which ranges from 0 to 14 for M2P.

Channels LCH6 to LCH8 and LCH11 are reserved channels (unused channels).

(1) M2P LCHx source address register

These registers (DMA_M2P_LCHx_AADD) specify the transfer source start addresses in byte units.

- DMA_M2P_LCH0_AADD: 4009_5000H (LCH0)
- DMA_M2P_LCH1_AADD: 4009_5100H (LCH1)
- DMA_M2P_LCH2_AADD: 4009_5200H (LCH2)
- DMA_M2P_LCH3_AADD: 4009_5300H (LCH3)
- DMA_M2P_LCH4_AADD: 4009_5400H (LCH4)
- DMA_M2P_LCH5_AADD: 4009_5500H (LCH5)
- DMA_M2P_LCH9_AADD: 4009_5900H (LCH9)
- DMA_M2P_LCH10_AADD: 4009_5A00H (LCH10)
- DMA_M2P_LCH12_AADD: 4009_5C00H (LCH12)
- DMA_M2P_LCH13_AADD: 4009_5D00H (LCH13)
- DMA_M2P_LCH14_AADD: 4009_5E00H (LCH14)

31	30	29	28	27	26	25	24
M2P_LCHx_AADD							
23	22	21	20	19	18	17	16
M2P_LCHx_AADD							
15	14	13	12	11	10	9	8
M2P_LCHx_AADD							
7	6	5	4	3	2	1	0
M2P_LCHx_AADD							

Name	R/W	Bit	After Reset	Function
M2P_LCHx_AADD	R/W	31:0	0	Specifies the M2P LCHx source address (start address).

(2) M2P LCHx source address pointer register

These registers (DMA_M2P_LCHx_AADP) store the transfer source addresses being accessed.

- DMA_M2P_LCH0_AADP: 4009_5004H (LCH0)
- DMA_M2P_LCH1_AADP: 4009_5104H (LCH1)
- DMA_M2P_LCH2_AADP: 4009_5204H (LCH2)
- DMA_M2P_LCH3_AADP: 4009_5304H (LCH3)
- DMA_M2P_LCH4_AADP: 4009_5404H (LCH4)
- DMA_M2P_LCH5_AADP: 4009_5504H (LCH5)
- DMA_M2P_LCH9_AADP: 4009_5904H (LCH9)
- DMA_M2P_LCH10_AADP: 4009_5A04H (LCH10)
- DMA_M2P_LCH12_AADP: 4009_5C04H (LCH12)
- DMA_M2P_LCH13_AADP: 4009_5D04H (LCH13)
- DMA_M2P_LCH14_AADP: 4009_5E04H (LCH14)

31	30	29	28	27	26	25	24
M2P_LCHx_AADP							
23	22	21	20	19	18	17	16
M2P_LCHx_AADP							
15	14	13	12	11	10	9	8
M2P_LCHx_AADP							
7	6	5	4	3	2	1	0
M2P_LCHx_AADP							

Name	R/W	Bit	After Reset	Function
M2P_LCHx_AADP	R	31:0	0	Stores the source address being accessed during transfer via M2P LCHx.

(3) M2P LCHx source address offset register

These registers (DMA_M2P_LCHx_AOFF) specify the offset between blocks on the source side, in byte units. Up to 65,535 bytes can be specified.

- DMA_M2P_LCH0_AOFF: 4009_5008H (LCH0)
- DMA_M2P_LCH1_AOFF: 4009_5108H (LCH1)
- DMA_M2P_LCH2_AOFF: 4009_5208H (LCH2)
- DMA_M2P_LCH3_AOFF: 4009_5308H (LCH3)
- DMA_M2P_LCH4_AOFF: 4009_5408H (LCH4)
- DMA_M2P_LCH5_AOFF: 4009_5508H (LCH5)
- DMA_M2P_LCH9_AOFF: 4009_5908H (LCH9)
- DMA_M2P_LCH10_AOFF: 4009_5A08H (LCH10)
- DMA_M2P_LCH12_AOFF: 4009_5C08H (LCH12)
- DMA_M2P_LCH13_AOFF: 4009_5D08H (LCH13)
- DMA_M2P_LCH14_AOFF: 4009_5E08H (LCH14)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
M2P_LCHx_AOFF							
7	6	5	4	3	2	1	0
M2P_LCHx_AOFF							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:16	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCHx_AOFF	R/W	15:0	0	Indicates the offset between blocks on the M2P LCHx source side in byte units. 00000000_00000000: 0 bytes (no offset) 00000000_00000001: 1 byte 00000000_00000010: 2 bytes (halfword) 00000000_00000011: 3 bytes 00000000_00000100: 4 bytes (1 word) 00000000_00000101: 5 bytes : 11111111_11111111: 65,535 bytes

(4) M2P LCHx source block size register

These registers (DMA_M2P_LCHx_ASIZE) specify the size of the transfer blocks on the source side, in byte units. Up to 65,535 bytes can be specified.

- DMA_M2P_LCH0_ASIZE: 4009_500CH (LCH0)
- DMA_M2P_LCH1_ASIZE: 4009_510CH (LCH1)
- DMA_M2P_LCH2_ASIZE: 4009_520CH (LCH2)
- DMA_M2P_LCH3_ASIZE: 4009_530CH (LCH3)
- DMA_M2P_LCH4_ASIZE: 4009_540CH (LCH4)
- DMA_M2P_LCH5_ASIZE: 4009_550CH (LCH5)
- DMA_M2P_LCH9_ASIZE: 4009_590CH (LCH9)
- DMA_M2P_LCH10_ASIZE: 4009_5A0CH (LCH10)
- DMA_M2P_LCH12_ASIZE: 4009_5C0CH (LCH12)
- DMA_M2P_LCH13_ASIZE: 4009_5D0CH (LCH13)
- DMA_M2P_LCH14_ASIZE: 4009_5E0CH (LCH14)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
M2P_LCHx_ASIZE							
7	6	5	4	3	2	1	0
M2P_LCHx_ASIZE							

Name	R/W	Bit	After Reset	Function
Reserved	–	31:16	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCHx_ASIZE	R/W	15:0	0	Specifies the size of M2P LCHx transfer blocks on the source side. 00000000_00000000: Setting prohibited 00000000_00000001: 1 byte 00000000_00000010: 2 bytes (halfword) 00000000_00000011: 3 bytes 00000000_00000100: 4 bytes (1 word) 00000000_00000101: 5 bytes : 11111111_11111111: 65,535 bytes

Cautions 1. Setting "0" in this register may cause a block interrupt to occur continuously. In this case, the normal DMA operation is not guaranteed.

2. To prevent a block interrupt from occurring for each block size, set the block size to the same value as the length. (In this case, a block interrupt and a length interrupt occur simultaneously when DMA transfer is completed.)

(5) M2P LCHx source block count registers

These registers (DMA_M2P_LCHx_ASIZE_COUNT) operate differently when read and written.

When these registers are written, the number of blocks transferred in a loop during repeat transfer is set. When these registers are read, the remaining number of transfer blocks on the source side is read out. The specified number of blocks is decremented each time block transfer ends, and the remaining count is shown in this register. To perform repeat transfer, the offset must be set to 0 (one-dimensional transfer).

- DMA_M2P_LCH0_ASIZE_COUNT: 4009_5010H (LCH0)
- DMA_M2P_LCH1_ASIZE_COUNT: 4009_5110H (LCH1)
- DMA_M2P_LCH2_ASIZE_COUNT: 4009_5210H (LCH2)
- DMA_M2P_LCH3_ASIZE_COUNT: 4009_5310H (LCH3)
- DMA_M2P_LCH4_ASIZE_COUNT: 4009_5410H (LCH4)
- DMA_M2P_LCH5_ASIZE_COUNT: 4009_5510H (LCH5)
- DMA_M2P_LCH9_ASIZE_COUNT: 4009_5910H (LCH9)
- DMA_M2P_LCH10_ASIZE_COUNT: 4009_5A10H (LCH10)
- DMA_M2P_LCH12_ASIZE_COUNT: 4009_5C10H (LCH12)
- DMA_M2P_LCH13_ASIZE_COUNT: 4009_5D10H (LCH13)
- DMA_M2P_LCH14_ASIZE_COUNT: 4009_5E10H (LCH14)

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved		M2P_LCHx_ASIZE_COUNT					

Name	R/W	Bit	After Reset	Function
Reserved	–	31:6	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCHx_ASIZE_COUNT	R/W	5:0	0	When written: Specifies the number of blocks to be transferred in a loop during repeat transfer on the source side. 000000: 1 block 000001: 2 blocks 000010: 3 blocks 000011: 4 blocks 000100: 5 blocks 000101: 6 blocks 000110: 7 blocks 000111: 8 blocks 001000: 9 blocks : 111111: 64 blocks When read: Indicates the number of remaining transfer blocks on the source side. The value written to this register is set when DMA is started, and the value is decremented each time block transfer ends.

(6) M2P LCHx destination address register

These registers (DMA_M2P_LCHx_BADD) specify the transfer destination start addresses in byte units.

If the 8-bit width is selected as the transfer bit width using the mode register, the address can be set in byte units.

Likewise, if the 16-bit width is selected, the address can be set in halfwords and if 32-bit width is selected it can be set in words.

- DMA_M2P_LCH0_BADD: 4009_5020H (LCH0)
- DMA_M2P_LCH1_BADD: 4009_5120H (LCH1)
- DMA_M2P_LCH2_BADD: 4009_5220H (LCH2)
- DMA_M2P_LCH3_BADD: 4009_5320H (LCH3)
- DMA_M2P_LCH4_BADD: 4009_5420H (LCH4)
- DMA_M2P_LCH5_BADD: 4009_5520H (LCH5)
- DMA_M2P_LCH9_BADD: 4009_5920H (LCH9)
- DMA_M2P_LCH10_BADD: 4009_5A20H (LCH10)
- DMA_M2P_LCH12_BADD: 4009_5C20H (LCH12)
- DMA_M2P_LCH13_BADD: 4009_5D20H (LCH13)
- DMA_M2P_LCH14_BADD: 4009_5E20H (LCH14)

31	30	29	28	27	26	25	24
M2P_LCHx_BADD							
23	22	21	20	19	18	17	16
M2P_LCHx_BADD							
15	14	13	12	11	10	9	8
M2P_LCHx_BADD							
7	6	5	4	3	2	1	0
M2P_LCHx_BADD							

Name	R/W	Bit	After Reset	Function
M2P_LCHx_BADD	R/W	31:0	0	Specifies the M2P LCHx destination address (start address).

(7) M2P LCHx length registers

These registers (DMA_M2P_LCHx_LENG) specify the total amount of transfer data, in byte units. Up to 16,777,215 bytes can be specified.

If repeat mode is specified in the relevant mode register, infinite-length transfer is specified by setting the corresponding length register to 0.

Caution Do not set these registers to 0 if the repeat mode is not specified. Specifying an offset for infinite-length transfer is prohibited.

- DMA_M2P_LCH0_LENG: 4009_5040H (LCH0)
- DMA_M2P_LCH1_LENG: 4009_5140H (LCH1)
- DMA_M2P_LCH2_LENG: 4009_5240H (LCH2)
- DMA_M2P_LCH3_LENG: 4009_5340H (LCH3)
- DMA_M2P_LCH4_LENG: 4009_5440H (LCH4)
- DMA_M2P_LCH5_LENG: 4009_5540H (LCH5)
- DMA_M2P_LCH9_LENG: 4009_5940H (LCH9)
- DMA_M2P_LCH10_LENG: 4009_5A40H (LCH10)
- DMA_M2P_LCH12_LENG: 4009_5C40H (LCH12)
- DMA_M2P_LCH13_LENG: 4009_5D40H (LCH13)
- DMA_M2P_LCH14_LENG: 4009_5E40H (LCH14)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
M2P_LCHx_LENG							
15	14	13	12	11	10	9	8
M2P_LCHx_LENG							
7	6	5	4	3	2	1	0
M2P_LCHx_LENG							

Name	R/W	Bit	After Reset	Function
Reserved	–	31:24	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCHx_LENG	R/W	23:0	0	Specifies the total amount of data transferred via M2P LCHx, in byte units. 00000000_00000000_00000000: Infinite-length transfer 00000000_00000000_00000001: 1 byte 00000000_00000000_00000010: 2 bytes 00000000_00000000_00000011: 3 bytes 00000000_00000000_00000100: 4 bytes : 11111111_11111111_11111111: 16,777,215 bytes

(8) M2P LCHx read length count registers

These registers (DMA_M2P_LCHx_LENG_RCOUNT) store the total amount of transfer data on the source side. The total transfer length is decremented from the length specified by the corresponding length register to indicate the remaining transfer amount.

- DMA_M2P_LCH0_LENG_RCOUNT: 4009_5044H (LCH0)
- DMA_M2P_LCH1_LENG_RCOUNT: 4009_5144H (LCH1)
- DMA_M2P_LCH2_LENG_RCOUNT: 4009_5244H (LCH2)
- DMA_M2P_LCH3_LENG_RCOUNT: 4009_5344H (LCH3)
- DMA_M2P_LCH4_LENG_RCOUNT: 4009_5444H (LCH4)
- DMA_M2P_LCH5_LENG_RCOUNT: 4009_5544H (LCH5)
- DMA_M2P_LCH9_LENG_RCOUNT: 4009_5944H (LCH9)
- DMA_M2P_LCH10_LENG_RCOUNT: 4009_5A44H (LCH10)
- DMA_M2P_LCH12_LENG_RCOUNT: 4009_5C44H (LCH12)
- DMA_M2P_LCH13_LENG_RCOUNT: 4009_5D44H (LCH13)
- DMA_M2P_LCH14_LENG_RCOUNT: 4009_5E44H (LCH14)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
M2P_LCHx_LENG_RCOUNT							
15	14	13	12	11	10	9	8
M2P_LCHx_LENG_RCOUNT							
7	6	5	4	3	2	1	0
M2P_LCHx_LENG_RCOUNT							

Name	R/W	Bit	After Reset	Function
Reserved	–	31:24	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCHx_LENG_RCOUNT	R	23:0	0	Specifies the total amount of data transferred via M2P LCHx, in byte units. 00000000_00000000_00000000: 0 bytes 00000000_00000000_00000001: 1 byte 00000000_00000000_00000010: 2 bytes 00000000_00000000_00000011: 3 bytes 00000000_00000000_00000100: 4 bytes : 11111111_11111111_11111111: 16,777,215 bytes

(9) M2P LCHx write length count registers

These registers (DMA_M2P_LCHx_LENG_WCOUNT) store the total amount of transfer data on the destination side. The total transfer length is decremented from the length specified by the corresponding length register to indicate the remaining transfer amount.

- DMA_M2P_LCH0_LENG_WCOUNT: 4009_5048H (LCH0)
- DMA_M2P_LCH1_LENG_WCOUNT: 4009_5148H (LCH1)
- DMA_M2P_LCH2_LENG_WCOUNT: 4009_5248H (LCH2)
- DMA_M2P_LCH3_LENG_WCOUNT: 4009_5348H (LCH3)
- DMA_M2P_LCH4_LENG_WCOUNT: 4009_5448H (LCH4)
- DMA_M2P_LCH5_LENG_WCOUNT: 4009_5548H (LCH5)
- DMA_M2P_LCH9_LENG_WCOUNT: 4009_5948H (LCH9)
- DMA_M2P_LCH10_LENG_WCOUNT: 4009_5A48H (LCH10)
- DMA_M2P_LCH12_LENG_WCOUNT: 4009_5C48H (LCH12)
- DMA_M2P_LCH13_LENG_WCOUNT: 4009_5D48H (LCH13)
- DMA_M2P_LCH14_LENG_WCOUNT: 4009_5E48H (LCH14)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
M2P_LCHx_LENG_WCOUNT							
15	14	13	12	11	10	9	8
M2P_LCHx_LENG_WCOUNT							
7	6	5	4	3	2	1	0
M2P_LCHx_LENG_WCOUNT							

Name	R/W	Bit	After Reset	Function
Reserved	–	31:24	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCHx_LENG_WCOUNT	R	23:0	0	Specifies the total amount of data transferred via M2P LCHx, in byte units. 00000000_00000000_00000000: 0 bytes 00000000_00000000_00000001: 1 byte 00000000_00000000_00000010: 2 bytes 00000000_00000000_00000011: 3 bytes 00000000_00000000_00000100: 4 bytes : 11111111_11111111_11111111: 16,777,215 bytes

(10) M2P LCHx mode registers

These registers (DMA_M2P_LCHx_MODE) specify transfer modes (endian, repeat, bit width, and timer settings).

To perform repeat transfer, the offset must be set to 0 (one-dimensional transfer).

- DMA_M2P_LCH0_MODE: 4009_5050H (LCH0)
- DMA_M2P_LCH1_MODE: 4009_5150H (LCH1)
- DMA_M2P_LCH2_MODE: 4009_5250H (LCH2)
- DMA_M2P_LCH3_MODE: 4009_5350H (LCH3)
- DMA_M2P_LCH4_MODE: 4009_5450H (LCH4)
- DMA_M2P_LCH5_MODE: 4009_5550H (LCH5)
- DMA_M2P_LCH9_MODE: 4009_5950H (LCH9)
- DMA_M2P_LCH10_MODE: 4009_5A50H (LCH10)
- DMA_M2P_LCH12_MODE: 4009_5C50H (LCH12)
- DMA_M2P_LCH13_MODE: 4009_5D50H (LCH13)
- DMA_M2P_LCH14_MODE: 4009_5E50H (LCH14)

The timer count setting (M2P_LCHx_MODE_TIME) is only valid for LCH0, LCH1, and LCH2. For other channels, so the bits assigned to the timeout interrupt are not available for other channels (i.e., they are reserved).

31 30	29 28	27 26	25 24
M2P_LCHx_MODE_ ENDI_W_HH	M2P_LCHx_MODE_ ENDI_W_HL	M2P_LCHx_MODE_ ENDI_W_LH	M2P_LCHx_MODE_ ENDI_W_LL
23 22	**21 20**	**19 18**	**17 16**
M2P_LCHx_MODE_ ENDI_R_HH	M2P_LCHx_MODE_ ENDI_R_HL	M2P_LCHx_MODE_ ENDI_R_LH	M2P_LCHx_MODE_ ENDI_R_LL
15 14	**13 12**	**11 10**	**9 8**
Reserved			
7 6	**5 4**	**3 2**	**1 0**
Reserved	M2P_LCHx_ MODE_BIT	Reserved	M2P_LCHx_ MODE_TIME	Reserved	M2P_LCHx_ AMODE_ REPEAT

Name	R/W	Bit	After Reset	Function
M2P_LCHx_MODE_ENDI_W_HH	R/W	31:30	E4H	Specifies the byte lane for writing data to the transfer destination. 00: Byte 0 01: Byte 1 10: Byte 2 11: Byte 3
M2P_LCHx_MODE_ENDI_W_HL	R/W	29:28		
M2P_LCHx_MODE_ENDI_W_LH	R/W	27:26		
M2P_LCHx_MODE_ENDI_W_LL	R/W	25:24		
M2P_LCHx_MODE_ENDI_R_HH	R/W	23:22	E4H	Specifies the byte lane for reading transfer data from the source side. 00: Byte 0 01: Byte 1 10: Byte 2 11: Byte 3
M2P_LCHx_MODE_ENDI_R_HL	R/W	21:20		
M2P_LCHx_MODE_ENDI_R_LH	R/W	19:18		
M2P_LCHx_MODE_ENDI_R_LL	R/W	17:16		
Reserved	R	15:6	0	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCHx_MODE_BIT	R/W	5:4	0	Specifies the transfer bit width. 00: 32 bits, 01: 16 bits, 10: 8 bits, 11: Setting prohibited
Reserved	R	3	0	Reserved. When this bit is read, 0 is returned.
M2P_LCHx_MODE_TIME	R/W	2	0	Specifies whether the timer count is used. 0: Does not use the timer, 1: Uses the timer (UART0 to UART2 only).
Reserved	R	1	0	Reserved. When this bit is read, 0 is returned.
M2P_LCHx_AMODE_REPEAT	R/W	0	0	Specifies the transfer source to repeat mode. 0: Does not specify repeat mode, 1: Specifies repeat mode.

Caution When restarting a logical channel that has timed out, M2P_LCHx_MODE_TIME needs to be set to "1," then "0," and then "1" again in order to preset the timer. Be sure to insert two or more DMA_TCLK clock cycles between setting "0" (low level) and setting "1" again.
Be sure to supply a timer clock (DMA_TCLK) when using a timer function; otherwise, DMA clock control may malfunction.

(11) M2P LCHx timer registers

These registers (DMA_M2P_LCHx_TIME) specify the time allowed to elapse until the DMA transfer is forced to end. If no DMA request has been issued for a specific period, DMA transfer is forced to end if the time specified in this register expires. Up to 24 bits can be set.

This function is valid only for memory-to-UART channels (LCH0, LCH1, and LCH2).

- DMA_M2P_LCH0_TIME: 4009_5054H (LCH0)
- DMA_M2P_LCH1_TIME: 4009_5154H (LCH1)
- DMA_M2P_LCH2_TIME: 4009_5254H (LCH2)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
M2P_LCHx_TIME							
15	14	13	12	11	10	9	8
M2P_LCHx_TIME							
7	6	5	4	3	2	1	0
M2P_LCHx_TIME							

Name	R/W	Bit	After Reset	Function
Reserved	–	31:24	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCHx_TIME	R/W	23:0	0	Specifies the time allowed to elapse before M2P LCHx operation times out.

Caution Be sure to supply a timer clock (DMA_TCLK) when using a timer function; otherwise, DMA clock control may malfunction.

(12) M2P LCHx timer count registers

These registers (DMA_M2P_LCHx_TIME_COUNT) count down the time until DMA transfer is forced to end. The time is counted down in units of the DMA_TCLK clock output from the ASMU. When the count reaches 0, DMA transfer times out and is forced to end.

This function is valid only for memory-to-UART channels (LCH0, LCH1, and LCH2).

- DMA_M2P_LCH0_TIME_COUNT: 4009_5058H (LCH0)
- DMA_M2P_LCH1_TIME_COUNT: 4009_5158H (LCH1)
- DMA_M2P_LCH2_TIME_COUNT: 4009_5258H (LCH2)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
M2P_LCHx_TIME_COUNT							
15	14	13	12	11	10	9	8
M2P_LCHx_TIME_COUNT							
7	6	5	4	3	2	1	0
M2P_LCHx_TIME_COUNT							

Name	R/W	Bit	After Reset	Function
Reserved	–	31:24	–	Reserved. When these bits are read, 0 is returned for each bit.
M2P_LCHx_TIME_COUNT	R	23:0	0	Stores the time allowed to elapse before M2P LCHx operation times out. DMA_TCLK is used for timer counting.

2.3.7 P2M DMA control/status registers

(1) P2M DMA start control register

This register (DMA_P2M_CONT: 4009_6000H) controls whether to start DMA transfer on a per-logical channel basis.

If this register is set up while the P2M_LCHx_RESERVE bit of the P2M DMA start control status register is set to 0, the subsequent transfer starts immediately after the current transfer ends (simple reservation). A transfer parameter for the subsequent transfer must be set before using simple reservation. For details, see **3.4.3 Continuous transfer**.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved	P2M_LCH14_CONT	P2M_LCH13_CONT	P2M_LCH12_CONT	Reserved	P2M_LCH10_CONT	P2M_LCH9_CONT	Reserved

7	6	5	4	3	2	1	0
Reserved		P2M_LCH5_CONT	P2M_LCH4_CONT	P2M_LCH3_CONT	P2M_LCH2_CONT	P2M_LCH1_CONT	P2M_LCH0_CONT

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31:15	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH14_CONT	W	14	0	Controls whether to start DMA transfer on P2M LCH14. (1: Starts DMA transfer.)
P2M_LCH13_CONT	W	13	0	Controls whether to start DMA transfer on P2M LCH13. (1: Starts DMA transfer.)
P2M_LCH12_CONT	W	12	0	Controls whether to start DMA transfer on P2M LCH12. (1: Starts DMA transfer.)
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
P2M_LCH10_CONT	W	10	0	Controls whether to start DMA transfer on P2M LCH10. (1: Starts DMA transfer.)
P2M_LCH9_CONT	W	9	0	Controls whether to start DMA transfer on P2M LCH9. (1: Starts DMA transfer.)
Reserved	R	8:6	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH5_CONT	W	5	0	Controls whether to start DMA transfer on P2M LCH5. (1: Starts DMA transfer.)
P2M_LCH4_CONT	W	4	0	Controls whether to start DMA transfer on P2M LCH4. (1: Starts DMA transfer.)

(2/2)

Name	R/W	Bit	After Reset	Function
P2M_LCH3_CONT	W	3	0	Controls whether to start DMA transfer on P2M LCH3. (1: Starts DMA transfer.)
P2M_LCH2_CONT	W	2	0	Controls whether to start DMA transfer on P2M LCH2. (1: Starts DMA transfer.)
P2M_LCH1_CONT	W	1	0	Controls whether to start DMA transfer on P2M LCH1. (1: Starts DMA transfer.)
P2M_LCH0_CONT	W	0	0	Controls whether to start DMA transfer on P2M LCH0. (1: Starts DMA transfer.)

(2) P2M DMA control status register

This register (DMA_P2M_CONTSTATUS: 4009_6004H) indicates the status of the DMA controller.

The DMA start reservation status register indicates whether DMA transfer has been reserved. If a bit is set to 1, the corresponding LCH has already been reserved for the next transfer, so another reservation cannot be made.

31	30	29	28	27	26	25	24
Reserved	P2M_LCH14_RESERVE	P2M_LCH13_RESERVE	P2M_LCH12_RESERVE	Reserved	P2M_LCH10_RESERVE	P2M_LCH9_RESERVE	Reserved
23	22	21	20	19	18	17	16
Reserved		P2M_LCH5_RESERVE	P2M_LCH4_RESERVE	P2M_LCH3_RESERVE	P2M_LCH2_RSERVE	P2M_LCH1_RSERVE	P2M_LCH0_RSERVE
15	14	13	12	11	10	9	8
Reserved	P2M_LCH14_CONTSTATUS	P2M_LCH13_CONTSTATUS	P2M_LCH12_CONTSTATUS	Reserved	P2M_LCH10_CONTSTATUS	P2M_LCH9_CONTSTATUS	Reserved
7	6	5	4	3	2	1	0
Reserved		P2M_LCH5_CONTSTATUS	P2M_LCH4_CONTSTATUS	P2M_LCH3_CONTSTATUS	P2M_LCH2_CONTSTATUS	P2M_LCH1_CONTSTATUS	P2M_LCH0_CONTSTATUS

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31	–	Reserved. When this bit is read, 0 is returned.
P2M_LCH14_RESERVE	R	30	0	Indicates the status of DMA transfer reservation on P2M LCH14. 0: Not reserved, 1: Reserved
P2M_LCH13_RESERVE	R	29	0	Indicates the status of DMA transfer reservation on P2M LCH13. 0: Not reserved, 1: Reserved
P2M_LCH12_RESERVE	R	28	0	Indicates the status of DMA transfer reservation on P2M LCH12. 0: Not reserved, 1: Reserved
Reserved	R	27	–	Reserved. When this bit is read, 0 is returned.
P2M_LCH10_RESERVE	R	26	0	Indicates the status of DMA transfer reservation on P2M LCH10. 0: Not reserved, 1: Reserved
P2M_LCH9_RESERVE	R	25	0	Indicates the status of DMA transfer reservation on P2M LCH9. 0: Not reserved, 1: Reserved
Reserved	R	24:22	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH5_RESERVE	R	21	0	Indicates the status of DMA transfer reservation on P2M LCH5. 0: Not reserved, 1: Reserved
P2M_LCH4_RESERVE	R	20	0	Indicates the status of DMA transfer reservation on P2M LCH4. 0: Not reserved, 1: Reserved
P2M_LCH3_RESERVE	R	19	0	Indicates the status of DMA transfer reservation on P2M LCH3. 0: Not reserved, 1: Reserved
P2M_LCH2_RESERVE	R	18	0	Indicates the status of DMA transfer reservation on P2M LCH2. 0: Not reserved, 1: Reserved
P2M_LCH1_RESERVE	R	17	0	Indicates the status of DMA transfer reservation on P2M LCH1. 0: Not reserved, 1: Reserved

(2/2)

Name	R/W	Bit	After Reset	Function
P2M_LCH0_RESERVE	R	16	0	Indicates the status of DMA transfer reservation on P2M LCH0. 0: Not reserved, 1: Reserved
Reserved	R	15	–	Reserved. When this bit is read, 0 is returned.
P2M_LCH14_CONTSTATUS	R	14	0	Indicates the status of DMA transfer on P2M LCH14. 0: DMA is inactive, 1: DMA is active
P2M_LCH13_CONTSTATUS	R	13	0	Indicates the status of DMA transfer on P2M LCH13. 0: DMA is inactive, 1: DMA is active
P2M_LCH12_CONTSTATUS	R	12	0	Indicates the status of DMA transfer on P2M LCH12. 0: DMA is inactive, 1: DMA is active
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
P2M_LCH10_CONTSTATUS	R	10	0	Indicates the status of DMA transfer on P2M LCH10. 0: DMA is inactive, 1: DMA is active
P2M_LCH9_CONTSTATUS	R	9	0	Indicates the status of DMA transfer on P2M LCH9. 0: DMA is inactive, 1: DMA is active
Reserved	R	8:6	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH5_CONTSTATUS	R	5	0	Indicates the status of DMA transfer on P2M LCH5. 0: DMA is inactive, 1: DMA is active
P2M_LCH4_CONTSTATUS	R	4	0	Indicates the status of DMA transfer on P2M LCH4. 0: DMA is inactive, 1: DMA is active
P2M_LCH3_CONTSTATUS	R	3	0	Indicates the status of DMA transfer on P2M LCH3. 0: DMA is inactive, 1: DMA is active
P2M_LCH2_CONTSTATUS	R	2	0	Indicates the status of DMA transfer on P2M LCH2. 0: DMA is inactive, 1: DMA is active
P2M_LCH1_CONTSTATUS	R	1	0	Indicates the status of DMA transfer on P2M LCH1. 0: DMA is inactive, 1: DMA is active
P2M_LCH0_CONTSTATUS	R	0	0	Indicates the status of DMA transfer on P2M LCH0. 0: DMA is inactive, 1: DMA is active

(3) P2M DMA end control register

This register (DMA_P2M_END: 4009_6008H) controls whether to force DMA transfer to end.

If DMA transfer is forcibly terminated, a reservation for the next transfer becomes invalid. If this register is set up, forced termination takes effect when the current AHB transaction is completed. Therefore, DMA transfer cannot be restarted until the AHB transaction ends. Once DMA starts, at least one DMA write transfer transaction must be performed before executing forced termination; otherwise, parameters are not updated in the internal circuits and thus DMA transfer is not executed correctly. In addition, before terminating the P2M channel forcibly, DMA requests from peripherals must be stopped first and data of the relevant LCH stored in the FIFO in the DMA controller must be read out.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved	P2M_LCH14_END	P2M_LCH13_END	P2M_LCH12_END	Reserved	P2M_LCH10_END	P2M_LCH9_END	Reserved
7	6	5	4	3	2	1	0
Reserved		P2M_LCH5_END	P2M_LCH4_END	P2M_LCH3_END	P2M_LCH2_END	P2M_LCH1_END	P2M_LCH0_END

Name	R/W	Bit	After Reset	Function
Reserved	R	31:15	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH14_END	W	14	0	Specifies whether to force DMA transfer on P2M LCH14 to end.
P2M_LCH13_END	W	13	0	Specifies whether to force DMA transfer on P2M LCH13 to end.
P2M_LCH12_END	W	12	0	Specifies whether to force DMA transfer on P2M LCH12 to end.
Reserved	R	11	–	Reserved. When this bit is read, 0 is returned.
P2M_LCH10_END	W	10	0	Specifies whether to force DMA transfer on P2M LCH10 to end.
P2M_LCH9_END	W	9	0	Specifies whether to force DMA transfer on P2M LCH9 to end.
Reserved	R	8:6	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH5_END	W	5	0	Specifies whether to force DMA transfer on P2M LCH5 to end.
P2M_LCH4_END	W	4	0	Specifies whether to force DMA transfer on P2M LCH4 to end.
P2M_LCH3_END	W	3	0	Specifies whether to force DMA transfer on P2M LCH3 to end.
P2M_LCH2_END	W	2	0	Specifies whether to force DMA transfer on P2M LCH2 to end.
P2M_LCH1_END	W	1	0	Specifies whether to force DMA transfer on P2M LCH1 to end.
P2M_LCH0_END	W	0	0	Specifies whether to force DMA transfer on P2M LCH0 to end.

Remark 0: Retains the current status, 1: Forces DMA transfer to end

2.3.8 P2M interrupt parameter setting registers

These registers set the parameters for four types of interrupts - length transfer end, block transfer end, error end, and timeout.

(1) P2M interrupt status registers

These registers (DMA_P2M_*XXX*_LCHx_INT_CONT) indicate the interrupt source statuses.
Separate source registers are provided for the AHB write side (*_W_*) and the AHB read side (*_R_*).

Remark The ACPU and ADSP each have their dedicated registers, and the P2M_LCHx_INT_SEL register is used to select which processor to use.

- DMA_P2M_PE0_LCH0LCH3_INT_CONT: 4009_6100H (ACPU, LCH0 to LCH3)
- DMA_P2M_DSP_LCH0LCH3_INT_CONT: 4009_6400H (ADSP, LCH0 to LCH3)
- DMA_P2M_PE0_LCH4LCH5_INT_CONT: 4009_6120H (ACPU, LCH4 to LCH5)
- DMA_P2M_DSP_LCH4LCH5_INT_CONT: 4009_6420H (ADSP, LCH4 to LCH5)
- DMA_P2M_PE0_LCH9LCH10_INT_CONT: 4009_6140H (ACPU, LCH9 to LCH10)
- DMA_P2M_DSP_LCH9LCH10_INT_CONT: 4009_6440H (ADSP, LCH9 to LCH10)
- DMA_P2M_PE0_LCH12LCH14_INT_CONT: 4009_6160H (ACPU, LCH12 to LCH14)
- DMA_P2M_DSP_LCH12LCH14_INT_CONT: 4009_6460H (ADSP, LCH12 to LCH14)

The bit assignment for LCH0 to LCH3 is shown below. The other channels have the same structure. However, the timeout interrupt (INT_TIME) occurs only on LCH0 to LCH3 and LCH7, so the bits assigned to the timeout interrupt are not available for other channels (i.e., they are reserved).

31	30	29	28	27	26	25	24
Reserved	P2M_LCH3_INT_ERROR_W_CONT	P2M_LCH3_INT_BLOCK_W_CONT	P2M_LCH3_INT_LENG_W_CONT	P2M_LCH3_INT_TIME_R_CONT	P2M_LCH3_INT_ERROR_R_CONT	Reserved	

23	22	21	20	19	18	17	16
Reserved	P2M_LCH2_INT_ERROR_W_CONT	P2M_LCH2_INT_BLOCK_W_CONT	P2M_LCH2_INT_LENG_W_CONT	P2M_LCH2_INT_TIME_R_CONT	P2M_LCH2_INT_ERROR_R_CONT	Reserved	

15	14	13	12	11	10	9	8
Reserved	P2M_LCH1_INT_ERROR_W_CONT	P2M_LCH1_INT_BLOCK_W_CONT	P2M_LCH1_INT_LENG_W_CONT	P2M_LCH1_INT_TIME_R_CONT	P2M_LCH1_INT_ERROR_R_CONT	Reserved	

7	6	5	4	3	2	1	0
Reserved	P2M_LCH0_INT_ERROR_W_CONT	P2M_LCH0_INT_BLOCK_W_CONT	P2M_LCH0_INT_LENG_W_CONT	P2M_LCH0_INT_TIME_R_CONT	P2M_LCH0_INT_ERROR_R_CONT	Reserved	

Name	R/W	Bit	After Reset	Function
Reserved	–	31	–	Reserved. When this bit is read, 0 is returned.
P2M_LCH3_INT_ ERROR_W_CONT	R	30	0	Indicates the status of the interrupt source generated upon a P2M LCH3 error.
P2M_LCH3_INT_ BLOCK_W_CONT	R	29	0	Indicates the status of the interrupt source generated upon completion of P2M LCH3 block transfer.
P2M_LCH3_INT_ LENG_W_CONT	R	28	0	Indicates the status of the interrupt source generated upon completion of P2M LCH3 length transfer.
P2M_LCH3_INT_ TIME_R_CONT	R	27	0	Indicates the status of the interrupt source generated upon P2M LCH3 timeout.
P2M_LCH3_INT_ ERROR_R_CONT	R	26	0	Indicates the status of the interrupt source generated upon a P2M LCH3 error.
Reserved	–	25:23	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH2_INT_ ERROR_W_CONT	R	22	0	Indicates the status of the interrupt source generated upon a P2M LCH2 error.
P2M_LCH2_INT_ BLOCK_W_CONT	R	21	0	Indicates the status of the interrupt source generated upon completion of P2M LCH2 block transfer.
P2M_LCH2_INT_ LENG_W_CONT	R	20	0	Indicates the status of the interrupt source generated upon completion of P2M LCH2 length transfer.
P2M_LCH2_INT_ TIME_R_CONT	R	19	0	Indicates the status of the interrupt source generated upon P2M LCH2 timeout.
P2M_LCH2_INT_ ERROR_R_CONT	R	18	0	Indicates the status of the interrupt source generated upon a P2M LCH2 error.
Reserved	–	17:15	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH1_INT_ ERROR_W_CONT	R	14	0	Indicates the status of the interrupt source generated upon a P2M LCH1 error.
P2M_LCH1_INT_ BLOCK_E_CONT	R	13	0	Indicates the status of the interrupt source generated upon completion of P2M LCH1 block transfer.
P2M_LCH1_INT_ LENG_W_CONT	R	12	–	Indicates the status of the interrupt source generated upon completion of P2M LCH1 length transfer.
P2M_LCH1_INT_ TIME_R_CONT	R	11	0	Indicates the status of the interrupt source generated upon P2M LCH1 timeout.
P2M_LCH1_INT_ ERROR_R_CONT	R	10	0	Indicates the status of the interrupt source generated upon a P2M LCH1 error.
Reserved	–	9:7		Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH0_INT_ ERROR_W_CONT	R	6	0	Indicates the status of the interrupt source generated upon a P2M LCH0 error.
P2M_LCH0_INT_ BLOCK_W_CONT	R	5	0	Indicates the status of the interrupt source generated upon completion of P2M LCH0 block transfer.
P2M_LCH0_INT_ LENG_W_CONT	R	4	0	Indicates the status of the interrupt source generated upon completion of P2M LCH0 length transfer.
P2M_LCH0_INT_ TIME_R_CONT	R	3	0	Indicates the status of the interrupt source generated upon P2M LCH0 timeout.
P2M_LCH0_INT_ ERROR_R_CONT	R	2	0	Indicates the status of the interrupt source generated upon a P2M LCH0 error.
Reserved	–	1:0	–	Reserved. When these bits are read, 0 is returned for each bit.

Remark 0: No interrupt source (default), 1: Interrupt source occurred

(2) P2M interrupt raw status registers

These registers (DMA_P2M_*XXX*_LCHx_INT_RAW) can be used to read the status of the interrupt sources regardless of the settings of the interrupt enable set register and the interrupt enable clear register. Separate source registers are provided for the AHB write side (*_W_*) and the AHB read side (*_R_*).

Remark The ACPU and ADSP each have their dedicated registers, and the P2M_LCHx_INT_SEL register is used to select which processor to use.

- DMA_P2M_PE0_LCH0LCH3_INT_RAW: 4009_6104H (ACPU, LCH0 to LCH3)
- DMA_P2M_DSP_LCH0LCH3_INT_RAW: 4009_6404H (ADSP, LCH0 to LCH3)
- DMA_P2M_PE0_LCH4LCH5_INT_RAW: 4009_6124H (ACPU, LCH4 to LCH5)
- DMA_P2M_DSP_LCH4LCH5_INT_RAW: 4009_6424H (ADSP, LCH4 to LCH5)
- DMA_P2M_PE0_LCH9LCH10_INT_RAW: 4009_6144H (ACPU, LCH9 to LCH10)
- DMA_P2M_DSP_LCH9LCH10_INT_RAW: 4009_6444H (ADSP, LCH9 to LCH10)
- DMA_P2M_PE0_LCH12LCH14_INT_RAW: 4009_6164H (ACPU, LCH12 to LCH14)
- DMA_P2M_DSP_LCH12LCH14_INT_RAW: 4009_6464H (ADSP, LCH12 to LCH14)

The bit assignment for LCH0 to LCH3 is shown below. The other channels have the same structure. However, the timeout interrupt (INT_TIME) occurs only on LCH0 to LCH3 and LCH7, so the bits assigned to the timeout interrupt are not available for other channels (i.e., they are reserved).

31	30	29	28	27	26	25	24
Reserved	P2M_LCH3_INT_ERROR_W_RAW	P2M_LCH3_INT_BLOCK_W_RAW	P2M_LCH3_INT_LENG_W_RAW	P2M_LCH3_INT_TIME_R_RAW	P2M_LCH3_INT_ERROR_R_RAW	Reserved	

23	22	21	20	19	18	17	16
Reserved	P2M_LCH2_INT_ERROR_W_RAW	P2M_LCH2_INT_BLOCK_W_RAW	P2M_LCH2_INT_LENG_W_RAW	P2M_LCH2_INT_TIME_R_RAW	P2M_LCH2_INT_ERROR_R_RAW	Reserved	

15	14	13	12	11	10	9	8
Reserved	P2M_LCH1_INT_ERROR_W_RAW	P2M_LCH1_INT_BLOCK_W_RAW	P2M_LCH1_INT_LENG_W_RAW	P2M_LCH1_INT_TIME_R_RAW	P2M_LCH1_INT_ERROR_R_RAW	Reserved	

7	6	5	4	3	2	1	0
Reserved	P2M_LCH0_INT_ERROR_W_RAW	P2M_LCH0_INT_BLOCK_W_RAW	P2M_LCH0_INT_LENG_W_RAW	P2M_LCH0_INT_TIME_R_RAW	P2M_LCH0_INT_ERROR_R_RAW	Reserved	

Name	R/W	Bit	After Reset	Function
Reserved	–	31	–	Reserved. When this bit is read, 0 is returned.
P2M_LCH3_INT_ ERROR_W_RAW	R	30	0	Indicates the status of the interrupt source generated upon a P2M LCH3 error.
P2M_LCH3_INT_ BLOCK_W_RAW	R	29	0	Indicates the status of the interrupt source generated upon completion of P2M LCH3 block transfer.
P2M_LCH3_INT_ LENG_W_RAW	R	28	0	Indicates the status of the interrupt source generated upon completion of P2M LCH3 length transfer.
P2M_LCH3_INT_ TIME_R_RAW	R	27	0	Indicates the status of the interrupt source generated upon P2M LCH3 timeout.
P2M_LCH3_INT_ ERROR_R_RAW	R	26	0	Indicates the status of the interrupt source generated upon a P2M LCH3 error.
Reserved	–	25:23	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH2_INT_ ERROR_W_RAW	R	22	0	Indicates the status of the interrupt source generated upon a P2M LCH2 error.
P2M_LCH2_INT_ BLOCK_W_RAW	R	21	0	Indicates the status of the interrupt source generated upon completion of P2M LCH2 block transfer.
P2M_LCH2_INT_ LENG_W_RAW	R	20	0	Indicates the status of the interrupt source generated upon completion of P2M LCH2 length transfer.
P2M_LCH2_INT_ TIME_R_RAW	R	19	0	Indicates the status of the interrupt source generated upon P2M LCH2 timeout.
P2M_LCH2_INT_ ERROR_R_RAW	R	18	0	Indicates the status of the interrupt source generated upon a P2M LCH2 error.
Reserved	–	17:15	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH1_INT_ ERROR_W_RAW	R	14	0	Indicates the status of the interrupt source generated upon a P2M LCH1 error.
P2M_LCH1_INT_ BLOCK_W_RAW	R	13	0	Indicates the status of the interrupt source generated upon completion of P2M LCH1 block transfer.
P2M_LCH1_INT_ LENG_W_RAW	R	12	0	Indicates the status of the interrupt source generated upon completion of P2M LCH1 length transfer.
P2M_LCH1_INT_ TIME_R_RAW	R	11	0	Indicates the status of the interrupt source generated upon P2M LCH1 timeout.
P2M_LCH1_INT_ ERROR_R_RAW	R	10	0	Indicates the status of the interrupt source generated upon a P2M LCH1 error.
Reserved	–	9:7	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH0_INT_ ERROR_W_RAW	R	6	0	Indicates the status of the interrupt source generated upon a P2M LCH0 error.
P2M_LCH0_INT_ BLOCK_W_RAW	R	5	0	Indicates the status of the interrupt source generated upon completion of P2M LCH0 block transfer.
P2M_LCH0_INT_ LENG_W_RAW	R	4	0	Indicates the status of the interrupt source generated upon completion of P2M LCH0 length transfer.
P2M_LCH0_INT_ TIME_R_RAW	R	3	0	Indicates the status of the interrupt source generated upon P2M LCH0 timeout.
P2M_LCH0_INT_ ERROR_R_RAW	R	2	0	Indicates the status of the interrupt source generated upon a P2M LCH0 error.
Reserved	–	1:0	–	Reserved. When these bits are read, 0 is returned for each bit.

Remark 0: No interrupt source (default), 1: Interrupt source occurred

(3) P2M interrupt enable set registers

These registers (DMA_P2M_*XXX*_LCHx_INT_ENABLE) enable interrupt sources. Only data of bits to which 1 is written is updated.

Masking of interrupt sources corresponding to bits to which 1 is written is cancelled. The interrupt enable status can be checked by reading this register. Writing 0 to this register does not affect the setting.

To mask an interrupt source, set the corresponding bit of the interrupt enable clear register to 1.

Remark The ACPU and ADSP each have their dedicated registers, and the P2M_LCHx_INT_SEL register is used to select which processor to use.

- DMA_P2M_PE0_LCH0LCH3_INT_ENABLE: 4009_6108H (ACPU, LCH0 to LCH3)
- DMA_P2M_DSP_LCH0LCH3_INT_ENABLE: 4009_6408H (ADSP, LCH0 to LCH3)
- DMA_P2M_PE0_LCH4LCH5_INT_ENABLE: 4009_6128H (ACPU, LCH4 to LCH5)
- DMA_P2M_DSP_LCH4LCH5_INT_ENABLE: 4009_6428H (ADSP, LCH4 to LCH5)
- DMA_P2M_PE0_LCH9LCH10_INT_ENABLE: 4009_6148H (ACPU, LCH9 to LCH10)
- DMA_P2M_DSP_LCH9LCH10_INT_ENABLE: 4009_6448H (ADSP, LCH9 to LCH10)
- DMA_P2M_PE0_LCH12LCH14_INT_ENABLE: 4009_6168H (ACPU, LCH12 to LCH14)
- DMA_P2M_DSP_LCH12LCH14_INT_ENABLE: 4009_6468H (ADSP, LCH12 to LCH14)

The bit assignment for LCH0 to LCH3 is shown below. The other channels have the same structure. However, the timeout interrupt (INT_TIME) occurs only on LCH0 to LCH3 and LCH7, so the bits assigned to the timeout interrupt are not available for other channels (i.e., they are reserved).

31	30	29	28	27	26	25	24
Reserved				P2M_LCH3_INT_TIME_ENABLE	P2M_LCH3_INT_ERROR_ENABLE	P2M_LCH3_INT_BLOCK_ENABLE	P2M_LCH3_INT_LENG_ENABLE

23	22	21	20	19	18	17	16
Reserved				P2M_LCH2_INT_TIME_ENABLE	P2M_LCH2_INT_ERROR_ENABLE	P2M_LCH2_INT_BLOCK_ENABLE	P2M_LCH2_INT_LENG_ENABLE

15	14	13	12	11	10	9	8
Reserved				P2M_LCH1_INT_TIME_ENABLE	P2M_CH1_INT_ERROR_ENABLE	P2M_CH1_INT_BLOCK_ENABLE	P2M_CH1_INT_LENG_ENABLE

7	6	5	4	3	2	1	0
Reserved				P2M_LCH0_INT_TIME_ENABLE	P2M_LCH0_INT_ERROR_ENABLE	P2M_LCH0_INT_BLOCK_ENABLE	P2M_LCH0_INT_LENG_ENABLE

Name	R/W	Bit	After Reset	Function
Reserved	–	31:28	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH3_INT_TIME_ENABLE	R/W	27	0	Enables the P2M LCH3 timeout interrupt source.
P2M_LCH3_INT_ERROR_ENABLE	R/W	26	0	Enables the P2M LCH3 error interrupt source.
P2M_LCH3_INT_BLOCK_ENABLE	R/W	25	0	Enables the P2M LCH3 block interrupt source.
P2M_LCH3_INT_LENG_ENABLE	R/W	24	0	Enables the P2M LCH3 length interrupt source.
Reserved	–	23:20	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH2_INT_TIME_ENABLE	R/W	19	0	Enables the P2M LCH2 timeout interrupt source.
P2M_LCH2_INT_ERROR_ENABLE	R/W	18	0	Enables the P2M LCH2 error interrupt source.
P2M_LCH2_INT_BLOCK_ENABLE	R/W	17	0	Enables the P2M LCH2 block interrupt source.
P2M_LCH2_INT_LENG_ENABLE	R/W	16	0	Enables the P2M LCH2 length interrupt source.
Reserved	–	15:12	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH1_INT_TIME_ENABLE	R/W	11	0	Enables the P2M LCH1 timeout interrupt source.
P2M_LCH1_INT_ERROR_ENABLE	R/W	10	0	Enables the P2M LCH1 error interrupt source.
P2M_LCH1_INT_BLOCK_ENABLE	R/W	9	0	Enables the P2M LCH1 block interrupt source.
P2M_LCH1_INT_LENG_ENABLE	R/W	8	0	Enables the P2M LCH1 length interrupt source.
Reserved	–	7:4	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH0_INT_TIME_ENABLE	R/W	3	0	Enables the P2M LCH0 timeout interrupt source.
P2M_LCH0_INT_ERROR_ENABLE	R/W	2	0	Enables the P2M LCH0 error interrupt source.
P2M_LCH0_INT_BLOCK_ENABLE	R/W	1	0	Enables the P2M LCH0 block interrupt source.
P2M_LCH0_INT_LENG_ENABLE	R/W	0	0	Enables the P2M LCH0 length interrupt source.

Remark 0: Disables the interrupt source (default), 1: Enables the interrupt source

(4) P2M interrupt enable clear registers

These registers (DMA_P2M_*XXX*_LCHx_INT_ENABLE_CL) mask interrupt sources.

If a bit of these registers is set to 1, the corresponding interrupt source is disabled. The bits to which 0 is written retain the current settings.

If interrupt sources are disabled in these registers, the corresponding bits in the ARM interrupt enable set register is set to 0 (masks the interrupt sources).

Remark The ACPU and ADSP each have their dedicated registers, and the P2M_LCHx_INT_SEL register is used to select which processor to use.

- DMA_P2M_PE0_LCH0LCH3_INT_ENABLE_CL: 4009_610CH (ACPU, LCH0 to LCH3)
- DMA_P2M_DSP_LCH0LCH3_INT_ENABLE_CL: 4009_640CH (ADSP, LCH0 to LCH3)
- DMA_P2M_PE0_LCH4LCH5_INT_ENABLE_CL: 4009_612CH (ACPU, LCH4 to LCH5)
- DMA_P2M_DSP_LCH4LCH5_INT_ENABLE_CL: 4009_642CH (ADSP, LCH4 to LCH5)
- DMA_P2M_PE0_LCH9LCH10_INT_ENABLE_CL: 4009_614CH (ACPU, LCH9 to LCH10)
- DMA_P2M_DSP_LCH9LCH10_INT_ENABLE_CL: 4009_644CH (ADSP, LCH9 to LCH10)
- DMA_P2M_PE0_LCH12LCH14_INT_ENABLE_CL: 4009_616CH (ACPU, LCH12 to LCH14)
- DMA_P2M_DSP_LCH12LCH14_INT_ENABLE_CL: 4009_646CH (ADSP, LCH12 to LCH14)

The bit assignment for LCH0 to LCH3 is shown below. The other channels have the same structure. However, the timeout interrupt (INT_TIME) occurs only on LCH0 to LCH3 and LCH7, so the bits assigned to the timeout interrupt are not available for other channels (i.e., they are reserved).

31	30	29	28	27	26	25	24
Reserved				P2M_LCH3_INT_TIME_ENABLE_CL	P2M_LCH3_INT_ERROR_ENABLE_CL	P2M_LCH3_INT_BLOCK_ENABLE_CL	P2M_LCH3_INT_LENG_ENABLE_CL

23	22	21	20	19	18	17	16
Reserved				P2M_LCH2_INT_TIME_ENABLE_CL	P2M_LCH2_INT_ERROR_ENABLE_CL	P2M_LCH2_INT_BLOCK_ENABLE_CL	P2M_LCH2_INT_LENG_ENABLE_CL

15	14	13	12	11	10	9	8
Reserved				P2M_LCH1_INT_TIME_ENABLE_CL	P2M_LCH1_INT_ERROR_ENABLE_CL	P2M_LCH1_INT_BLOCK_ENABLE_CL	P2M_LCH1_INT_LENG_ENABLE_CL

7	6	5	4	3	2	1	0
Reserved				P2M_LCH0_INT_TIME_ENABLE_CL	P2M_LCH0_INT_ERROR_ENABLE_CL	P2M_LCH0_INT_BLOCK_ENABLE_CL	P2M_LCH0_INT_LENG_ENABLE_CL

Name	R/W	Bit	After Reset	Function
Reserved	–	31:28	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH3_INT_TIME_ENABLE_CL	W	27	0	Disables the P2M LCH3 timeout interrupt source.
P2M_LCH3_INT_ERROR_ENABLE_CL	W	26	0	Disables the P2M LCH3 error interrupt source.
P2M_LCH3_INT_BLOCK_ENABLE_CL	W	25	0	Disables the P2M LCH3 block interrupt source.
P2M_LCH3_INT_LENG_ENABLE_CL	W	24	0	Disables the P2M LCH3 length interrupt source.
Reserved	–	23:20	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH2_INT_TIME_ENABLE_CL	W	19	0	Disables the P2M LCH2 timeout interrupt source.
P2M_LCH2_INT_ERROR_ENABLE_CL	W	18	0	Disables the P2M LCH2 error interrupt source.
P2M_LCH2_INT_BLOCK_ENABLE_CL	W	17	0	Disables the P2M LCH2 block interrupt source.
P2M_LCH2_INT_LENG_ENABLE_CL	W	16	0	Disables the P2M LCH2 length interrupt source.
Reserved	–	15:12	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH1_INT_TIME_ENABLE_CL	W	11	0	Disables the P2M LCH1 timeout interrupt source.
P2M_LCH1_INT_ERROR_ENABLE_CL	W	10	0	Disables the P2M LCH1 error interrupt source.
P2M_LCH1_INT_BLOCK_ENABLE_CL	W	9	0	Disables the P2M LCH1 block interrupt source.
P2M_LCH1_INT_LENG_ENABLE_CL	W	8	0	Disables the P2M LCH1 length interrupt source.
Reserved	–	7:4	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH0_INT_TIME_ENABLE_CL	W	3	0	Disables the P2M LCH0 timeout interrupt source.
P2M_LCH0_INT_ERROR_ENABLE_CL	W	2	0	Disables the P2M LCH0 error interrupt source.
P2M_LCH0_INT_BLOCK_ENABLE_CL	W	1	0	Disables the P2M LCH0 block interrupt source.
P2M_LCH0_INT_LENG_ENABLE_CL	W	0	0	Disables the P2M LCH0 length interrupt source.

Remark 0: Disables the interrupt source (default), 1: Enables the interrupt source

(5) P2M interrupt source clear registers

These registers (DMA_P2M_*XXX*_LCHx_INT_REQ_CL) request clearing of interrupt sources. Only data of bits to which 1 is written is updated.

Separate source registers are provided for the AHB write side (*_W_*) and the AHB read side (*_R_*).

Remark The ACPU and ADSP each have their dedicated registers, and the P2M_LCHx_INT_SEL register is used to select which processor to use.

- DMA_P2M_PE0_LCH0LCH3_INT_REQ_CL: 4009_6110H (ACPU, LCH0 to LCH3)
- DMA_P2M_DSP_LCH0LCH3_INT_REQ_CL: 4009_6410H (ADSP, LCH0 to LCH3)
- DMA_P2M_PE0_LCH4LCH5_INT_REQ_CL: 4009_6130H (ACPU, LCH4 to LCH5)
- DMA_P2M_DSP_LCH4LCH5_INT_REQ_CL: 4009_6430H (ADSP, LCH4 to LCH5)
- DMA_P2M_PE0_LCH9LCH10_INT_REQ_CL: 4009_6150H (ACPU, LCH9 to LCH10)
- DMA_P2M_DSP_LCH9LCH10_INT_REQ_CL: 4009_6450H (ADSP, LCH9 to LCH10)
- DMA_P2M_PE0_LCH12LCH14_INT_REQ_CL: 4009_6170H (ACPU, LCH12 to LCH14)
- DMA_P2M_DSP_LCH12LCH14_INT_REQ_CL: 4009_6470H (ADSP, LCH12 to LCH14)

The bit assignment for LCH0 to LCH3 is shown below. The other channels have the same structure. However, the timeout interrupt (INT_TIME) occurs only on LCH0 to LCH3 and LCH7, so the bits assigned to the timeout interrupt are not available for other channels (i.e., they are reserved).

31	30	29	28	27	26	25	24
Reserved	P2M_LCH3_INT_ERROR_W_REQ_CL	P2M_LCH3_INT_BLOCK_W_REQ_CL	P2M_LCH3_INT_LENG_W_REQ_CL	P2M_LCH3_INT_TIME_R_REQ_CL	P2M_LCH3_INT_ERROR_R_REQ_CL	Reserved	

23	22	21	20	19	18	17	16
Reserved	P2M_LCH2_INT_ERROR_W_REQ_CL	P2M_LCH2_INT_BLOCK_W_REQ_CL	P2M_LCH2_INT_LENG_W_REQ_CL	P2M_LCH2_INT_TIME_R_REQ_CL	P2M_LCH2_INT_ERROR_R_REQ_CL	Reserved	

15	14	13	12	11	10	9	8
Reserved	P2M_LCH1_INT_ERROR_W_REQ_CL	P2M_LCH1_INT_BLOCK_W_REQ_CL	P2M_LCH1_INT_LENG_W_REQ_CL	P2M_LCH1_INT_TIME_R_REQ_CL	P2M_LCH1_INT_ERROR_R_REQ_CL	Reserved	

7	6	5	4	3	2	1	0
Reserved	P2M_LCH0_INT_ERROR_W_REQ_CL	P2M_LCH0_INT_BLOCK_W_REQ_CL	P2M_LCH0_INT_LENG_W_REQ_CL	P2M_LCH0_INT_TIME_R_REQ_CL	P2M_LCH0_INT_ERROR_R_REQ_CL	Reserved	

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	–	31	–	Reserved. When this bit is read, 0 is returned.
P2M_LCH3_INT_ ERROR_W_REQ_CL	W	30	0	Clears the P2M LCH3 error interrupt source.
P2M_LCH3_INT_ BLOCK_W_REQ_CL	W	29	0	Clears the P2M LCH3 block interrupt source.
P2M_LCH3_INT_ LENG_W_REQ_CL	W	28	0	Clears the P2M LCH3 length interrupt source.
P2M_LCH3_INT_ TIME_R_REQ_CL	W	27	0	Clears the P2M LCH3 timeout interrupt source.
P2M_LCH3_INT_ ERROR_R_REQ_CL	W	26	0	Clears the P2M LCH3 error interrupt source.
Reserved	–	25:23	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH2_INT_ ERROR_W_REQ_CL	W	22	0	Clears the P2M LCH2 error interrupt source.
P2M_LCH2_INT_ BLOCK_W_REQ_CL	W	21	0	Clears the P2M LCH2 block interrupt source.
P2M_LCH2_INT_ LENG_W_REQ_CL	W	20	0	Clears the P2M LCH2 length interrupt source.
P2M_LCH2_INT_ TIME_R_REQ_CL	W	19	0	Clears the P2M LCH2 timeout interrupt source.
P2M_LCH2_INT_ ERROR_R_REQ_CL	W	18	0	Clears the P2M LCH2 error interrupt source.
Reserved	–	17:15	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH1_INT_ ERROR_W_REQ_CL	W	14	0	Clears the P2M LCH1 error interrupt source.
P2M_LCH1_INT_ BLOCK_W_REQ_CL	W	13	0	Clears the P2M LCH1 block interrupt source.
P2M_LCH1_INT_ LENG_W_REQ_CL	W	12	0	Clears the P2M LCH1 length interrupt source.
P2M_LCH1_INT_ TIME_R_REQ_CL	W	11	0	Clears the P2M LCH1 timeout interrupt source.
P2M_LCH1_INT_ ERROR_R_REQ_CL	W	10	0	Clears the P2M LCH1 error interrupt source.
Reserved	–	9:7	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH0_INT_ ERROR_W_REQ_CL	W	6	0	Clears the P2M LCH0 error interrupt source.
P2M_LCH0_INT_ BLOCK_W_REQ_CL	W	5	0	Clears the P2M LCH0 block interrupt source.

Remark 0: No operation (retains the current setting), 1: Clears the interrupt source

(2/2)

Name	R/W	Bit	After Reset	Function
P2M_LCH0_INT_ LENG_W_REQ_CL	W	4	0	P2M LCH0 length interrupt source.
P2M_LCH0_INT_ TIME_R_REQ_CL	W	3	0	P2M LCH0 timeout interrupt source.
P2M_LCH0_INT_ ERROR_R_REQ_CL	W	2	0	Clears the P2M LCH0 error interrupt source.
Reserved	–	1:0	–	Reserved. When these bits are read, 0 is returned for each bit.

(6) P2M interrupt output destination setting register

This register (DMA_P2M_LCH0LCH14_INT_SEL: 4009_6800H) specifies the destinations to which interrupt signals are output.

31	30	29	28	27	26	25	24
Reserved		P2M_LCH14_INT_SEL		P2M_LCH13_INT_SEL		P2M_LCH12_INT_SEL	
23	22	21	20	19	18	17	16
Reserved		P2M_LCH10_INT_SEL		P2M_LCH9_INT_SEL		P2M_LCH8_INT_SEL	
15	14	13	12	11	10	9	8
Reserved				P2M_LCH5_INT_SEL		P2M_LCH4_INT_SEL	
7	6	5	4	3	2	1	0
P2M_LCH3_INT_SEL		P2M_LCH2_INT_SEL		P2M_LCH1_INT_SEL		P2M_LCH0_INT_SEL	

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	–	31:30	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH14_INT_SEL	R/W	29:28	0	Specifies the P2M LCH14 interrupt output destination.
P2M_LCH13_INT_SEL	R/W	27:26	0	Specifies the P2M LCH13 interrupt output destination.
P2M_LCH12_INT_SEL	R/W	25:24	0	Specifies the P2M LCH12 interrupt output destination.
Reserved	–	23:22	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH10_INT_SEL	R/W	21:20	0	Specifies the P2M LCH10 interrupt output destination.
P2M_LCH9_INT_SEL	R/W	19:18	0	Specifies the P2M LCH9 interrupt output destination.
Reserved	–	17:12	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCH5_INT_SEL	R/W	11:10	0	Specifies the P2M LCH5 interrupt output destination.
P2M_LCH4_INT_SEL	R/W	9:8	0	Specifies the P2M LCH4 interrupt output destination.
P2M_LCH3_INT_SEL	R/W	7:6	0	Specifies the P2M LCH3 interrupt output destination.
P2M_LCH2_INT_SEL	R/W	5:4	0	Specifies the P2M LCH2 interrupt output destination.
P2M_LCH1_INT_SEL	R/W	3:2	0	Specifies the P2M LCH1 interrupt output destination.
P2M_LCH0_INT_SEL	R/W	1:0	0	Specifies the P2M LCH0 interrupt output destination.

Remark 00: ACPU (default), 01: Reserved, 10: Reserved, 11: ADSP

2.3.9 P2M LCHx parameter setting registers

These registers define the settings for each P2M logical channel. The letter “x” in LCHx represents a channel number, which ranges from 0 to 14 for P2M.

Channels LCH6 and LCH8 are reserved channels (unused channels).

(1) P2M LCHx source address registers

These registers (DMA_P2M_LCHx_AADD) specify the transfer source addresses (fixed address) in byte units. If the 8-bit width is selected as the transfer bit width using the mode register, the address can be set in byte units.

Likewise, if the 16-bit width is selected, the address can be set in halfwords and if 32-bit width is selected it can be set in words.

- DMA_P2M_LCH0_AADD: 4009_7000H (LCH0)
- DMA_P2M_LCH1_AADD: 4009_7100H (LCH1)
- DMA_P2M_LCH2_AADD: 4009_7200H (LCH2)
- DMA_P2M_LCH3_AADD: 4009_7300H (LCH3)
- DMA_P2M_LCH4_AADD: 4009_7400H (LCH4)
- DMA_P2M_LCH5_AADD: 4009_7500H (LCH5)
- DMA_P2M_LCH9_AADD: 4009_7900H (LCH9)
- DMA_P2M_LCH10_AADD: 4009_7A00H (LCH10)
- DMA_P2M_LCH12_AADD: 4009_7C00H (LCH12)
- DMA_P2M_LCH13_AADD: 4009_7D00H (LCH13)
- DMA_P2M_LCH14_AADD: 4009_7E00H (LCH14)

31	30	29	28	27	26	25	24
P2M_LCHx_AADD							
23	22	21	20	19	18	17	16
P2M_LCHx_AADD							
15	14	13	12	11	10	9	8
P2M_LCHx_AADD							
7	6	5	4	3	2	1	0
P2M_LCHx_AADD							

Name	R/W	Bit	After Reset	Function
P2M_LCHx_AADD	R/W	31:0	0	Specifies the P2M LCHx source address.

(2) P2M LCHx destination address registers

These registers (DMA_P2M_LCHx_BADD) specify the transfer destination start addresses in byte units.

Remark The valid bit varies depending on the bit width set by a mode register. See **4.1.1 Restrictions on parameter settings**.

- DMA_P2M_LCH0_BADD: 4009_7020H (LCH0)
- DMA_P2M_LCH1_BADD: 4009_7120H (LCH1)
- DMA_P2M_LCH2_BADD: 4009_7220H (LCH2)
- DMA_P2M_LCH3_BADD: 4009_7320H (LCH3)
- DMA_P2M_LCH4_BADD: 4009_7420H (LCH4)
- DMA_P2M_LCH5_BADD: 4009_7520H (LCH5)
- DMA_P2M_LCH9_BADD: 4009_7920H (LCH9)
- DMA_P2M_LCH10_BADD: 4009_7A20H (LCH10)
- DMA_P2M_LCH12_BADD: 4009_7C20H (LCH12)
- DMA_P2M_LCH13_BADD: 4009_7D20H (LCH13)
- DMA_P2M_LCH14_BADD: 4009_7E20H (LCH14)

31	30	29	28	27	26	25	24
P2M_LCHx_BADD							
23	22	21	20	19	18	17	16
P2M_LCHx_BADD							
15	14	13	12	11	10	9	8
P2M_LCHx_BADD							
7	6	5	4	3	2	1	0
P2M_LCHx_BADD							

Name	R/W	Bit	After Reset	Function
P2M_LCHx_BADD	R/W	31:0	0	Specifies the P2M LCHx destination address (start address).

(3) P2M LCHx destination address pointer registers

These registers (DMA_P2M_LCHx_BADP) store the transfer destination addresses being accessed.

Remark The valid bit varies depending on the bit width set by a mode register. See **4.1.1 Restrictions on parameter settings**.

- DMA_P2M_LCH0_BADP: 4009_7024H (LCH0)
- DMA_P2M_LCH1_BADP: 4009_7124H (LCH1)
- DMA_P2M_LCH2_BADP: 4009_7224H (LCH2)
- DMA_P2M_LCH3_BADP: 4009_7324H (LCH3)
- DMA_P2M_LCH4_BADP: 4009_7424H (LCH4)
- DMA_P2M_LCH5_BADP: 4009_7524H (LCH5)
- DMA_P2M_LCH9_BADP: 4009_7924H (LCH9)
- DMA_P2M_LCH10_BADP: 4009_7A24H (LCH10)
- DMA_P2M_LCH12_BADP: 4009_7C24H (LCH12)
- DMA_P2M_LCH13_BADP: 4009_7D24H (LCH13)
- DMA_P2M_LCH14_BADP: 4009_7E24H (LCH14)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
P2M_LCHx_BADP							
15	14	13	12	11	10	9	8
P2M_LCHx_BADP							
7	6	5	4	3	2	1	0
P2M_LCHx_BADP							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:24	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCHx_BADP	R	23:0	0	Stores the transfer address being accessed during transfer via P2M LCHx.

(4) P2M LCHx destination address offset registers

These registers (DMA_P2M_LCHx_BOFF) specify the offset between blocks on the destination side, in byte units. Up to 65,535 bytes can be specified.

Remark The offset register and block size register need to be set so that their combined value is in units of words (4 bytes); otherwise, the normal DMA operation is not guaranteed.

- DMA_P2M_LCH0_BOFF: 4009_7028H (LCH0)
- DMA_P2M_LCH1_BOFF: 4009_7128H (LCH1)
- DMA_P2M_LCH2_BOFF: 4009_7228H (LCH2)
- DMA_P2M_LCH3_BOFF: 4009_7328H (LCH3)
- DMA_P2M_LCH4_BOFF: 4009_7428H (LCH4)
- DMA_P2M_LCH5_BOFF: 4009_7528H (LCH5)
- DMA_P2M_LCH9_BOFF: 4009_7928H (LCH9)
- DMA_P2M_LCH10_BOFF: 4009_7A28H (LCH10)
- DMA_P2M_LCH12_BOFF: 4009_7C28H (LCH12)
- DMA_P2M_LCH13_BOFF: 4009_7D28H (LCH13)
- DMA_P2M_LCH14_BOFF: 4009_7E28H (LCH14)

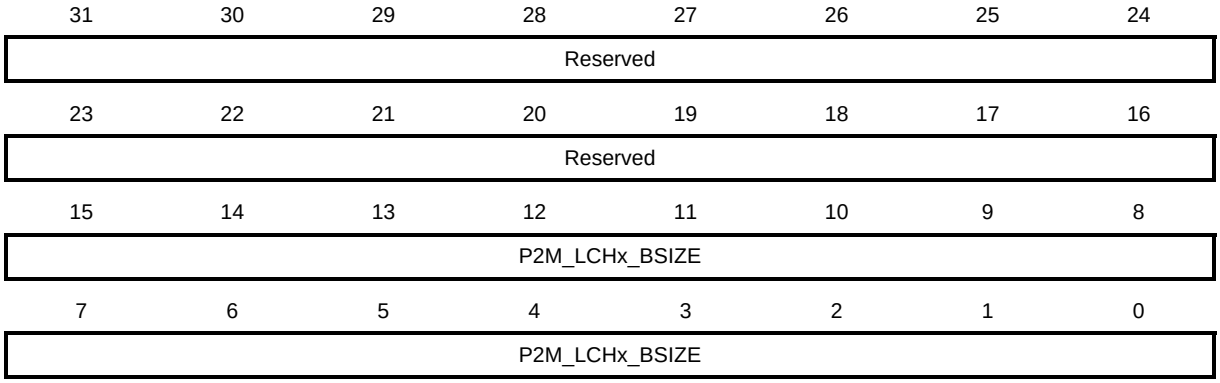
31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
P2M_LCHx_BOFF							
7	6	5	4	3	2	1	0
P2M_LCHx_BOFF							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:16	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCHx_BOFF	R/W	15:0	0	Indicates the offset between blocks on the P2M LCHx destination side in byte units. 00000000_00000000: 0 bytes (no offset) 00000000_00000001: 1 byte 00000000_00000010: 2 bytes (halfword) 00000000_00000011: 3 bytes 00000000_00000100: 4 bytes (1 word) 00000000_00000101: 5 bytes : 11111111_11111111: 65,535 bytes

(5) P2M LCHx destination block size registers

These registers (DMA_P2M_LCHx_BSIZE) specify the size of transfer blocks on the destination side, in byte units. Up to 65,535 bytes can be specified.

- DMA_P2M_LCH0_BSIZE: 4009_702CH (LCH0)
- DMA_P2M_LCH1_BSIZE: 4009_712CH (LCH1)
- DMA_P2M_LCH2_BSIZE: 4009_722CH (LCH2)
- DMA_P2M_LCH3_BSIZE: 4009_732CH (LCH3)
- DMA_P2M_LCH4_BSIZE: 4009_742CH (LCH4)
- DMA_P2M_LCH5_BSIZE: 4009_752CH (LCH5)
- DMA_P2M_LCH9_BSIZE: 4009_792CH (LCH9)
- DMA_P2M_LCH10_BSIZE: 4009_7A2CH (LCH10)
- DMA_P2M_LCH12_BSIZE: 4009_7C2CH (LCH12)
- DMA_P2M_LCH13_BSIZE: 4009_7D2CH (LCH13)
- DMA_P2M_LCH14_BSIZE: 4009_7E2CH (LCH14)



Name	R/W	Bit	After Reset	Function
Reserved	–	31:16	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCHx_BSIZE	R/W	15:0	0	Specifies the size of P2M LCHx transfer blocks on the destination side. 00000000_00000000: Setting prohibited 00000000_00000001: 1 byte 00000000_00000010: 2 bytes (halfword) 00000000_00000011: 3 bytes 00000000_00000100: 4 bytes (1 word) 00000000_00000101: 5 bytes : 11111111_11111111: 65,535 bytes

Cautions 1. Setting "0" in this register may cause a block interrupt to occur continuously. In this case, the normal DMA operation is not guaranteed.

2. To prevent a block interrupt from occurring for each block size, set the block size to the same value as the length. (In this case, a block interrupt and a length interrupt occur simultaneously when DMA transfer is completed.)

(6) P2M LCHx destination block count registers

These registers (DMA_P2M_LCHx_BSIZE_COUNT) operate differently when read and written.

When these registers are written, the number of blocks transferred in a loop during repeat transfer is set. When these registers are read, the remaining number of transfer blocks on the destination side is read out. The specified number of blocks is decremented each time block transfer ends, and the remaining count is shown in this register. To perform repeat transfer, the offset must be set to 0 (one-dimensional transfer).

- DMA_P2M_LCH0_BSIZE_COUNT: 4009_7030H (LCH0)
- DMA_P2M_LCH1_BSIZE_COUNT: 4009_7130H (LCH1)
- DMA_P2M_LCH2_BSIZE_COUNT: 4009_7230H (LCH2)
- DMA_P2M_LCH3_BSIZE_COUNT: 4009_7330H (LCH3)
- DMA_P2M_LCH4_BSIZE_COUNT: 4009_7430H (LCH4)
- DMA_P2M_LCH5_BSIZE_COUNT: 4009_7530H (LCH5)
- DMA_P2M_LCH9_BSIZE_COUNT: 4009_7930H (LCH9)
- DMA_P2M_LCH10_BSIZE_COUNT: 4009_7A30H (LCH10)
- DMA_P2M_LCH12_BSIZE_COUNT: 4009_7C30H (LCH12)
- DMA_P2M_LCH13_BSIZE_COUNT: 4009_7D30H (LCH13)
- DMA_P2M_LCH14_BSIZE_COUNT: 4009_7E30H (LCH14)

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved		P2M_LCHx_BSIZE_COUNT					

Name	R/W	Bit	After Reset	Function
Reserved	–	31:6	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCHx_BSIZE_COUNT	R/W	5:0	0	When written: Specifies the number of blocks to be transferred in a loop during repeat transfer on the destination side. 000000: 1 block 000001: 2 blocks 000010: 3 blocks 000011: 4 blocks 000100: 5 blocks 000101: 6 blocks 000110: 7 blocks 000111: 8 blocks 001000: 9 blocks : 111111: 64 blocks When read: Indicates the number of remaining transfer blocks on the destination side. The value written to this register is set when DMA is started, and the value is decremented each time block transfer ends.

(7) P2M LCHx length registers

These registers (DMA_P2M_LCHx_LENG) specify the total amount of transfer data, in byte units. Up to 16,777,215 bytes can be specified.

If repeat mode is specified in the relevant mode register, infinite-length transfer is specified by setting the corresponding length register to 0.

Caution Do not set these registers to 0 if the repeat mode is not specified. Specifying an offset for infinite-length transfer is prohibited.

- DMA_P2M_LCH0_LENG: 4009_7040H (LCH0)
- DMA_P2M_LCH1_LENG: 4009_7140H (LCH1)
- DMA_P2M_LCH2_LENG: 4009_7240H (LCH2)
- DMA_P2M_LCH3_LENG: 4009_7340H (LCH3)
- DMA_P2M_LCH4_LENG: 4009_7440H (LCH4)
- DMA_P2M_LCH5_LENG: 4009_7540H (LCH5)
- DMA_P2M_LCH9_LENG: 4009_7940H (LCH9)
- DMA_P2M_LCH10_LENG: 4009_7A40H (LCH10)
- DMA_P2M_LCH12_LENG: 4009_7C40H (LCH12)
- DMA_P2M_LCH13_LENG: 4009_7D40H (LCH13)
- DMA_P2M_LCH14_LENG: 4009_7E40H (LCH14)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
P2M_LCHx_LENG							
15	14	13	12	11	10	9	8
P2M_LCHx_LENG							
7	6	5	4	3	2	1	0
P2M_LCHx_LENG							

Name	R/W	Bit	After Reset	Function
Reserved	–	31:24	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCHx_LENG	R/W	23:0	0	Specifies the total amount of data transferred via P2M LCHx, in byte units. 00000000_00000000_00000000: Infinite-length transfer 00000000_00000000_00000001: 1 byte 00000000_00000000_00000010: 2 bytes 00000000_00000000_00000011: 3 bytes 00000000_00000000_00000100: 4 bytes : 11111111_11111111_11111111: 16,777,215 bytes

(3) P2M LCHx read length count registers

These registers (DMA_P2M_LCHx_LENG_RCOUNT) store the total amount of transfer data on the source side. The total transfer length is decremented from the length specified by the corresponding length register to indicate the remaining transfer amount.

- DMA_P2M_LCH0_LENG_RCOUNT: 4009_7044H (LCH0)
- DMA_P2M_LCH1_LENG_RCOUNT: 4009_7144H (LCH1)
- DMA_P2M_LCH2_LENG_RCOUNT: 4009_7244H (LCH2)
- DMA_P2M_LCH3_LENG_RCOUNT: 4009_7344H (LCH3)
- DMA_P2M_LCH4_LENG_RCOUNT: 4009_7444H (LCH4)
- DMA_P2M_LCH5_LENG_RCOUNT: 4009_7544H (LCH5)
- DMA_P2M_LCH9_LENG_RCOUNT: 4009_7944H (LCH9)
- DMA_P2M_LCH10_LENG_RCOUNT: 4009_7A44H (LCH10)
- DMA_P2M_LCH12_LENG_RCOUNT: 4009_7C44H (LCH12)
- DMA_P2M_LCH13_LENG_RCOUNT: 4009_7D44H (LCH13)
- DMA_P2M_LCH14_LENG_RCOUNT: 4009_7E44H (LCH14)

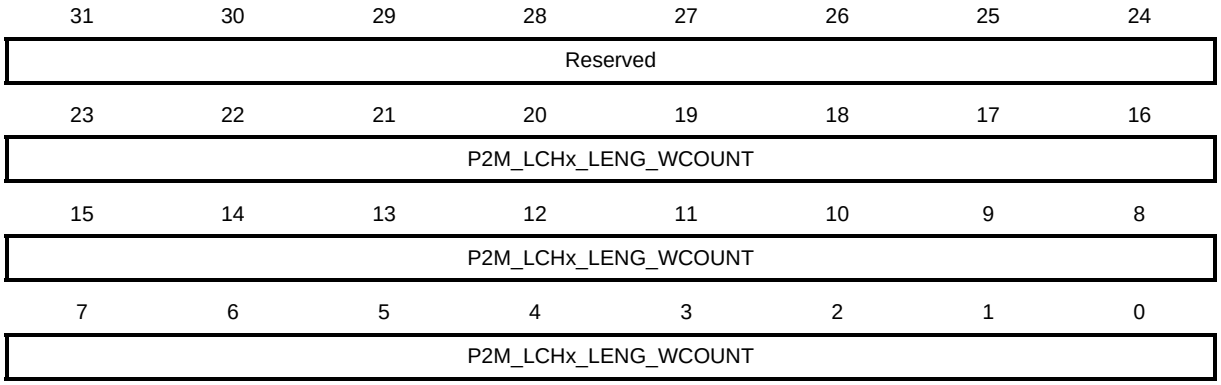
31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
P2M_LCHx_LENG_RCOUNT							
15	14	13	12	11	10	9	8
P2M_LCHx_LENG_RCOUNT							
7	6	5	4	3	2	1	0
P2M_LCHx_LENG_RCOUNT							

Name	R/W	Bit	After Reset	Function
Reserved	–	31:24	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCHx_LENG_RCOUNT	R	23:0	0	Specifies the total amount of data transferred via P2M LCHx, in byte units. 00000000_00000000_00000000: 0 bytes 00000000_00000000_00000001: 1 byte 00000000_00000000_00000010: 2 bytes 00000000_00000000_00000011: 3 bytes 00000000_00000000_00000100: 4 bytes : 11111111_11111111_11111111: 16,777,215 bytes

(9) P2M LCHx write length count registers

These registers (DMA_P2M_LCHx_LENG_WCOUNT) store the total amount of transfer data on the destination side. The total transfer length is decremented from the length specified by the corresponding length register to indicate the remaining transfer amount.

- DMA_P2M_LCH0_LENG_WCOUNT: 4009_7048H (LCH0)
- DMA_P2M_LCH1_LENG_WCOUNT: 4009_7148H (LCH1)
- DMA_P2M_LCH2_LENG_WCOUNT: 4009_7248H (LCH2)
- DMA_P2M_LCH3_LENG_WCOUNT: 4009_7348H (LCH3)
- DMA_P2M_LCH4_LENG_WCOUNT: 4009_7448H (LCH4)
- DMA_P2M_LCH5_LENG_WCOUNT: 4009_7548H (LCH5)
- DMA_P2M_LCH9_LENG_WCOUNT: 4009_7948H (LCH9)
- DMA_P2M_LCH10_LENG_WCOUNT: 4009_7A48H (LCH10)
- DMA_P2M_LCH12_LENG_WCOUNT: 4009_7C48H (LCH12)
- DMA_P2M_LCH13_LENG_WCOUNT: 4009_7D48H (LCH13)
- DMA_P2M_LCH14_LENG_WCOUNT: 4009_7E48H (LCH14)



Name	R/W	Bit	After Reset	Function
Reserved	–	31:24	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCHx_LENG_WCOUNT	R	23:0	0	Specifies the total amount of data transferred via P2M LCHx, in byte units. 00000000_00000000_00000000: 0 bytes 00000000_00000000_00000001: 1 byte 00000000_00000000_00000010: 2 bytes 00000000_00000000_00000011: 3 bytes 00000000_00000000_00000100: 4 bytes : 11111111_11111111_11111111: 16,777,215 bytes

(10) P2M LCHx mode registers

These registers (DMA_P2M_LCHx_MODE) specify transfer modes (endian, repeat, bit width, and timer settings).

To perform repeat transfer, the offset must be set to 0 (one-dimensional transfer).

- DMA_P2M_LCH0_MODE: 4009_7050H (LCH0)
- DMA_P2M_LCH1_MODE: 4009_7150H (LCH1)
- DMA_P2M_LCH2_MODE: 4009_7250H (LCH2)
- DMA_P2M_LCH3_MODE: 4009_7350H (LCH3)
- DMA_P2M_LCH4_MODE: 4009_7450H (LCH4)
- DMA_P2M_LCH5_MODE: 4009_7550H (LCH5)
- DMA_P2M_LCH9_MODE: 4009_7950H (LCH9)
- DMA_P2M_LCH10_MODE: 4009_7A50H (LCH10)
- DMA_P2M_LCH12_MODE: 4009_7C50H (LCH12)
- DMA_P2M_LCH13_MODE: 4009_7D50H (LCH13)
- DMA_P2M_LCH14_MODE: 4009_7E50H (LCH14)

The timer count setting (P2M_LCHx_MODE_TIME) is only valid for LCH0, LCH1, and LCH2. For other channels, so the bits assigned to the timeout interrupt are not available for other channels (i.e., they are reserved).

31 30	29 28	27 26	25 24
P2M_LCHx_MODE_ENDI_W_HH	P2M_LCHx_MODE_ENDI_W_HL	P2M_LCHx_MODE_ENDI_W_LH	P2M_LCHx_MODE_ENDI_W_LL

23 22	21 20	19 18	17 16
P2M_LCHx_MODE_ENDI_R_HH	P2M_LCHx_MODE_ENDI_R_HL	P2M_LCHx_MODE_ENDI_R_LH	P2M_LCHx_MODE_ENDI_R_LL

15 14 13 12 11 10 9	8
Reserved	P2M_LCHx_BMODE_REPEAT

7 6	5 4	3	2	1 0
Reserved	P2M_LCHx_MODE_BIT	Reserved	P2M_LCHx_MODE_TIME	Reserved

Name	R/W	Bit	After Reset	Function
P2M_LCHx_MODE_ ENDI_W_HH	R/W	31:30	E4H	Specifies the byte lane for writing data to the transfer destination. 00: Byte 0 01: Byte 1 10: Byte 2 11: Byte 3
P2M_LCHx_MODE_ ENDI_W_HL	R/W	29:28		
P2M_LCHx_MODE_ ENDI_W_LH	R/W	27:26		
P2M_LCHx_MODE_ ENDI_W_LL	R/W	25:24		
P2M_LCHx_MODE_ ENDI_R_HH	R/W	23:22	E4H	Specifies the byte lane for reading transfer data from the source side. 00: Byte 0 01: Byte 1 10: Byte 2 11: Byte 3
P2M_LCHx_MODE_ ENDI_R_HL	R/W	21:20		
P2M_LCHx_MODE_ ENDI_R_LH	R/W	19:18		
P2M_LCHx_MODE_ ENDI_R_LL	R/W	17:16		
Reserved	R	15:6	0	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCHx_BMODE_ REPEAT	R/W	8	0	Specifies the transfer destination to repeat mode. 0: Does not specify repeat mode, 1: Specifies repeat mode.
Reserved	R	7:6	00	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCHx_MODE_ BIT	R/W	5:4	00	Specifies the transfer bit width. 00: 32 bits, 01: 16 bits, 10: 8 bits, 11: Setting prohibited
Reserved	R	3	0	Reserved. When this bit is read, 0 is returned.
P2M_LCHx_MODE_ TIME	R/W	2	0	Specifies whether the timer count is used. 0: Does not use the timer, 1: Uses the timer (UART0 to UART2 only).
Reserved	R	1:0	00	Reserved. When these bits are read, 0 is returned for each bit.

Caution When restarting a logical channel that has timed out, P2M_LCHx_MODE_TIME needs to be set to "1," then "0," and then "1" again in order to preset the timer. Be sure to insert two or more DMA_TCLK clock cycles between setting "0" (low level) and setting "1" again.
Be sure to supply a timer clock (DMA_TCLK) when using a timer function; otherwise, DMA clock control may malfunction.

(11) P2M LCHx timer registers

These registers (DMA_P2M_LCHx_TIME) specify the time allowed to elapse until the DMA transfer is forced to end. If no DMA request has been issued for a specific period, DMA transfer is forced to end if the time specified in this register expires. Up to 24 bits can be set.

This function is valid only for memory-to-UART channels (LCH0, LCH1, and LCH2).

- DMA_P2M_LCH0_TIME: 4009_7054H (LCH0)
- DMA_P2M_LCH1_TIME: 4009_7154H (LCH1)
- DMA_P2M_LCH2_TIME: 4009_7254H (LCH2)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
P2M_LCHx_TIME							
15	14	13	12	11	10	9	8
P2M_LCHx_TIME							
7	6	5	4	3	2	1	0
P2M_LCHx_TIME							

Name	R/W	Bit	After Reset	Function
Reserved	–	31:24	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCHx_TIME	R/W	23:0	0	Specifies the time allowed to elapse before P2M LCHx operation times out.

Caution Be sure to supply a timer clock (DMA_TCLK) when using a timer function; otherwise, DMA clock control may malfunction.

(12) P2M LCHx timer count registers

These registers (DMA_P2M_LCHx_TIME_COUNT) count down the time until DMA transfer is forced to end. The time is counted down in units of the DMA_TCLK clock output from the ASMU. When the count reaches 0, DMA transfer times out and is forced to end.

This function is valid only for memory-to-UART channels (LCH0, LCH1, and LCH2).

- DMA_P2M_LCH0_TIME_COUNT: 4009_7058H (LCH0)
- DMA_P2M_LCH1_TIME_COUNT: 4009_7158H (LCH1)
- DMA_P2M_LCH2_TIME_COUNT: 4009_7258H (LCH2)

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
P2M_LCHx_TIME_COUNT							
15	14	13	12	11	10	9	8
P2M_LCHx_TIME_COUNT							
7	6	5	4	3	2	1	0
P2M_LCHx_TIME_COUNT							

Name	R/W	Bit	After Reset	Function
Reserved	–	31:24	–	Reserved. When these bits are read, 0 is returned for each bit.
P2M_LCHx_TIME_ COUNT	R	23:0	0	Stores the time allowed to elapse before P2M LCHx operation times out. DMA_TCLK is used for timer counting.

2.3.10 Interrupt index registers

(1) ACPU interrupt index register

This register (DMA_PE0_INT_INDEX: 4009_8000H) can be used to identify the channel on which an interrupt source occurred. This register is valid only for those channels for which the ACPU is selected in an interrupt output destination setting register.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							PE0_INT_INDEX
7	6	5	4	3	2	1	0
PE0_INT_INDEX							

Name	R/W	Bit	After Reset	Function
Reserved	–	31:9	–	Reserved. When these bits are read, 0 is returned for each bit.
PE0_INT_INDEX[8]	R	8	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on P2M LCH12 to LCH14.
PE0_INT_INDEX[7]	R	7	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on P2M LCH8 to LCH11.
PE0_INT_INDEX[6]	R	6	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on P2M LCH4 to LCH7.
PE0_INT_INDEX[5]	R	5	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on P2M LCH0 to LCH3.
PE0_INT_INDEX[4]	R	4	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on M2P LCH12 to LCH14.
PE0_INT_INDEX[3]	R	3	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on M2P LCH8 to LCH11.
PE0_INT_INDEX[2]	R	2	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on M2P LCH4 to LCH7.
PE0_INT_INDEX[1]	R	1	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on M2P LCH0 to LCH3.
PE0_INT_INDEX[0]	R	0	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on ACPU LCH0 to LCH3.

(2) ADSP interrupt index register

This register (DMA_DSP_INT_INDEX: 4009_800CH) can be used to identify the channel on which an interrupt source occurred. This register is valid only for those channels for which the DSP is selected in an interrupt output destination setting register.

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							DSP_INT_INDEX
7	6	5	4	3	2	1	0
DSP_INT_INDEX							

Name	R/W	Bit	After Reset	Function
Reserved	–	31:9	–	Reserved. When these bits are read, 0 is returned for each bit.
DSP_INT_INDEX[8]	R	8	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on P2M LCH12 to LCH14.
DSP_INT_INDEX[7]	R	7	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on P2M LCH8 to LCH11.
DSP_INT_INDEX[6]	R	6	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on P2M LCH4 to LCH7.
DSP_INT_INDEX[5]	R	5	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on P2M LCH0 to LCH3.
DSP_INT_INDEX[4]	R	4	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on M2P LCH12 to LCH14.
DSP_INT_INDEX[3]	R	3	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on M2P LCH8 to LCH11.
DSP_INT_INDEX[2]	R	2	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on M2P LCH4 to LCH7.
DSP_INT_INDEX[1]	R	1	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on M2P LCH0 to LCH3.
DSP_INT_INDEX[0]	R	0	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on ACPU LCH0 to LCH3.

(3) ACPU interrupt index 2 register

This register (DMA_PE0_INT_INDEX2: 4009_8100H) can be used to identify the channel on which an interrupt source occurred. One difference from DMA_PE0_INT_INDEX is that a logical channel is assigned to each bit. Therefore, on which logical channel an interrupt source has occurred can be checked through a single read of this register.

31	30	29	28	27	26	25	24
Reserved		PE0_INDEX_PCH3_LCH14	PE0_INDEX_PCH3_LCH13	PE0_INDEX_PCH3_LCH12	Reserved	PE0_INDEX_PCH3_LCH10	PE0_INDEX_PCH3_LCH9

23	22	21	20	19	18	17	16
Reserved	PE0_INDEX_PCH3_LCH5	PE0_INDEX_PCH3_LCH4	PE0_INDEX_PCH3_LCH3	PE0_INDEX_PCH3_LCH2	PE0_INDEX_PCH3_LCH1	PE0_INDEX_PCH3_LCH0	PE0_INDEX_PCH2_LCH14

15	14	13	12	11	10	9	8
PE0_INDEX_PCH2_LCH13	PE0_INDEX_PCH2_LCH12	Reserved	PE0_INDEX_PCH2_LCH10	PE0_INDEX_PCH2_LCH9	Reserved	PE0_INDEX_PCH2_LCH5	PE0_INDEX_PCH2_LCH4

7	6	5	4	3	2	1	0
PE0_INDEX_PCH2_LCH3	PE0_INDEX_PCH2_LCH2	PE0_INDEX_PCH2_LCH1	PE0_INDEX_PCH2_LCH0	PE0_INDEX_PCH0_LCH3	PE0_INDEX_PCH0_LCH2	PE0_INDEX_PCH0_LCH1	PE0_INDEX_PCH0_LCH0

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	–	31:30	–	Reserved. When these bits are read, 0 is returned for each bit.
PE0_INDEX_PCH3_LCH14	R	29	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH3 LCH14.
PE0_INDEX_PCH3_LCH13	R	28	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH3 LCH13.
PE0_INDEX_PCH3_LCH12	R	27	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH3 LCH12.
Reserved	R	26	–	Reserved. When this bit is read, 0 is returned.
PE0_INDEX_PCH3_LCH10	R	25	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH3 LCH10.
PE0_INDEX_PCH3_LCH9	R	24	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH3 LCH9.
Reserved	R	23	–	Reserved. When this bit is read, 0 is returned.
PE0_INDEX_PCH3_LCH5	R	22	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH3 LCH5.
PE0_INDEX_PCH3_LCH4	R	21	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH3 LCH4.
PE0_INDEX_PCH3_LCH3	R	20	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH3 LCH3.
PE0_INDEX_PCH3_LCH2	R	19	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH3 LCH2.
PE0_INDEX_PCH3_LCH1	R	18	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH3 LCH1.

(2/2)

Name	R/W	Bit	After Reset	Function
PE0_INDEX_PCH3_ LCH0	R	17	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH3 LCH0.
PE0_INDEX_PCH2_ LCH14	R	16	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH2 LCH14.
PE0_INDEX_PCH2_ LCH13	R	15	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH2 LCH13.
PE0_INDEX_PCH2_ LCH12	R	14	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH2 LCH12.
Reserved	R	13	–	Reserved. When this bit is read, 0 is returned.
PE0_INDEX_PCH2_ LCH10	R	12	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH2 LCH10.
PE0_INDEX_PCH2_ LCH9	R	11	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH2 LCH9.
Reserved	R	10	–	Reserved. When this bit is read, 0 is returned.
PE0_INDEX_PCH2_ LCH5	R	9	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH2 LCH5.
PE0_INDEX_PCH2_ LCH4	R	8	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH2 LCH4.
PE0_INDEX_PCH2_ LCH3	R	7	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH2 LCH3.
PE0_INDEX_PCH2_ LCH2	R	6	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH2 LCH2.
PE0_INDEX_PCH2_ LCH1	R	5	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH2 LCH1.
PE0_INDEX_PCH2_ LCH0	R	4	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH2 LCH0.
PE0_INDEX_PCH0_ LCH3	R	3	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH0 LCH3.
PE0_INDEX_PCH0_ LCH2	R	2	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH0 LCH2.
PE0_INDEX_PCH0_ LCH1	R	1	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH0 LCH1.
PE0_INDEX_PCH0_ LCH0	R	0	0	Interrupt index register for ACPU Indicates that an interrupt source occurred on PCH0 LCH0.

(4) ADSP interrupt index 2 register

This register (DMA_DSP_INT_INDEX2: 4009_810CH) can be used to identify the channel on which an interrupt source occurred. One difference from DMA_DSP_INT_INDEX is that a logical channel is assigned to each bit. Therefore, on which logical channel an interrupt source has occurred can be checked through a single read of this register.

31	30	29	28	27	26	25	24
Reserved		DSP_INDEX_PCH3_LCH14	DSP_INDEX_PCH3_LCH13	DSP_INDEX_PCH3_LCH12	Reserved	DSP_INDEX_PCH3_LCH10	DSP_INDEX_PCH3_LCH9

23	22	21	20	19	18	17	16
Reserved	DSP_INDEX_PCH3_LCH5	DSP_INDEX_PCH3_LCH4	DSP_INDEX_PCH3_LCH3	DSP_INDEX_PCH3_LCH2	DSP_INDEX_PCH3_LCH1	DSP_INDEX_PCH3_LCH0	DSP_INDEX_PCH2_LCH14

15	14	13	12	11	10	9	8
DSP_INDEX_PCH2_LCH13	DSP_INDEX_PCH2_LCH12	Reserved	DSP_INDEX_PCH2_LCH10	DSP_INDEX_PCH2_LCH9	Reserved	DSP_INDEX_PCH2_LCH5	DSP_INDEX_PCH2_LCH4

7	6	5	4	3	2	1	0
DSP_INDEX_PCH2_LCH3	DSP_INDEX_PCH2_LCH2	DSP_INDEX_PCH2_LCH1	DSP_INDEX_PCH2_LCH0	DSP_INDEX_PCH0_LCH3	DSP_INDEX_PCH0_LCH2	DSP_INDEX_PCH0_LCH1	DSP_INDEX_PCH0_LCH0

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	–	31: 30	–	Reserved. When these bits are read, 0 is returned for each bit.
DSP_INDEX_PCH3_LCH14	R	29	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH3 LCH14.
DSP_INDEX_PCH3_LCH13	R	28	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH3 LCH13.
DSP_INDEX_PCH3_LCH12	R	27	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH3 LCH12.
Reserved	R	26	–	Reserved. When this bit is read, 0 is returned.
DSP_INDEX_PCH3_LCH10	R	25	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH3 LCH10.
DSP_INDEX_PCH3_LCH9	R	24	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH3 LCH9.
Reserved	R	23	–	Reserved. When this bit is read, 0 is returned.
DSP_INDEX_PCH3_LCH5	R	22	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH3 LCH5.
DSP_INDEX_PCH3_LCH4	R	21	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH3 LCH4.
DSP_INDEX_PCH3_LCH3	R	20	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH3 LCH3.
DSP_INDEX_PCH3_LCH2	R	19	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH3 LCH2.

(2/2)

Name	R/W	Bit	After Reset	Function
DSP_INDEX_PCH3_LCH1	R	18	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH3 LCH1.
DSP_INDEX_PCH3_LCH0	R	17	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH3 LCH0.
DSP_INDEX_PCH2_LCH14	R	16	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH2 LCH14.
DSP_INDEX_PCH2_LCH13	R	15	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH2 LCH13.
DSP_INDEX_PCH2_LCH12	R	14	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH2 LCH12.
Reserved	R	13	–	Reserved. When this bit is read, 0 is returned.
DSP_INDEX_PCH2_LCH10	R	12	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH2 LCH10.
DSP_INDEX_PCH2_LCH9	R	11	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH2 LCH9.
Reserved	R	10	–	Reserved. When this bit is read, 0 is returned.
DSP_INDEX_PCH2_LCH5	R	9	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH2 LCH5.
DSP_INDEX_PCH2_LCH4	R	8	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH2 LCH4.
DSP_INDEX_PCH2_LCH3	R	7	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH2 LCH3.
DSP_INDEX_PCH2_LCH2	R	6	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH2 LCH2.
DSP_INDEX_PCH2_LCH1	R	5	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH2 LCH1.
DSP_INDEX_PCH2_LCH0	R	4	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH2 LCH0.
DSP_INDEX_PCH0_LCH3	R	3	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH0 LCH3.
DSP_INDEX_PCH0_LCH2	R	2	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH0 LCH2.
DSP_INDEX_PCH0_LCH1	R	1	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH0 LCH1.
DSP_INDEX_PCH0_LCH0	R	0	0	Interrupt index register for ADSP Indicates that an interrupt source occurred on PCH0 LCH0.

CHAPTER 3 DESCRIPTION OF FUNCTIONS

3.1 Overview of DMA Transfer

DMA transfers are classified into the types shown in the following table. A separate physical channel is provided for each transfer type.

Physical channel 1 (PCH1) does not exist

Table 3-1. Transfer Types and Number of Channels

Transfer Type	Memory-to-Memory	Memory-to-Peripheral	Peripheral-to-Memory
Physical channel	PCH0	PCH2	PCH3
Number of logical channels	4	11	11
Two-dimensional transfer	○	△ Note 1	△ Note 1
Timer function	×	△ Note 2	△ Note 2
Reverse transfer	○	×	×

Notes 1. Two-dimensional transfer is supported only on the memory side.

2. The timer function is supported only for UART channels (LCH0, LCH1, LCH2).

Remark ○: Supported, △: Supported with certain conditions, ×: Not supported

3.2 Physical Channel Functions

3.2.1 Memory-to-memory transfer (PCH0)

Memory-to-memory transfer sends data from a source address to a destination address, according to the ACPU register settings. The areas AB0, MEMC and SRC are subject to memory-to-memory transfer, in any combinations, except for transfer that involves overwriting (such as right-scrolling of an image). The minimum unit of transfer is one byte.

Physical channel 0 (PCH0) is a channel dedicated to memory-to-memory transfer and is controlled according to the ACPU register settings. PCH0 has four logical channels (LCH0 to LCH3) and they are arbitrated on a per-transaction basis in a round-robin fashion.

Table 3-2. Memory-to-Memory Transfer Combinations

Memory-to-Memory Transfer	AB0 Area	SRC	MEMC Area
AB0 area	○	○	○
SRC area	○	○	○
MEMC area	○	○	○

Remark ○: Combination available

(1) LCH arbitration control

(a) Read control block

Round-robin arbitration is performed among those logical channels for which starting of DMA transfer is directed in the DMA start control register (DMA_ARM_CONT), to select a logical channel subject to transfer.

Note that a logical channel cannot participate in arbitration if the FIFO buffer assigned to that channel does not have 68 bytes (64 bytes + 4 bytes) or more of free space.

(b) Write control block

As with the read control block, round-robin arbitration is performed among those logical channels for which starting of DMA transfer is directed in the DMA start control register, to select a logical channel subject to transfer. Note that a logical channel can participate in arbitration only if the FIFO buffer assigned to that channel has 64 bytes or more of valid data or if the last data transfer completion signal from the read control block has been asserted indicating that the amount of data transferred has reached the total transfer data length specified.

(2) AHB access control

(a) Read control block

To enhance the AHB transfer efficiency, only 8-beat incrementing burst (INCR8) and 16-beat incrementing burst (INCR16) are used. The transfer start address for INCR16 must be on a 64-byte boundary, and the transfer start address for INCR8 must be on a 32-byte address boundary. If data to be transferred is 32 bytes or less, an INCR8 burst including null data is sent.

If data to be transferred is less than 32 bytes, the data is transferred using the INCR8 burst size and the DMA controller receives only necessary data into the FIFO buffer. Unnecessary data is discarded when data is stored in the FIFO buffer.

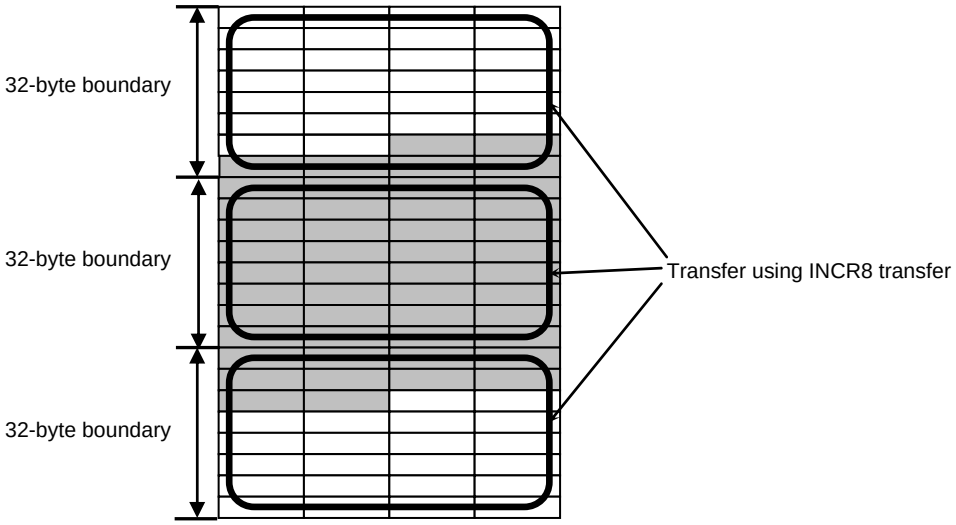
The transfer burst size is selected according to the rules described in Table 3-3.

Table 3-3. Transfer Burst Size Selection (Read Control Block)

Transfer Start Address	Transfer Burst Size
64-byte boundary	INCR16 (16-beat burst)
32-byte boundary	INCR8 (8-beat burst)
Other	INCR8 (8-beat burst), unnecessary data is discarded.

An image of AHB read transfer is shown below.

Figure 3-1. Transfer Burst Size Selection Example (for AHB Read)



Remark : Valid transferred data

(b) Write control block

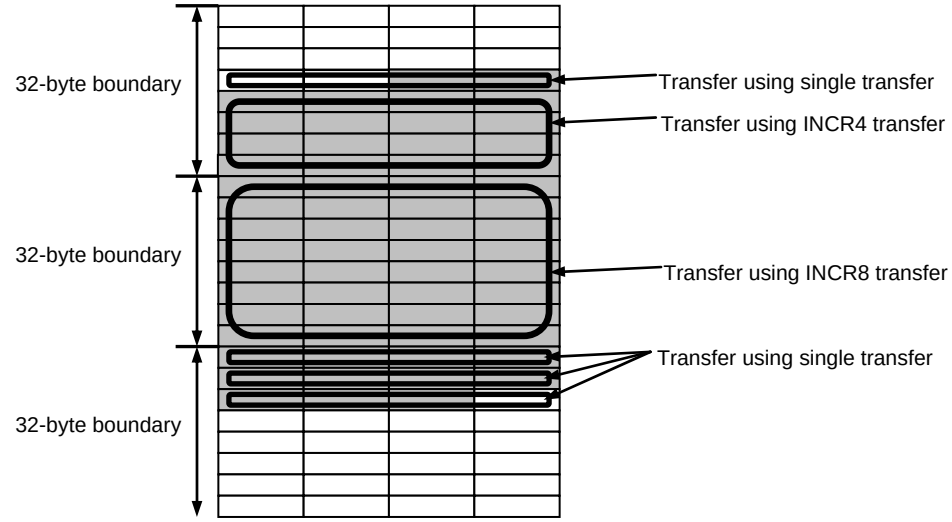
The burst size for AHB transfers by the write control block is basically 16-beat incrementing burst (INCR16). The transfer start address for INCR16 must be on a 64-byte boundary. If the transfer start address is not on a 64-byte boundary, the data is segmented so that the largest possible transfer burst size is selected according to the rules described in Table 3-4.

Table 3-4. Transfer Burst Size Selection (Write Control Block)

Transfer Start Address	Transfer Burst Size
64-byte boundary	INCR16 (16-beat burst)
32-byte boundary	INCR8 (8-beat burst)
16-byte boundary	INCR4 (4-beat burst)
Other	Single (including byte/halfword transfer)

An image of AHB write transfer is shown below.

Figure 3-2. Transfer Burst Size Selection Example (for AHB Write)



Remark : Valid transferred data

(3) Address control

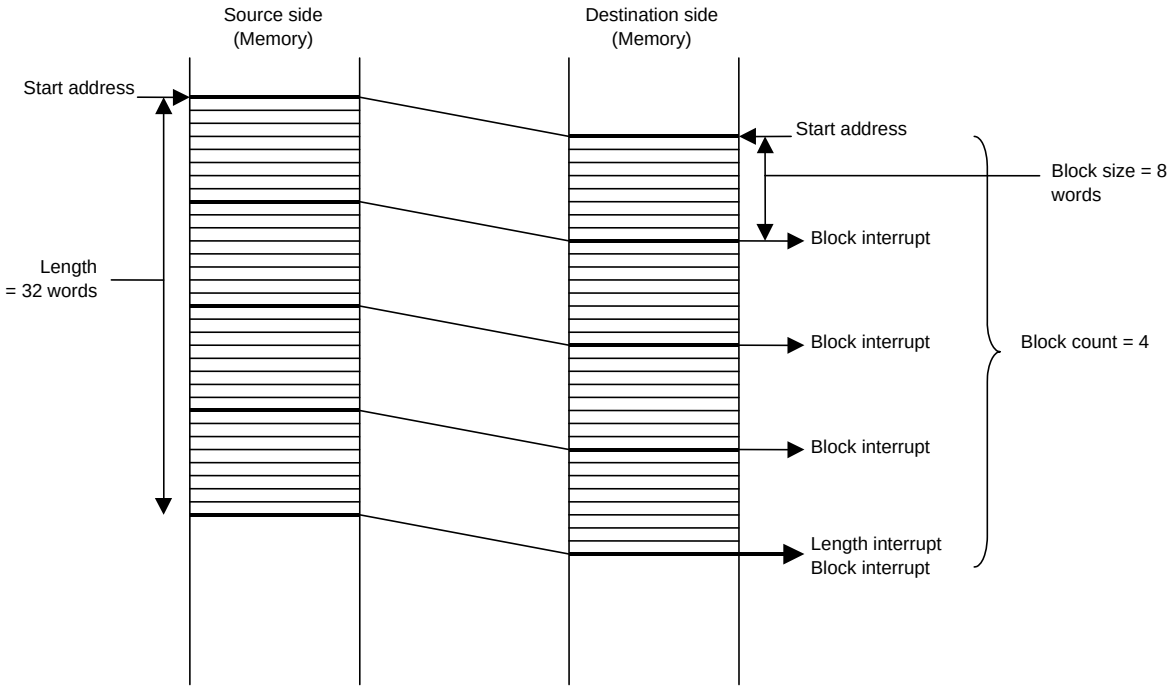
(a) Memory-to-memory transfer (one-dimensional transfer)

Memory-to-memory transfer supports the offset function for both the source and destination sides.

Figure 3-3 shows an example of one-dimensional memory-to-memory transfer.

The transfer is continued by incrementing the address value on both the source and destination sides, from the start address. When the specified block size or length of data has been transferred, an interrupt request signal is output. The types of block and length interrupts are managed separately.

Figure 3-3. Memory-to-Memory Transfer (Example of One-Dimensional Transfer)



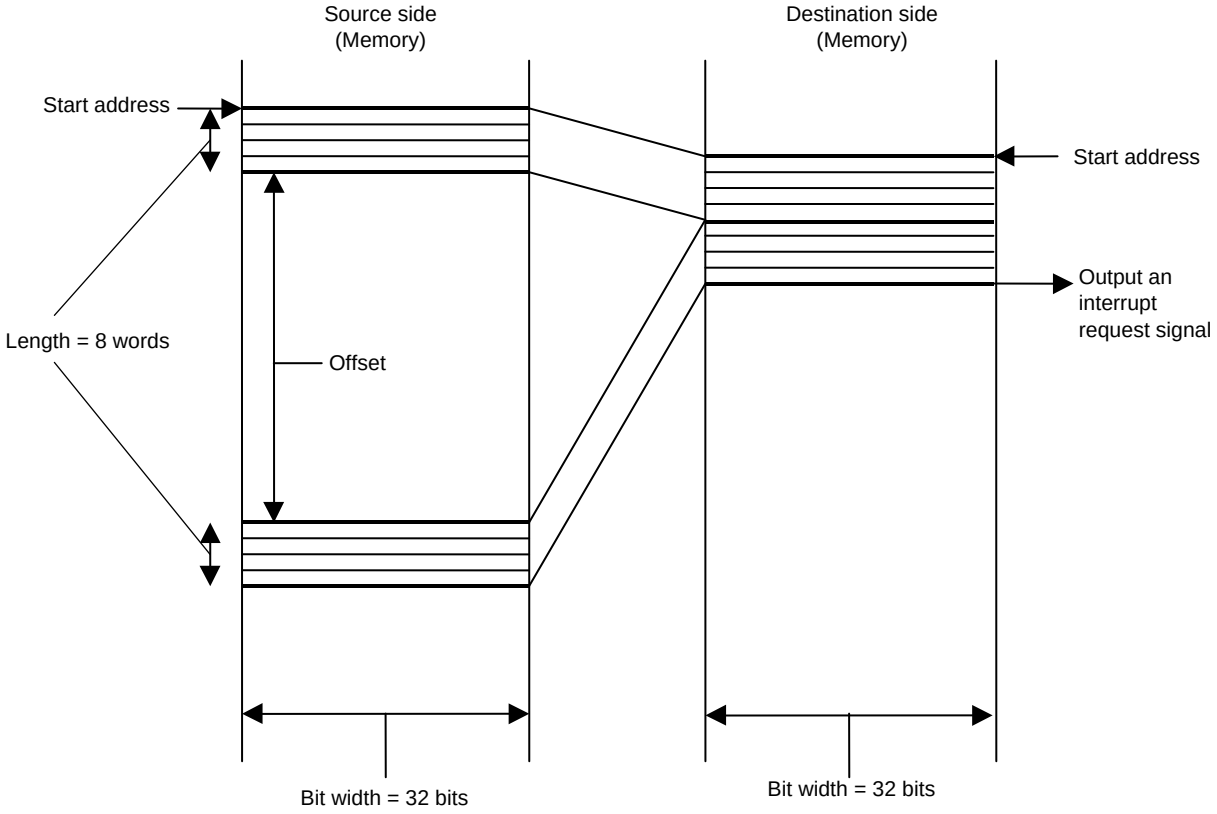
Remark To prevent a block interrupt from occurring for each block size, set the block size to the same value as the length. In this case, a length interrupt and a block interrupt occur simultaneously when DMA transfer ends.

(b) Memory-to-memory transfer (two-dimensional transfer)

Figure 3-4 shows an example of two-dimensional memory-to-memory transfer.

On the source side, the start address is incremented by the block size. After the address is incremented by the block size, the offset is added to the incremented address value and access is made to another block of data. On the destination side, addresses are generated in an incremental manner. Upon completion of the transfer of the total transfer amount, an interrupt request signal is output. While the offset function is not used on the destination side in the example shown in Figure 3-4, it is also possible to accomplish the transfer with the block size or offset specified.

Figure 3-4. Memory-to-Memory Transfer (Example of Two-Dimensional Transfer)



(c) Memory to Memory transfer (repeat transfer)

Figure 3-5 shows an example of memory-to-memory transfer with which only the destination side repeats transfer.

On the source side, data is transferred in an incremental manner beginning with the start address. Upon completion of the transfer of the total transfer amount, a length interrupt is issued (a block interrupt can be issued as well).

On the destination side, when data of the block size counted from the start address has been transferred, a block interrupt is issued and the start address is initialized. (If a block count is set in the block size count register, the start address is initialized as soon as the specified count of blocks is transferred.)

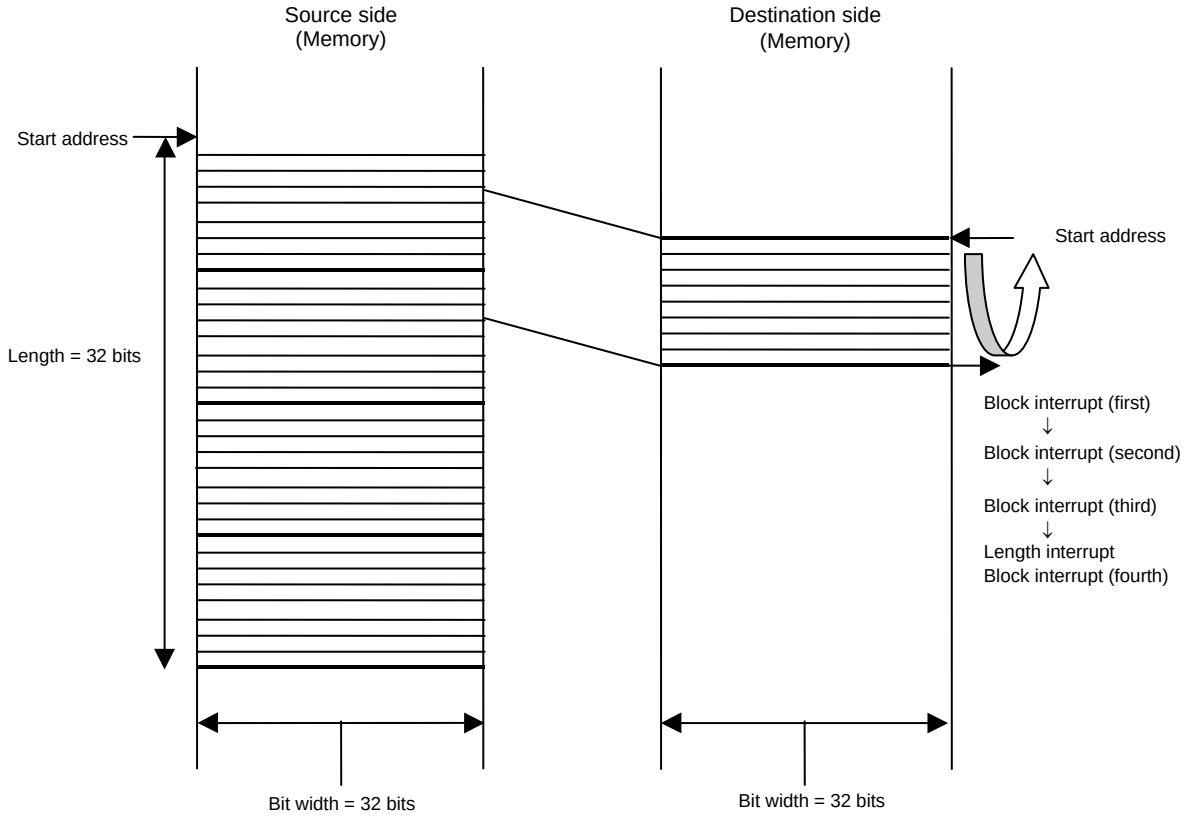
Upon completion of the transfer of the total transfer amount, an interrupt request signal is output. To perform repeat transfer, the offset must be set to 0 (one-dimensional transfer).

While the source side does not operate in repeat transfer mode in the example shown in Figure 3-5, it is also possible to set the repeat mode for the source side, as for the destination side.

If “0” is set as the length when the repeat transfer mode is specified, the length of data to be transferred is infinite.

Parameters for repeat transfer can be set only in word units.

Figure 3-5. Memory-to-Memory Transfer (Example of Repeat Transfer)



(d) Memory-to-memory transfer (reverse transfer)

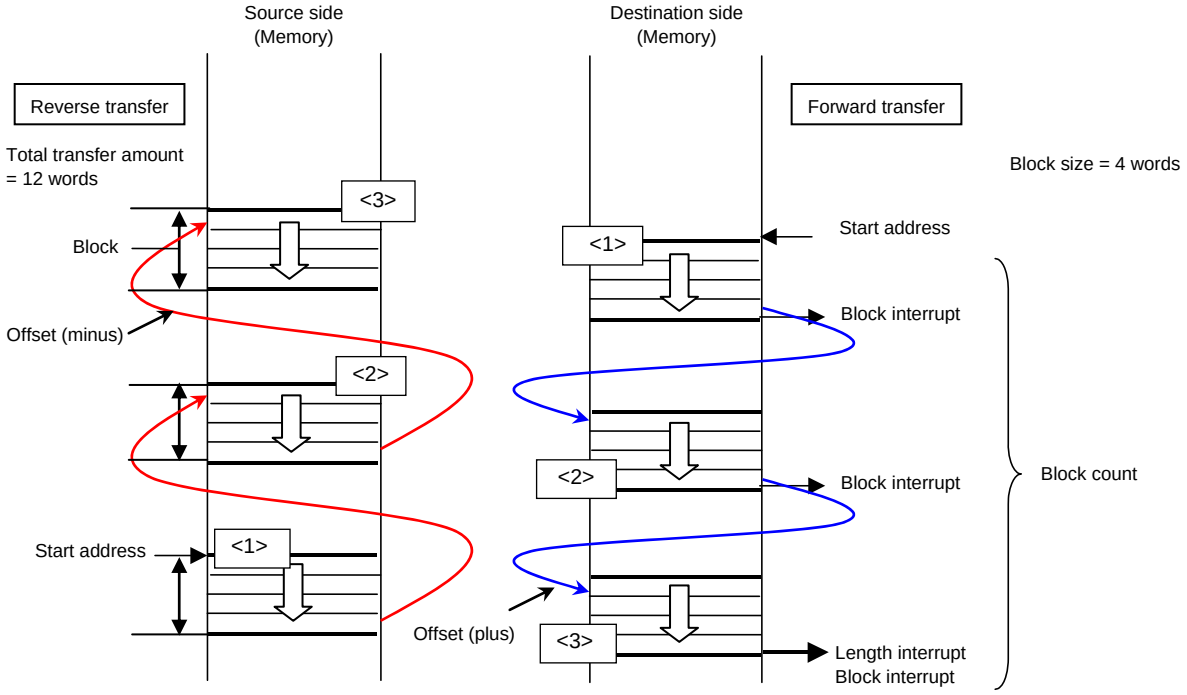
Memory-to-memory transfer supports reverse transfer in block units, separately for the source and destination sides. (Reverse transfer is implemented by using an offset setting toward lower addresses.)

Figure 3-6 shows an example of reverse transfer with which the source side performs reverse transfer and the destination side performs forward transfer.

On the source side, the start address is incremented by the block size. After the address is incremented by the block size, the offset is subtracted from the address value and then the specified number of blocks are transferred again. On the destination side, the offset is added to the address.

The figure below shows an example of reverse transfer with which the destination side performs forward transfer. Reverse transfer with which the destination side performs reverse transfer or both sides perform reverse transfer are also available.

Figure 3-6. Memory-to-Memory Transfer (Example of Reverse Transfer)



(4) Data control

(a) Read control block

Between the read control block and the write control block is a built-in four-entry FIFO buffer holding up to 256 bytes of data per entry.

Even if valid data is not specified to be a word length, the read control block reads an entire word of data and stores the valid data in the FIFO buffer along with the null data. To inform the write control block about the valid data bytes written to the FIFO buffer, the read control block outputs the addition value of the FIFO read pointer to the write control block.

Table 3-5. Transfer Type Selection and FIFO Read Pointer Addition Values

Transfer Start Address		Transfer Type	FIFO Read Pointer Addition Value
64-byte boundary		INCR16	0
32-byte boundary		INCR8	0
Other	Word boundary	INCR8	0
	SA[1:0] = 3H	INCR8	+3
	SA[1:0] = 2H	INCR8	+2
	SA[1:0] = 1H	INCR8	+1

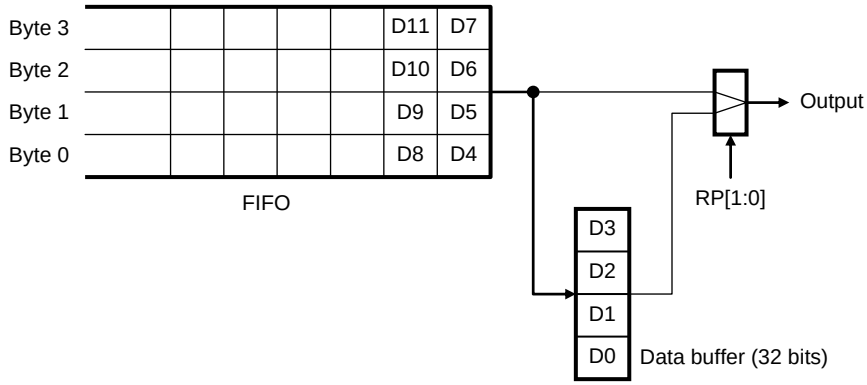
Remark SA: Source address

In addition, upon completion of the transfer of data of the length specified in the length register, the read control block outputs a transfer completion signal to the write control block. In response to this signal, the write control block writes all the data remaining in the FIFO buffer.

(b) Write control block

The write control block reads necessary data from the FIFO buffer and writes it to the destination specified in the parameter register. It starts to read data from the location indicated by the read pointer of the logical channel entry that is selected through logical channel arbitration. To allow data to be transferred in byte units, data alignment is required.

Endian conversion is provided for both read and write control blocks.



WP[1:0]	RP[1:0]	Output [31:24]	Output [23:16]	Output [15:8]	Output [7:0]	Transfer Type
00	00	D3	D2	D1	D0	Word
00	01	D4	D3	D2	D1	Word
00	10	D5	D4	D3	D2	Word
00	11	D6	D5	D4	D3	Word
01	00	–	–	D0	–	Byte
		D2	D1	–	–	Halfword
01	01	–	–	D1	–	Byte
		D3	D2	–	–	Halfword
01	10	–	–	D2	–	Byte
		D4	D3	–	–	Halfword
01	11	–	–	D3	–	Byte
		D5	D4	–	–	Halfword
10	00	D1	D0	–	–	Halfword
10	01	D2	D1	–	–	Halfword
10	10	D3	D2	–	–	Halfword
10	11	D4	D3	–	–	Halfword
11	00	D0	–	–	–	Byte
11	01	D1	–	–	–	Byte
11	10	D2	–	–	–	Byte
11	11	D3	–	–	–	Byte

Remark WP: Write pointer, RP: FIFO read pointer

3.2.2 Memory-to-peripheral transfer (PCH2)

Memory-to-peripheral transfer sends data from a source address to a destination address, in response to request signals sent from each module, in addition to transfer according to the ACPU register settings.

The following table lists blocks subject to memory-to-peripheral transfer.

Table 3-6. Memory-to-Peripheral Transfer Combinations

LCH No.	Memory-to-Peripheral Transfer	AB0 Area	MEMC Area
0	UART0	○	○
1	UART1	○	○
2	UART2	○	○
3	SDIA	○	○
4	SDIB	○	○
5	SDIC	○	○
6	Reserved (unused)	–	–
7	Reserved (unused)	–	–
8	Reserved (unused)	–	–
9	PCM0 (audio serial)	○	○
10	PCM1 (audio serial)	○	○
11	Reserved (unused)	–	–
12	SPI0	○	○
13	SPI1	○	○
14	SPI2/MSP (GD)	○	○

Physical channel 2 (PCH2) is a channel dedicated to memory-to-peripheral transfer. PCH2 has 15 logical channels (LCH0 to LCH14). These logical channels are arbitrated on a burst transfer size basis in a round-robin fashion. LCH6 to LCH8 and LCH11 are the reserved channels and therefore cannot be used.

(1) LCH arbitration control

(a) Read control block

The same processing as for PCH0 is performed.

(b) Write control block

Round-robin arbitration is performed among those logical channels for which starting of DMA transfer is directed in the DMA start control register and for which the transfer request signal from the relevant peripheral is active, to select a logical channel subject to transfer. Note that a logical channel can participate in arbitration only if the FIFO buffer assigned to that channel has 4 bytes equal to or more than the peripheral transfer size.

(2) AHB access control

(a) Read control block

The same processing as for PCH0 is performed. Note that only INCR8 is used as the transfer burst size.

(b) Write control block

AHB access by the write control block is performed using only single transfer. The transfer bit width (8 bits, 16 bits, or 32 bits) can be selected according to the specifications of the peripheral unit concerned. Specify the transfer bit width for each logical channel using the mode register, according to the transfer bit width supported by each peripheral unit.

Table 3-7. Memory-to-Peripheral Transfer Combinations and Transfer Bit Width

LCH No.	Peripheral	Transfer Bit Width Supported
0	UART0	The DMA controller supports 8, 16, and 32 bits. Specify the relevant width according to the specification of the peripheral.
1	UART1	
2	UART2	
3	SDIA	
4	SDIB	
5	SDIC	
6	Reserved (unused)	
7	Reserved (unused)	
8	Reserved (unused)	
9	PCM0 (audio serial)	
10	PCM1 (audio serial)	
11	Reserved (unused)	
12	SPI0	
13	SPI1	
14	SPI2/MSP (GD)	

(3) Address control

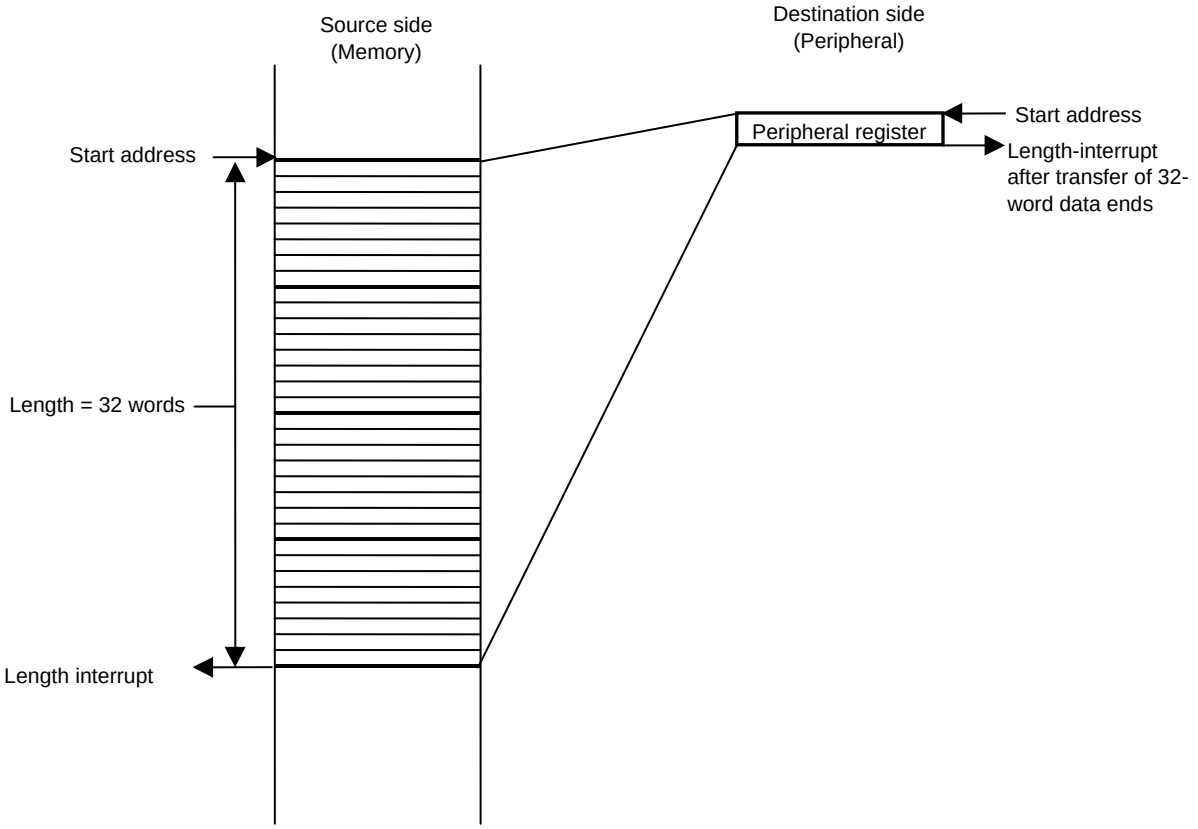
(a) Read control block

The same processing as for PCH0 is performed.

(b) Write control block

On the peripheral side, the value set in a start address register is not updated; i.e., the address is fixed. On the memory side, the value set in a start address register is incremented. Upon completion of transfer of data of the specified length, an interrupt request signal is issued. It is also possible to set a block size and output an interrupt on a per-block size basis, as shown in the examples of the memory-to-memory transfer. Figure 3-7 shows an example of memory-to-peripheral transfer.

Figure 3-7. Example of Memory-to-Peripheral Transfer



(4) Data control

(a) Read control block

Between the read control block and the write control block is a built-in 12-entry FIFO buffer holding up to 128 bytes of data per entry.

The basic control processing is the same as that for PCH0.

(b) Write control block

The write control block reads necessary data from the FIFO buffer and writes it to the destination specified in the parameter register. FIFO read pointer control changes depending on the transfer bus width on the peripheral side.

Table 3-8. Data Alignment for PCH2 Write Control Block

Peripheral Transfer Bus Width	RP	Byte Lane Selected	RP Addition Value
8 bits	00	n	+1
	01	n + 1	
	10	n + 2	
	11	n + 3	
16 bits	00	n	+2
	01	n + 1	
	10	n + 2	
	11	n + 3	
32 bits	00	n	+4
	01	n + 1	
	10	n + 2	
	11	n + 3	

(5) Timeout function

See **3.2.3 (5) Timeout function**.

3.2.3 Peripheral-to-memory transfer (PCH3)

Peripheral-to-memory transfer sends data from a source address to a destination address, in response to request signals sent from each module, in addition to transfer according to the ACPU register settings. The following table lists blocks subject to peripheral-to-memory transfer.

Table 3-9. Peripheral-to-Memory Transfer Combinations

LCH No.	Peripheral-to-Memory Transfer	AB0 Area	MEMC Area
0	UART0	○	○
1	UART1	○	○
2	UART2	○	○
3	SDIA	○	○
4	SDIB	○	○
5	SDIC	○	○
6	Reserved (unused)	–	–
7	Reserved (unused)	–	–
8	Reserved (unused)	–	–
9	PCM0 (audio serial)	○	○
10	PCM1 (audio serial)	○	○
11	Reserved (unused)	–	–
12	SPI0	○	○
13	SPI1	○	○
14	SPI2/MSP (GD)	○	○

Physical channel 3 (PCH3) is a channel dedicated to peripheral-to-memory transfer. PCH3 has 11 logical channels . These logical channels are arbitrated on a single transfer size basis in a round-robin fashion.

(1) LCH arbitration control

(a) Read processing

Round-robin arbitration is performed among those logical channels for which starting of DMA transfer is directed in the DMA start control register and for which the transfer request signal from the relevant peripheral is active, to select a logical channel subject to transfer. Note that a logical channel can participate in arbitration only if the 16-entry entry buffer has one or more free areas.

(b) Write processing

No arbitration is performed, but entries are processed in the order they are registered in the entry buffer.

(2) AHB access control

(a) Read processing

AHB access is performed using single transfer. The transfer bit width (8 bits, 16 bits, or 32 bits) can be selected according to the specifications of the peripheral unit concerned. The transfer bit width can be specified using the mode register.

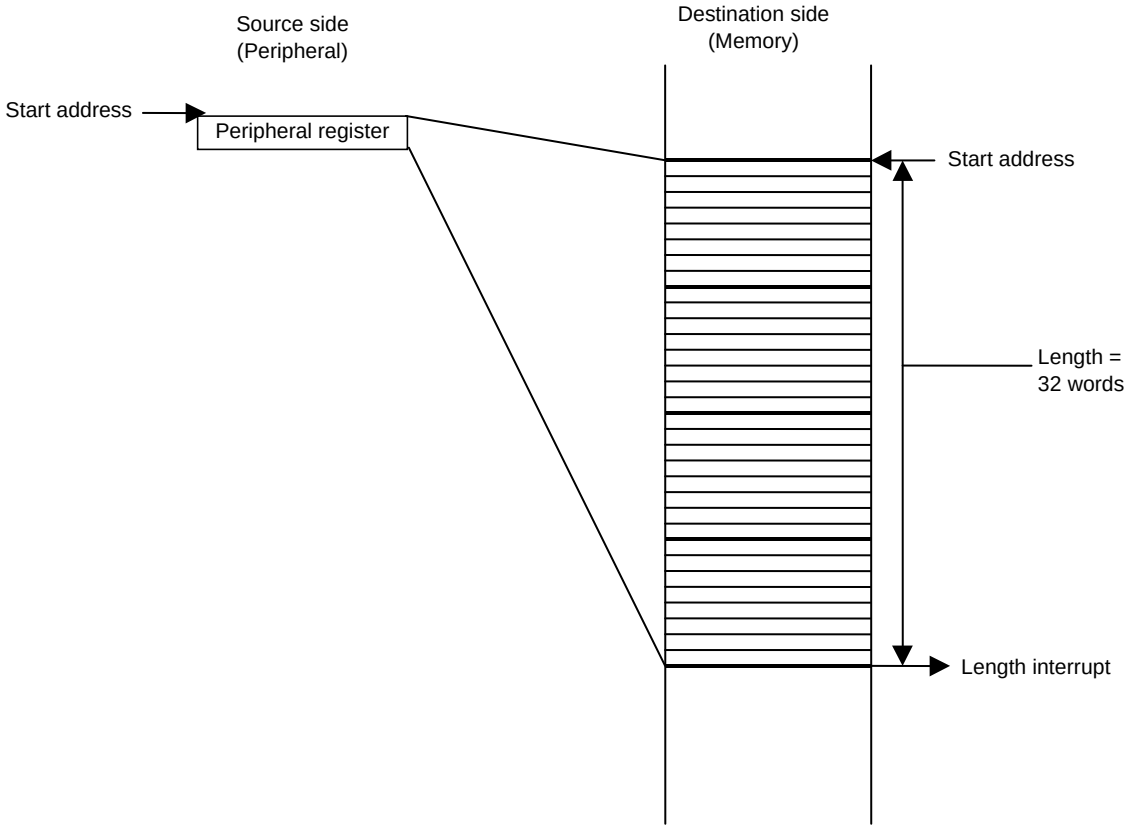
(b) Write processing

AHB access is performed using single transfer. The transfer bit width applied when writing data to memory can be changed according to the entry in the entry buffer.

(3) Address control

On the peripheral side, the value set in a start address register is not updated; i.e., the address is fixed. On the memory side, the value set in the start address register is incremented. Upon completion of transfer of data of the specified length, an interrupt request signal is issued. It is also possible to set a block size and output an interrupt on a per-block size basis, as shown in the examples of the memory-to-memory transfer. Figure 3-8 shows an example of peripheral-to-memory transfer.

Figure 3-8. Example of Peripheral-to-Memory Transfer



(4) Data control

(a) Read control block

Between the read control block and the write control block is a built-in 16-entry entry buffer holding up to 4 bytes of data per entry.

The read control block writes the data read through a single transfer to the entry buffer by consuming an entry per transaction. At the same time, it saves the entry about the written data to the entry buffer. The items to be stored in the entry information register are the logical channel number and the number of valid bytes.

(b) Write control block

The write control block retrieves the transferred data in the order of entry and passes the LCH number and the number of valid bytes, stored in the entry information register, to the AHB access control block.

(5) Timeout function

A timeout function is provided for transfers between memory and UART interface, which is used when no DMA transfer request is sent from the peripheral interface for a specific period. To enable this function, set the mode register to use the timer and specify the timeout time in the timer register. This timeout function is intended exclusively for UART0 to UART2.

The timer starts counting when the first DMA transfer request (DMARQ) is received after DMA startup.

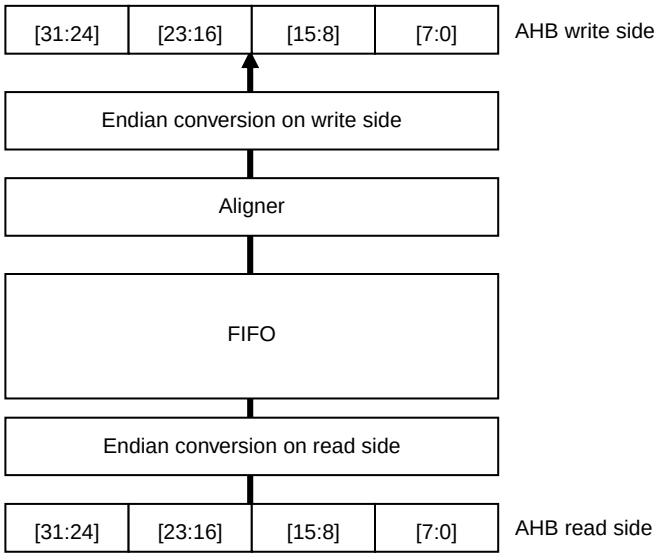
When DMARQ is received again, the counter is set to the timer register value and starts counting down.

3.3 Endian Conversion Functions

The DMAC has a byte endian conversion function for the read and write control blocks.

Parameters for using endian processing must be set in word units. If endian conversion is performed with parameters which do not satisfy this condition, the first 4 bytes and the last 4 bytes of each transfer block may be garbled. Transfer under conditions described in **3.3.3 Setting exception for endian conversion**, however, is available as an exception.

Figure 3-9. Timing for Performing Endian Processing

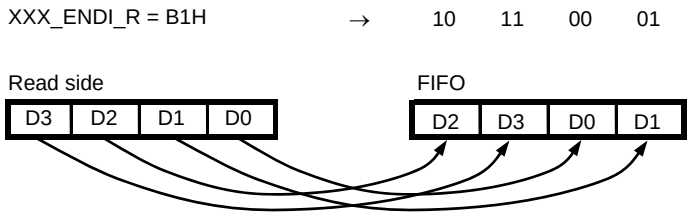


3.3.1 Endian conversion functions on read control block

Byte lane of data to be captured into a data buffer (FIFO) can be selected for each byte.

- Data read from byte 0 → Selectable from byte 0, 1, 2 or 3 of AHB read data
- Data read from byte 1 → Selectable from byte 0, 1, 2 or 3 of AHB read data
- Data read from byte 2 → Selectable from byte 0, 1, 2 or 3 of AHB read data
- Data read from byte 3 → Selectable from byte 0, 1, 2 or 3 of AHB read data

Figure 3-10. Example of Basic Endian Conversion in Read Control Block

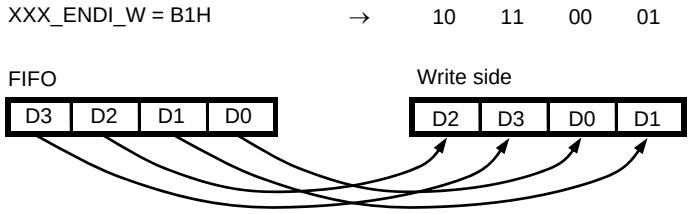


3.3.2 Endian conversion functions on write control block

Byte lane for peripherals to be written can be selected for each byte.

- Data written to byte 0 → Selectable from byte 0, 1, 2 or 3 of write data
- Data written to byte 1 → Selectable from byte 0, 1, 2 or 3 of write data
- Data written to byte 2 → Selectable from byte 0, 1, 2 or 3 of write data
- Data written to byte 3 → Selectable from byte 0, 1, 2 or 3 of write data

Figure 3-11. Example of Basic Endian Conversion in Write Control Block



3.3.3 Setting exception for endian conversion

Parameters for endian conversion must basically be set in word units. However, setting in other units is available if any of the following conditions is satisfied.

The table below shows whether endian conversion is enabled for memory-to-memory transfer (PCH0) if the data length, block size and offset are set in word units.

Transfer Address Boundary		Endian Conversion	
SourceAddress[1:0]	DestinationAddress[1:0]	Read Side	Write Side
Word Lower address = 00	Word	○	○
	Halfword	○	△
	Byte	○	×
Halfword Lower address = 10	Word	△	○
	Halfword	△	△
	Byte	△	×
Byte Lower address = 01 10	Word	×	○
	Halfword	×	△
	Byte	×	×

Remark ○: Available
△: Available only for conversion in halfword units. Example: D3D2D1D0 will be D2D3D0D1.
×: Unavailable

3.4 DMA Transfer Start Sources

The following two types of sources trigger DMA transfer.

3.4.1 Software request (PCH0)

DMA transfer starts when the DMA start control register of the DMA controller is set to 1.

3.4.2 Request from DMAC external pins (PCH2, PCH3)

DMA transfer starts when a DMA request is issued from a peripheral while start of DMA transfer is directed in the DMA start control register controlled via software.

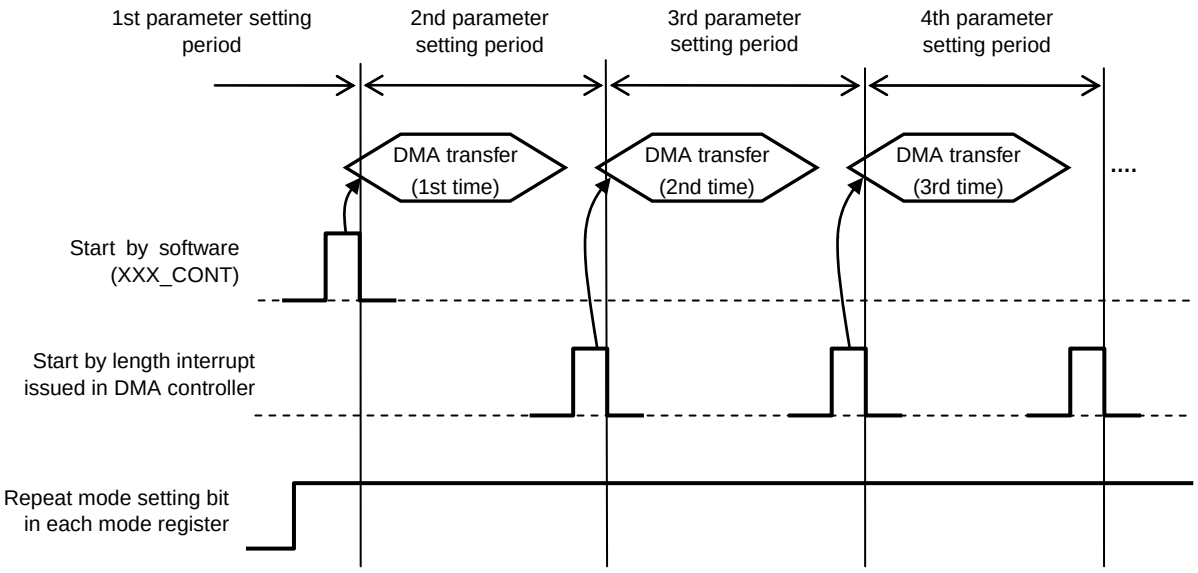
3.4.3 Continuous transfer

Parameter setting registers have a reservation function, so the parameters for the subsequent transfer can be set while DMA on a channel has been started. The transfer reservation must be set in a period from when DMA starts until the next DMA starts. In addition, the repeat mode setting bits corresponding to the transfer channel in each mode register must be set to 1.

A procedure for continuous transfer is shown below.

<1> Sets transfer parameters (1st time).
<2> Starts DMA.
<3> Sets transfer parameters (2nd time).
<4> Waits for a length interrupt to occur. → A length interrupt occurs (1st time).
<5> Sets transfer parameters (3rd time).
<6> Waits for a length interrupt to occur. → A length interrupt occurs (2nd time).
<7> Sets transfer parameters (4th time).
<8> Waits for a length interrupt to occur. → A length interrupt occurs (3rd time).
: Repeat

Figure 3-12. Continuous Transfer



3.5 Forced End

The following three types of sources force DMA transfer to end.

(1) Forced end due to an error response

See **3.6 Response**.

(2) Abortion by DMA end control register

Ongoing DMA transfer can be aborted forcibly by setting the DMA end control register during DMA transfer. After the forced abortion, the internal state is initialized.

Caution During transfer between memory and peripheral, initialize the internal state on the peripheral side as well, after the transfer is forced to end.

(3) Forced end due to timeout (for UART only)

See **3.2.3 (5) Timeout function**.

3.6 Responses

When operating as the AHB master, the DMA controller behaves according to an error response (HRESP[1:0]) as shown below.

Table 3-10. DMA Operation in Response to HRESP

HRESP	OKAY	ERROR	RETRY	SPLIT
DMA operation	Normal operation	Ends the transfer and generates an interrupt.	Ends the transfer and generates an interrupt.	Ends the transfer and generates an interrupt.

An error response is returned if the DMA controller attempts to access an address to which no device is assigned, or accesses the ADSP with power turned off. In this case, a correct result is not obtained even if the operation continues, so the DMA controller ends the transfer and generates an interrupt. The interrupt source can be identified as a slave response error.

The slave side does not return RETRY or SPLIT. If either of these responses is returned, there may be a problem, so the DMA controller ends the transfer and generates an interrupt. The interrupt source can be identified as a slave response error.

3.7 Interrupts

The following four types of sources cause interrupt signals to be output.

- End due to a timeout
  An interrupt signal is output when no DMA requests are input from peripherals for the time set to the timer.
- End due to an error
  An interrupt signal is output when DMA does not end normally (when an AHB error response is returned).
- End of block transfer
  PCH0 and PCH3 generate this interrupt each time block transfer is completed on the destination (write) side.
  PCH2 generates this interrupt each time block transfer is completed on the source (read) side.
- End of length transfer
  This interrupt source indicates the end of an ordinary DMA transfer. It occurs each time transfer of data of the specified length is completed on the destination (write) side.

One interrupt signal is output per processor (ACPU/ADSP).

An interrupt output destination can be specified on a per-logical channel basis by using an interrupt output destination setting register.

For a timing of transfer end due to a timeout, see **3.2.3 (5) Timeout function**.

The relationships between interrupt signals and interrupt sources are shown below.

	Timeout		Error		Block		Length	
	Read Side	Write Side	Read Side	Write Side	Read Side	Write Side	Read Side	Write Side
PCH0	–	–	○	○	×	○	–	○
PCH2	–	○	○	○	○	–	–	○
PCH3	○	–	○	○	–	○	–	○

Remark ○: If the interrupt caused by this source occurs, the corresponding interrupt pin changes to high level.
×: The interrupt caused by this source is not reflected on the corresponding interrupt pin.
–: Not applicable (no interrupt source)

3.8 Internal Clock Control

The DMA controller controls the AHB clocks on a per-physical-channel basis.

Clocks are input to the DMA block by outputting a clock request signal (DMA_PCHnCLKREQ: n = 0, 2, 3) to the ASMU.

- PCH0

  The signal for requesting a clock for PCH0 is obtained by ORing the DMA status on each logical channel. (The clock supply starts when any of the logical channels is enabled by the DMA control register.)

- PCH2

  The signal for requesting a clock for PCH2 is obtained by ORing the signal on the read side (memory) when at least one status of the FIFO write enable signal on an active logical channel becomes true and the signal on the write side (peripheral) obtained by extending all the DMARQ signals for 5 clock cycles.

  The ORed DMARQ signal (PCH2_TXDMARQ) is supplied to the ASMU, and the ASMU starts supplying DMA_PCH2_CLK when this signal is set to 1.

- PCH3

  The signal for requesting a clock for PCH3 is obtained by ORing the signal obtained by ORing all the DMARQ signals and extending the ORed signal for 5 clock cycles, in a state in which the FIFO is not empty, with the transaction busy signals on the read and write sides.

CHAPTER 4 USAGE

4.1 Cautions on Use

4.1.1 Restrictions on parameter settings

The restrictions shown below apply to the parameter settings for the DMA controller.

DMA operation is not guaranteed if these restrictions are not observed.

- Repeat transfer must be enabled to perform infinite-length transfer. The offset must be set to 0.
- The offset for repeat transfer must be set to 0 (one-dimensional transfer).
- Parameters for endian conversion must be set in word units (see the exception described in **3.3.3 Setting exception for endian conversion**).
- PCH1 is reserved.

(1) PCH0

	Register	Minimum Settable Unit
Source side	Address	Byte
	Offset	Byte
Destination side	Address	Byte
	Offset	Byte
Common	Block size	Byte
	Length	Byte

(2) PCH2

	Register	Minimum Settable Unit
Source side	Address	Byte
	Offset	Byte
	Block size	Byte
Destination side	Address	Byte
Common	Length	Byte

(3) PCH3

	Register	Minimum Settable Unit
Source side	Address	Byte
Destination side	Address	Byte
	Offset	Byte
	Block size	Byte
Common	Length	Byte

Remarks 1. The minimum settable unit is “word” if “word” is specified as the transfer bit width by using a mode register.

2. The minimum settable unit is halfword if halfword is specified as the transfer bit width by using a mode register.

Revision History

Date	Revision	Comments
February 10, 2009	1.0	–
April 27, 2009	2.0	• Incremental update from comments to the 1.0. • LCH7 (MSP) and LCH11 (MMM) are changed to Reserved.
June 30, 2009	3.0	• Incremental update from comments to the 2.0.

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