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User's Manual

Multimedia Processor for Mobile Applications

I²C Interface

EMMA Mobile™1

[MEMO]

--- **NOTES FOR CMOS DEVICES** ---

① **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② **HANDLING OF UNUSED INPUT PINS**

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ **PRECAUTION AGAINST ESD**

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ **STATUS BEFORE INITIALIZATION**

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ **POWER ON/OFF SEQUENCE**

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ **INPUT OF SIGNAL DURING POWER OFF STATE**

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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PREFACE

Readers   This manual is intended for hardware/software application system designers who wish to understand and use the I^2C interface functions of EMMA Mobile1 (EM1), a multimedia processor for mobile applications.

Purpose   This manual is intended to explain to users the hardware and software functions of the I^2C interface of EM1, and be used as a reference material for developing hardware and software for systems that use EM1.

Organization   This manual consists of the following chapters.
- Chapter 1   Overview
- Chapter 2   Pin functions
- Chapter 3   Registers
- Chapter 4   Description of functions

How to Read This Manual   It is assumed that the readers of this manual have general knowledge of electricity, logic circuits, and microcontrollers.

To understand the functions of the I^2C interface of EM1 in detail
→   Read this manual according to the **CONTENTS**.

To understand the other functions of EM1
→   Refer to the user's manual of the respective module.

To understand the electrical specifications of EM1
→   Refer to the Data Sheet.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH
Data type:	Word … 32 bits
	Halfword … 16 bits
	Byte … 8 bits

Related Documents The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name		Document No.
MC-10118A Data sheet		S19657E
μ PD77630A Data sheet		S19686E
User's manual	Audio/Voice and PWM Interfaces	S19253E
	DDR SDRAM Interface	S19254E
	DMA Controller	S19255E
	I^{2}C Interface	This manual
	ITU-R BT.656 Interface	S19257E
	LCD Controller	S19258E
	MICROWIRE	S19259E
	NAND Flash Interface	S19260E
	SPI	S19261E
	UART Interface	S19262E
	Image Composer	S19263E
	Image Processor Unit	S19264E
	System Control/General-Purpose I/O Interface	S19265E
	Timer	S19266E
	Terrestrial Digital TV Interface	S19267E
	Camera Interface	S19285E
	USB Interface	S19359E
	SD Memory Card Interface	S19361E
	PDMA	S19373E
	One Chip (MC-10118A)	S19598E
	One Chip (μ PD77630A)	S19687E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

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CHAPTER 1 OVERVIEW

The I^{2}C interface is used for master and slave operations on the I^{2}C bus.

1.1 Features

The main features of the I^{2}C interface are as follows.

○ Two channels: IIC and IIC2

○ Conformance to the I^{2}C bus format (1995 updated version of Philips specification)
Data length: 8 bits (Eight-bit data is followed by one ACK signal bit.) The standard mode (transfer rate: 70 kbps maximum) and high-speed mode (transfer rate: 341 kbps maximum) are supported.

○ Automatic serial data identification
A start condition, slave address, data, and stop condition on the serial data bus are automatically detected.

○ Address-based chip selection
In master operation, a slave device on the I^{2}C bus can be selected for communication by transmitting a slave address or extension code.

○ Wake-up operation
In slave operation, an interrupt is generated only when the received address matches the value of the SVA0 register or when an extension code is received. Therefore, devices on the I^{2}C bus other than the selected slave can operate independently of serial communication.

○ Acknowledge (ACK) transmission
In master/slave operation, the ACK signal is sent to confirm that serial communication has been executed normally.

○ Wait (WAIT) notification
A wait signal is sent to report that the device is waiting.

○ Arbitration notification
When more than one master device generated the start condition "at the same time ", the control which does level comparison of a serial data bus (SDA) terminal after zero in of serial clock (SCL) and chooses a master device can be performed.

2.1 I^{2}C Interface Pins

Pin Name	I/O	Function	Alternate Pin Function
IIC_SCL	I/O	Serial clock input	GIO_P83
IIC_SDA	I/O	Serial data input	GIO_P84
IIC2_SCL	I/O	Serial clock input	NAND_WE
IIC2_SDA	I/O	Serial data input	NAND_RB0

CHAPTER 3 REGISTERS

3.1 Registers

The I^{2}C interface registers allow halfword access only.

Do not access reserved registers.

Do not write any value other than 0 to reserved bits in each register.

Base address: 5004_0000H (IIC)

Address	Register Name	Symbol	R/W	After Reset
0000H	IIC0 shift register	IIC_IIC0	R/W	0000H
0004H	Reserved	–	–	–
0008H	IIC0 control register	IIC_IICC0	R/W	0000H
000CH	Slave address register	IIC_SVA0	R/W	0000H
0010H	IIC0 clock selection register	IIC_IICCL0	R/W	0000H
0014H-0018H	Reserved	–	–	–
001CH	IIC0 state register (Read-only register for emulation)	IIC_IICSE0	R	0000H
0020H-0024H	Reserved	–	–	–
0028H	IIC0 flag register	IIC_IICF0	R/W	0000H

Base address: 5003_0000H (IIC2)

Address	Register Name	Symbol	R/W	After Reset
0000H	IIC0 shift register	IIC2_IIC0	R/W	0000H
0004H	Reserved	–	–	–
0008H	IIC0 control register	IIC2_IICC0	R/W	0000H
000CH	Slave address register	IIC2_SVA0	R/W	0000H
0010H	IIC0 clock selection register	IIC2_IICCL0	R/W	0000H
0014H-0018H	Reserved	–	–	–
001CH	IIC0 state register (Read-only register for emulation)	IIC2_IICSE0	R	0000H
0020H-0024H	Reserved	–	–	–
0028H	IIC0 flag register	IIC2_IICF0	R/W	0000H

3.2 Register Functions

3.2.1 IIC0 shift register

This register (IIC_IIC0: 5004_0000H (IIC), 5003_0000H (IIC2)) is used to perform serial transmission/reception (shift operation) in synchronization with the serial clock. Data is transferred, starting with the most significant bit (MSB).

Operation is not guaranteed if this register is accessed during data transfer.

If this register is written to during a wait period, the wait state is canceled and data transfer starts.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Transmit/receive data							
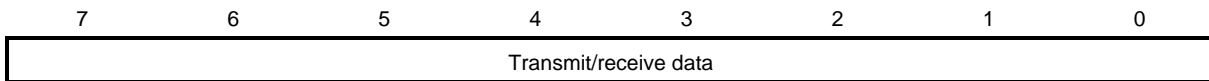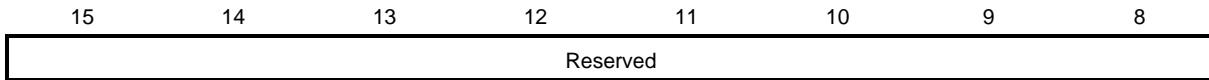
Name	R/W	Bit	After Reset	Function
Reserved	R	15:8	00H	Reserved.
Transmit/receive data	R/W	7:0	00H	Transmit/receive data is read/written.

3.2.2 IIC0 control register

This register (IIC_IICC0: 5004_0008H (IIC), 5003_0008H (IIC2)) specifies the settings for I^2C interface operations such as enabling/disabling the I^2C interface and specifying the wait timing.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
IICE0	LREL0	WREL0	SPIE0	WTIM0	ACKE0	STT0	SPT0

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R/W	15:8	00H	Reserved.
IICE0	R/W	7	0b	Enables/disables the I^2C interface. 0: Presets the state register and stops internal operations. 1: I2C interface operation is enabled.
LREL0	R/W	6	0b	Ends the communication state and sets the wait state. This bit is used, for example, when an extension code irrelevant to this device is received. When this bit is set to 1, the SCL/SDA line is placed in the Hi-Z state, and the STT0 and SPT0 bits of this register and the MSTS0, EXC0, COI0, TRC0, ACKD0, and STD0 bits of the IIC_IICSE0 register are cleared. After this bit is set to 1, it is automatically reset to 0 (one-shot operation). When this bit is read, 0 is returned. 0: Normal operation 1: When communication ends, the operation enters the wait state.
WREL0	R/W	5	0b	Cancels the wait state. After this bit is set to 1, it is automatically reset to 0 (one-shot operation). If the wait state is canceled by setting the WREL0 bit when the wait period is set to 9th clocks and when the TRC0 bit of the IIC_IICSE0 register is set to 1, the TRC0 bit is cleared to release the SDA line (Hi-Z). When this bit is read, 0 is returned. 0: The wait state is preserved. 1: The wait state is canceled.
SPIE0	R/W	4	0b	Enables/disables a stop condition interrupt. 0: Disables issuance of stop condition interrupt requests. 1: Enables issuance of stop condition interrupt requests.

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Name	R/W	Bit	After Reset	Function
WTIM0[Note 1]	R/W	3	0b	Specifies the timing of interrupt request generation. In master operation, the clock output is pulled low to wait after the specified number of clock cycles are output. In slave operation, the clock output is pulled low to make the master wait when the specified number of clock cycles are input. 0: Interrupt is generated at the 8th falling edge of the clock. 1: Interrupt is generated at the 9th falling edge of the clock.
ACKE0 [Note 2]	R/W	2	0b	Controls the acknowledge signal (ACK). "1" is set in this bit because it's receive-enable state when the TRC bit of the IIC register is "0". When not needing the next data, "0" is set in this bit. 0: Disables ACK. 1: Enables ACK. (Sets the SDA line to low during the 9th clock cycle.)
STT0[Note 3]	R/W	1	0b	Issues a start condition. The operation differs depending on what the state was before this bit was set. When this bit is read, 0 is returned. 0: No operation is performed. 1: A start condition is issued. **Remark** This bit is automatically cleared when any of the following conditions occurs: • When a start condition is detected by the master • When a master loses arbitration • When the LREL0 bit is set to 1 • When the IICE0 bit is set to 0 • When a reset is input
SPT0	R/W	0	0b	Issues a stop condition (ends transfer operation as the master). When this bit is set, the SDA line is pulled low, then the SCL line is pulled high or the system waits for the SCL line to be pulled high. Next, a specified time is secured and then the SDA line is pulled high to issue a stop condition. By setting this bit in the wait state, the wait state can be canceled to issue a stop condition. When this bit is read, 0 is returned. 0: No operation is performed. 1: A stop condition is issued. **Remark** This bit is automatically cleared when any of the following conditions occurs: • When a stop condition is detected • When a master loses arbitration • When the LREL0 bit is set to 1 • When the IICE0 bit is set to 0 • When a reset is input

Notes 1. During address transfer, the following operations are performed:
- On the master side, a wait or interrupt request is issued at the 9th falling edge of the clock, regardless of the value of the WTIM0 bit.
- When the address being transferred matches an address input on the slave side (COI0 = 1), a wait or interrupt request is issued at the 9th falling edge of the clock, regardless of the value of the WTIM0 bit.
- When an extension code is received (EXC0 = 1) on the slave side, a wait or interrupt request is issued at the 8th falling edge of the clock, regardless of the value of the WTIM0 bit. If the WTIM0 bit is set to 1, another wait or interrupt request is issued at the 9th falling edge of the clock.

2. Observe the following order when setting the WREL0 and ACKE0 bits.
- Be sure to set the ACKE0 bit and then set the WREL0 bit because the timing at which the setting is applied differs between the WREL0 and ACKE0 bits.

3. When the STT0 bit is set to 1, the following operations are performed according to the state the system was in before the bit was set:
- If the bus is released (communication is stopped), a master device pulls the SDA line low to issue a start condition (to serve as the master). Next, the master secures the specified time and then pulls the SCL line low.
- If there is no participation on the bus and communication reservation is enabled (the IICRSV bit of the IIC_IICF0 register is set to 0 (default)), the start condition can be reserved. After the bus is released, a start condition is automatically issued.
- If there is no participation on the bus and communication cannot be reserved (the IICRSV bit of the IIC_IICF0 register is set to 1), the STCF bit of the IIC_IICF0 register is set to 1. No start condition is issued.
- If the master is in the wait state, the wait state is released and a start condition is issued again.

3.2.3 Slave address register

This register (IIC_SVA0: 5004_000CH (IIC), 5003_000CH (IIC2)) stores the address of a slave device when a device is connected to the serial bus as a slave device.

15	14	13	12	11	10	9	8
Slave address							Reserved

7	6	5	4	3	2	1	0
Reserved							
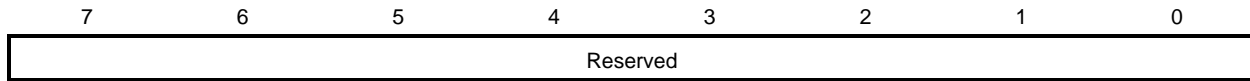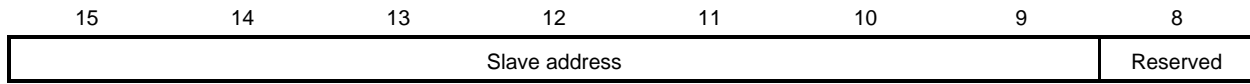
Name	R/W	Bit	After Reset	Function
Slave address	R/W	15:9	00H	Stores a slave address.
Reserved	R	8:0	000H	Reserved.

3.2.4 IIC0 clock selection register

This register (IIC_IICCL0: 5004_0010H (IIC), 5003_0010H (IIC2)) specifies the transfer clock for the I^{2}C interface. Specify the transfer clock by using this register before setting the IICE0 bit of the IIC_IICC0 register.

15	14	13	12	11	10	9	8
			Reserved				

7	6	5	4	3	2	1	0
Reserved		CLD0	DAD0	SMC0	DFC0	CL01	CL00

Name	R/W	Bit	After Reset	Function
Reserved	R	15:6	000H	Reserved.
CLD0[Note 1]	R	5	0b	Detects the level of the SCL line. 0: The level of the SCL line is low. 1: The level of the SCL line is high.
DAD0[Note 1]	R	4	0b	Detects the level of the SDA line. 0: The level of the SDA line is low. 1: The level of the SDA line is high.
SMC0	R/W	3	0b	Specifies the operating mode. 0: Standard mode (Maximum transfer rate: 70 kbps) 1: High-speed mode (Maximum transfer rate: 341 kbps)
DFC0[Note 2]	R/W	2	0b	Enables/disables digital filtering. 0: Digital filtering is disabled. 1: Digital filtering is enabled.
CL01[Note 3]	R/W	1	0b	Selects the transfer clock frequency.
CL00[Note 3]	R/W	0	0b	(see table below)

Selects the transfer clock frequency.

CL01	CL00	Standard mode	High-speed mode
0	0	f$_{XX}$/44	f$_{XX}$/24
0	1	f$_{XX}$/86	f$_{XX}$/24
1	0	f$_{XX}$/86	f$_{XX}$/24
1	1	Setting prohibited	Setting prohibited

Remark f$_{XX}$: Frequency of internal system clock
The internal system clock (IIC_CLK) is output from the system control unit (ASMU).

Notes 1. The CLD0 and DAD0 bits are valid only when the IICE0 bit of the IIC_IICC0 register is set to 1. If the CLD0 and DAD0 bits are read when the IICE0 bit is set to 0, 0 is returned, regardless of the state of the SCL/SDA line.

2. Digital filtering can only be used in the high-speed mode (the SMC0 bit is set to 1).
In either the standard mode or the high-speed mode, the signal is output at the same timing, regardless of the value of the DFC0 bit (used to enable/disable digital filtering).

3. Set the CLO1 and CLO0 bits so that the frequency of the I^{2}C interface internal system clock (IIC_CLK) satisfies the condition indicated below. The same operation is performed, regardless of whether 01b or 10b is set. In the high-speed mode, the same operation is performed when any value other than 11b is set.

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CL01	CL00	Standard Mode	High-Speed Mode
0	0	$2.00 \text{ MHz} \leq f_{XX} \leq 4.19 \text{ MHz}$	$4.19 \text{ MHz} \leq f_{XX} \leq 8.38 \text{ MHz}$
0	1	$4.19 \text{ MHz} \leq f_{XX} \leq 8.38 \text{ MHz}$	$4.19 \text{ MHz} \leq f_{XX} \leq 8.38 \text{ MHz}$
1	0	$4.19 \text{ MHz} \leq f_{XX} \leq 8.38 \text{ MHz}$	$4.19 \text{ MHz} \leq f_{XX} \leq 8.38 \text{ MHz}$
1	1	Setting prohibited	Setting prohibited

3.2.5 IIC0 state register

This read-only register (IIC_IICSE0: 5004_001CH (IIC), 5003_001CH (IIC2)) indicates the state of the I^{2}C interface and is used during emulation. If this register is read, one retry will always occur.

15	14	13	12	11	10	9	8
MSTS0	ALD0	EXC0	COI0	TRC0	ACKD0	STD0	SPD0

7	6	5	4	3	2	1	0
Reserved							

(1/3)

Name	R/W	Bit	After Reset	Function
MSTS0	R	15	0b	Flag for indicating the master communication state. 0: Serving as a slave or communication is enabled 1: Serving as a master [Condition for setting this bit] • When a start condition is issued [Condition for clearing this bit] • When a stop condition is detected • When a master loses arbitration • When the LREL0 bit is set to 1 • When the IICE0 bit is set to 0 • When a reset is input
ALD0	R	14	0b	Flag for indicating arbitration loss. When this bit is set, the MSTS0 bit is cleared. 0: No arbitration has occurred or a master won arbitration 1: A master lost arbitration [Condition for setting this bit] • When a master loses arbitration [Condition for clearing this bit] • When the IICE0 bit is set to 0 • When a reset is input
EXC0	R	13	0b	Flag for indicating whether an extension code has been received. 0: No extension code has been received. 1: An extension code has been received. [Condition for setting this bit] • When the higher 4 bits of the received address data are 0000b or 1111b (at the 8th rising edge of the SCL clock) [Condition for clearing this bit] • When a start condition is detected • When a stop condition is detected • When the LREL0 bit is set to 1 • When the IICE0 bit is set to 0 • When a reset is input

Name	R/W	Bit	After Reset	Function
COI0	R	12	0b	Flag for indicating an address match. 0: No address match was detected. 1: An address match was detected. [Condition for setting this bit] • When the received address data matches the slave address (IIC_SVA0 register) of this device (at the 8th rising edge of the SCL clock) [Condition for clearing this bit] • When a start condition is detected • When a stop condition is detected • When the LREL0 bit is set to 1 • When the IICE0 bit is set to 0 • When a reset is input
TRC0	R	11	0b	Flag for indicating the transmission/reception state. 0: Reception mode (or other than transmission mode) The SDA line is placed in the Hi-Z state. 1: Transmission mode Setting this bit to 1 enables serial data to be output to the SDA line. This setting is valid at the 9th falling edge or later of the SCL clock for the first byte. [Condition for setting this bit] For the master: • When a start condition is issued (STD0 = 1 and MSTS0 = 1) • When 0 is output as the LSB of the first byte of transmit/receive data For the slave: • When 1 is input as the LSB of the first byte of transmit/receive data [Condition for clearing this bit] • When a stop condition is detected • When a master loses arbitration • When the LREL0 bit is set to 1 • When the IICE0 bit is set to 0 • When the WREL0 bit is set to 1 during a wait period. Note • When a reset is input For the master: • When 1 is output as the LSB of the first byte of transmit/receive data For the slave: • When a start condition is detected (STD0 = 1 and MSTS0 = 0) • When 0 is input as the LSB of the first byte of transmit/receive data

Note For the wait period, see **4.1.6 Wait signal (WAIT).**

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Name	R/W	Bit	After Reset	Function
ACKD0	R	10	0b	Flag for indicating whether an ACK signal has been detected. 0: No ACK signal was detected. 1: An ACK signal was detected. [Condition for setting this bit] • When the level of the SDA line is low at the 9th rising edge of the SCL clock [Condition for clearing this bit] • First rising edge of the SCL clock for the next byte • When a stop condition is detected • When the LREL0 bit is set to 1 • When the IICE0 bit is set to 0 • When a reset is input
STD0	R	9	0b	Flag for indicating whether a start condition has been detected. 0: No start condition was detected. 1: A start condition was detected. A setting of 1 indicates that an address is being transferred. [Condition for setting this bit] • When a start condition is detected [Condition for clearing this bit] • First rising edge of the SCL clock for the address transfer byte following the detection of a start condition after this bit is set • When a stop condition is detected • When the IICE0 bit is set to 0 • When a reset is input
SPD0	R	8	0b	Flag for indicating whether a stop condition has been detected. 0: No stop condition was detected. 1: A stop condition was detected. A setting of 1 setting indicates that communication by a master has ended and the bus is released. [Condition for setting this bit] • When a stop condition is detected [Condition for clearing this bit] • First rising edge of the SCL clock for the address transfer byte following the detection of a start condition after this bit is set • When the IICE0 bit is set to 0 • When a reset is input
Reserved	R	7:0	00H	Reserved.

3.2.6 IIC0 flag register

This register (IIC_IICF0: 5004_0028H (IIC), 5003_0028H (IIC2)) controls the I^{2}C interface.

Operation is not guaranteed if this register is written when the IICE0 bit of the IIC_IICC0 register is set to 1.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
STCF	IICBSY	0	0	0	0	STCEN	IICRSV

Name	R/W	Bit	After Reset	Function
Reserved	R	15:8	00H	Reserved.
STCF	R	7	0b	Flag for indicating whether the STT0 bit of the IIC_IICC0 register has cleared. 0: A start condition was issued. 1: The STT0 bit has been cleared. [Condition for setting this bit] • When the STT0 bit is cleared while communication reservation is disabled (IICRSV = 1) [Condition for clearing this bit] • When the STT0 bit is set to 1 • When the IICE0 bit is set to 0 • When a reset is input
IICBSY^{Note1}	R	6	0b	Flag for indicating the I^{2}C bus state. 0: The bus is released. 1: The bus is occupied. [Condition for setting this bit] • When a start condition is detected • When the IICE0 bit is set to 0 while the STCEN bit is set to 0 [Condition for clearing this bit] • When the IICE0 bit is set to 0 • When a reset is input
0	R	5:2	0H	Fix these bits to 0.
STCEN^{Note2}	R/W	1	0b	By setting this bit to 1 after enabling operation (IICE0 = 1), a start condition can be issued without detecting a stop condition. 0: No start condition can be issued without detecting a stop condition. 1: A start condition can be issued without detecting a stop condition. **Remark** This bit is automatically cleared when any of the following conditions occurs: • Start condition detection • Reset input
IICRSV	R/W	0	0b	Enables/disables communication reservation. 0: Enables communication reservation. 1: Disables communication reservation.

Note1 At least 2 clocks of IICBSY is need by the inner internal system clock before the state of the bus is reflected after the I2C is made Enable. It's checked after I wait for 3 clocks by the inner internal system clock because there is a possibility that a difference for 1 clocks occurs by a simultaneous change in the condition.

Note2 When setting the STCEN bit to 1, ensure that other I^2C devices on the I^2C bus are not engaged in communication. If the STCEN bit is set to 1 and the STT0 bit of the IIC_IICC0 register is set to 1 while other I^2C devices are engaged in communication, a start condition is issued and data being sent is lost.

CHAPTER 4 DESCRIPTION OF FUNCTIONS

4.1 I^{2}C Bus Operations

This section describes the serial data communication format of the I^{2}C bus and explains the meanings of the signals used.

Figure 4-1 shows the timing of transferring a start condition, slave address, data, and stop condition output on the SDA line of the I^{2}C bus.

Figure 4-1. Timing of I^{2}C Bus Serial Data Transfer
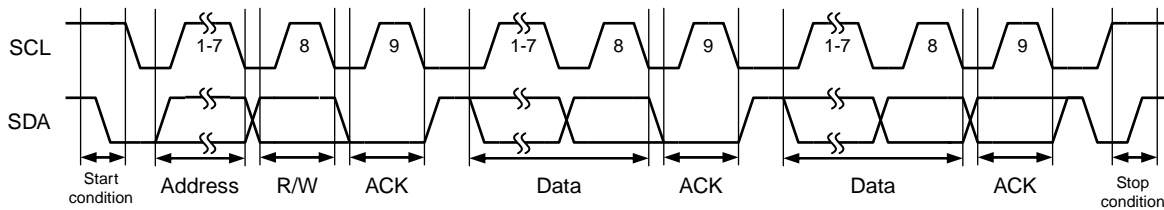
A start condition, slave address, and stop condition are output by the master device.

The acknowledge signal (ACK) can be output by either the master device or slave device. (Usually, the receiver of 8-bit data outputs the ACK signal.)

The serial clock (SCL) is output by the master device.

4.1.1 Start condition

A start condition is issued when the SCL line is high (when the serial clock is not output) and the SDA line is pulled low.

A start condition is a signal output by the master device when it starts a serial transfer to a slave device.

The I^{2}C interface incorporates hardware for detecting a start condition in slave operation.

Figure 4-2. Start Condition
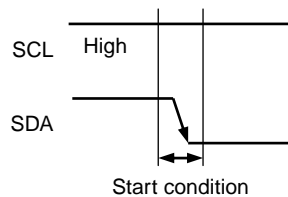
A serial transfer ends with a stop condition. If a start condition is issued again before the stop condition for the current transaction is issued, this start condition is called a restart condition.

4.1.2 Address

The 7-bit data following a start condition is defined as the address.

The address is 7-bit data output by the master device to select a particular slave from multiple slave devices on the bus line. This means that a unique address needs to be assigned to each slave on the bus line.

A slave device detects, by hardware, that data on the SDA line is an address then checks if the 7-bit data matches the value of the slave address register (SVA0). If the 7-bit data matches the value of the SVA0 register, the slave device is selected. The slave device communicates with the master device until the master device transmits a restart condition or a stop condition.

Figure 4-3. Address
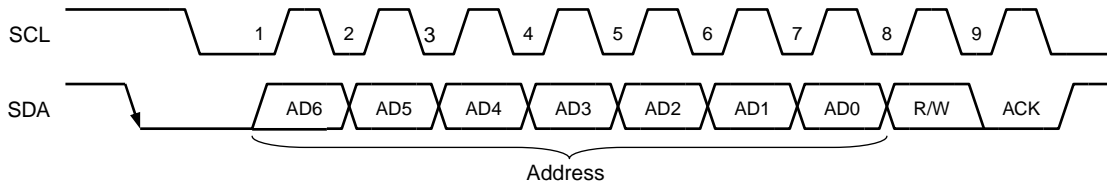
4.1.3 Transfer direction specification

The master device transmits 1-bit data for specifying the transfer direction after the 7-bit address data. If the transfer direction bit is set to 0, it means that the master device is transmitting data to a slave device. If the transfer direction bit is set to 1, it means that the master device is receiving data from a slave device.

Figure 4-4. Transfer Direction Specification
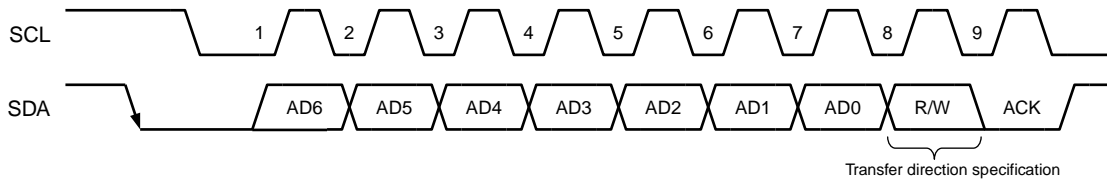
4.1.4 Acknowledge signal (ACK)

The ACK signal is used by the receiving side to notify the transmitting side of the reception of serial data.

The receiving side returns an ACK signal each time 8-bit data is received. An ACK signal is generated by pulling the SDA line low during the 9th high-level period of the clock on the SCL line.

After transmitting 8-bit data, the transmitting side checks if an ACK signal has been returned from the receiving side.

If an ACK signal is returned, the master device proceeds to the next processing, assuming that the data has been received normally. If no ACK signal has been returned from the slave device, the data is not received normally. In this case, the master device outputs a stop condition to stop transmission.

Figure 4-5. Acknowledge Signal
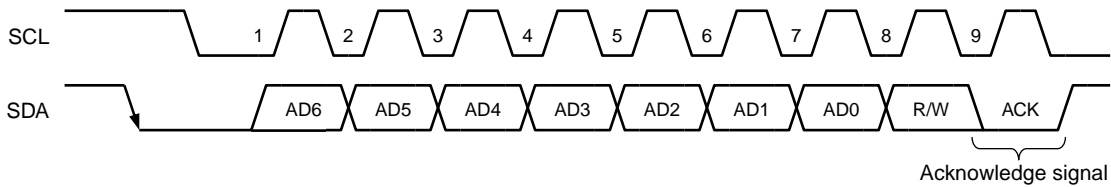
4.1.5 Stop condition

A stop condition is issued when the SCL line is high (when serial transfer ends and the serial clock is not output) and the SDA line is pulled high.

A stop condition is a signal output by the master device to a slave device when a serial transfer ends.

The I^2C interface incorporates hardware for detecting a stop condition in slave operation.

Figure 4-6. Stop Condition
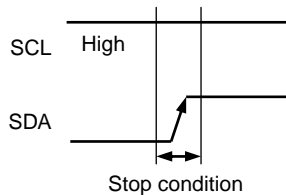
4.1.6 Wait signal (WAIT)

The wait signal is used by the master/slave device to notify the communication destination that the master/slave device is preparing for data transmission/reception (that is, the device is in the wait state).

By pulling the SCL line low, the master/slave device reports its wait state to the communication destination.

When the WAIT signal is canceled, the master device can start the next transfer operation.

Figure 4-7. Wait Signal

(a) Waiting for 8 clock cycles
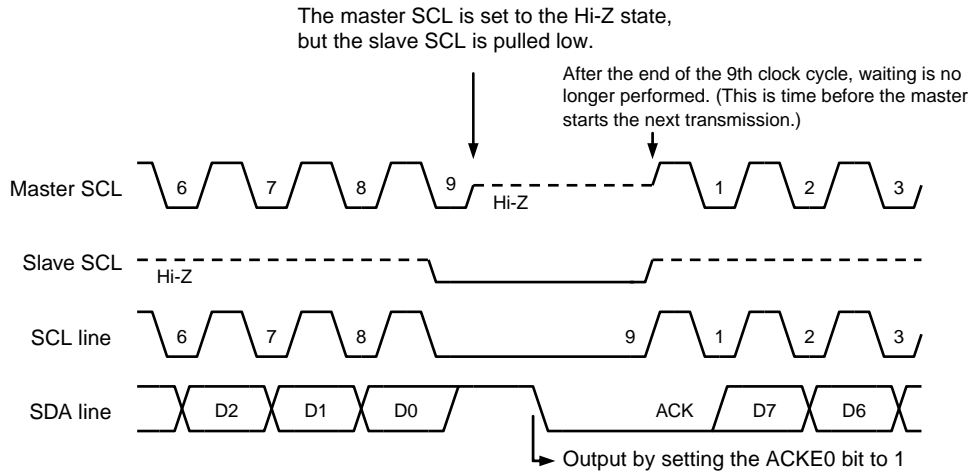
(b) Waiting for 9 clock cycles
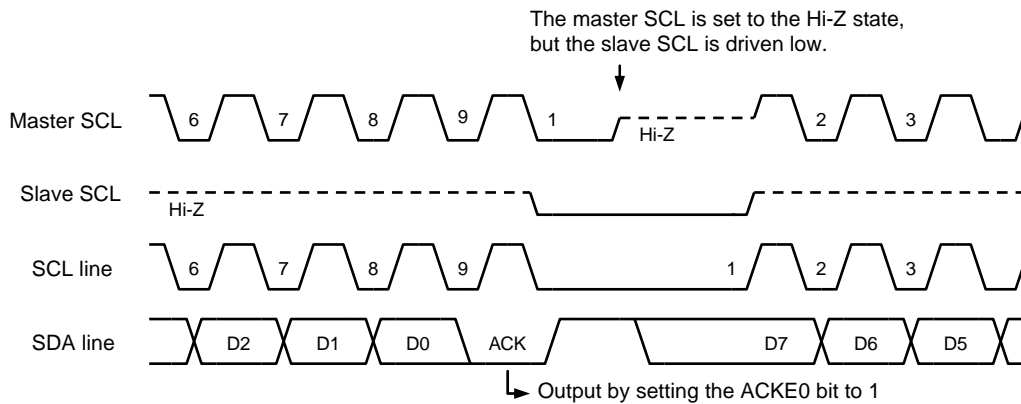
4.2 Shift Register (IIC_IIC0) Operation

The shift register (IIC_IIC0) performs a shift operation at the rising edge of the serial clock (SCL). At the rising edge of the SCL line, the register shifts one bit toward the MSB, and the value of the SDA line is read into the LSB.
Figure 4-8 shows an example of the IIC_IIC0 register shift operation.

Figure 4-8. Example of Shift Register Operation (During Address Transfer with a 9-Clock-Cycle Wait)
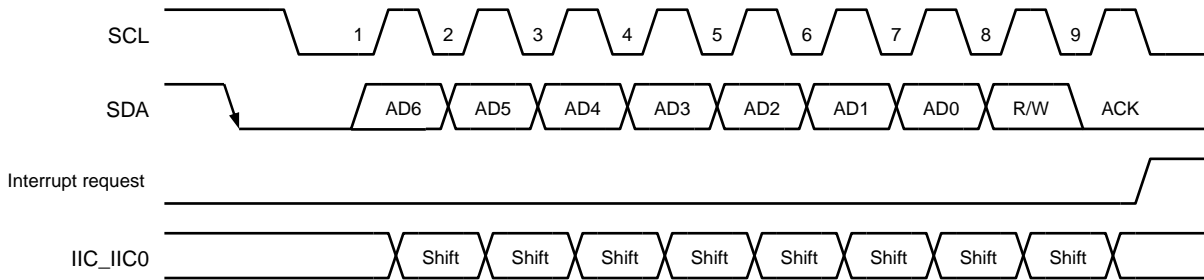
4.3 Extension Code

When the higher 4 bits of a received address are 0000b or 1111b, the extension code reception flag (EXC0) is set to 1 and an interrupt request signal is sent at the 8th falling edge of the clock, assuming the reception of an extension code.
The address stored in the SVA0 register is not affected.
For example, if 111110xxb is set in the SVA0 register and 111110xxb is transferred from the master device in a 10-bit address transfer, the EXC0 bit of the IIC_IICSE0 register is set to 1 because the higher 4 bits of data matches, and the COI0 bit of the IIC_IICSE0 register is set to 1 because the higher 7 bits of data matches.
Note, however, that an interrupt request signal is sent at the 8th falling edge of the clock.
The processing performed after an interrupt request signal is sent depends on the data that follows the extension code. This data should be processed by using software.
To disable slave operation after reception of an extension code, set the LREL0 bit of the IIC_IICC0 register to 1. This sets the communication standby state.

Table 4-1. Extension Code Bit Definition

Slave Address	R/W Bit	Explanation
0000000b	0	General call address
0000000b	1	Start byte
0000001b	x	CBUS address
0000010b	x	Address reserved for a different bus format
0000011b	x	Address reserved for future use
00001xxb	x	
11111xxb	x	
11110xxb	x	10-bit slave address specification

Remark x: Undefined

4.4 Arbitration

When multiple master devices issue a start condition at the same time, the I^2C interface compares the 7-bit address output from each master device with the SDA value, and grants the bus to the master device whose address matches the SDA line. This operation is called arbitration, and if a device is not granted the bus as a result of arbitration, such state is called arbitration loss.

The master that lost arbitration sets the ALD0 flag to 1 when the loss is determined, and waits as a slave with the SCL and SDA lines kept in the Hi-Z state.

The ALD0 flag must be detected by using software when the next interrupt request is issued.

For the interrupt generation timing, see **4.5 Interrupts.**

Figure 4-9. Example of Arbitration
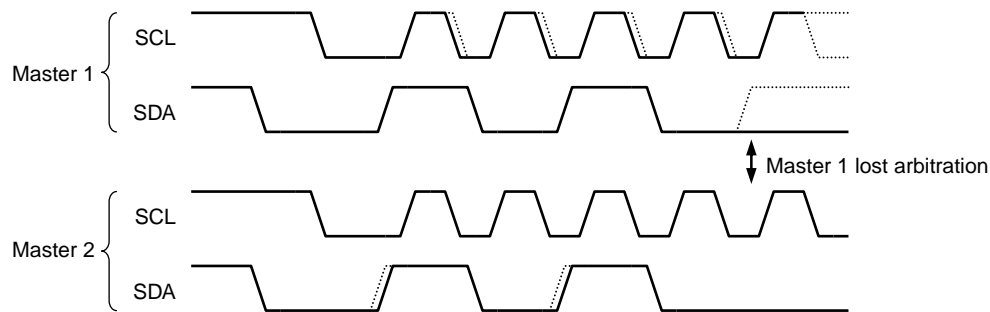
Arbitration occurs under the following conditions:

<1> During address transfer
<2> During R/W information transfer after address transfer
<3> During extension code transfer
<4> During R/W information transfer after extension code transfer
<5> During data transfer
<6> During ACK transfer after data reception
<7> If a restart condition is detected during data transfer.
<8> If a stop condition is detected during data transfer.
<9> If the SDL line is low level when a master attempts to issue a restart condition.
<10> If a stop condition is detected when a master attempts to issue a restart condition.
<11> If the SDL line is low level when a master attempts to issue a stop condition.
<12> If the SCL line is pulled low when a master attempts to issue a restart condition.

Remark In the case of <1> to <7>, <9>, <11>, and <12>, an interrupt request is issued at the basic timing (at the 8th falling edge or the 9th rising edge of the clock after byte transfer).

In the case of <8> and <10>, an interrupt request is issued when a stop condition interrupt is generated while the SPIE0 bit of the IIC_IICC0 register is set to 1. Be sure to set the SPIE0 bit to 1 if arbitration might occur during master operation.

4.5 Interrupts

This section describes the timing at which an interrupt request is issued by the I^2C interface and indicates the value of the IIC_IICSE0 register when the interrupt is generated.

An interrupt signal is generated at the following timing:

<1> At the 8th or 9th falling edge of the serial clock (IIC_SCLK) (controlled by the WTIM0 bit of the IIC_IICC0 register)

<2> When a stop condition is detected (controlled by the SPIE0 bit of the IIC_IICC0 register)

Remarks 1. △ and ▲ show the timing at which an interrupt occurs.

An interrupt might not occur at △, depending on the state of the SPIE0 bit.

2. A value of "x" in the IIC_IICSE0 register does not represent an undefined value, but means that either 1 or 0 may be assumed.

3. The following symbols are used:
- ST: Start condition
- AD6-AD0: Address data
- RW: Transfer direction specification (R/W)
- AK: Acknowledge signal (ACK)
- D7-D0: Transfer data
- SP: Stop condition

4.5.1 Master operation

Figure 4-10. Timing for Master Operation (1/2)

(1) Start → Address → Data → Data → ⋯ → Stop (when WTIM0 = 0)

ST	AD6-AD0	RW	AK	D7-D0	AK	D7-D0	AK	SP

▲1   ▲2   ▲3 ▲4 △5
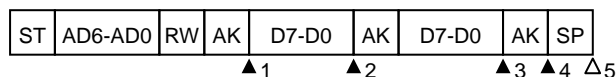
▲1: IIC_IICSE0 = 1000x110

▲2: IIC_IICSE0 = 1000x000

▲3: IIC_IICSE0 = 1000x000 (The WTIM0 bit is set to 1.)

▲4: IIC_IICSE0 = 1000xx00 (The SPT0 bit is set to 1.)

△5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(2) Start → Address → Data → Data → ⋯ → Stop (when WTIM0 = 1)

ST	AD6-AD0	RW	AK	D7-D0	AK	D7-D0	AK	SP

▲1   ▲2   ▲3 △4
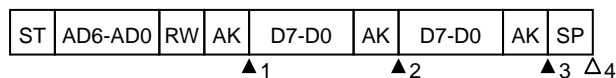
▲1: IIC_IICSE0 = 1000x110

▲2: IIC_IICSE0 = 1000x100

▲3: IIC_IICSE0 = 1000xx00 (The SPT0 bit is set to 1.)

△4: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

Figure 4-10. Timing for Master Operation (2/2)

(3) Start → Address → Data → ··· → Start → Address → Data → ··· → Stop (when WTIM0 = 0)
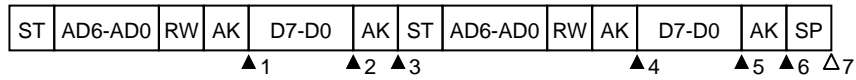
ST	AD6-AD0	RW	AK	D7-D0	AK	ST	AD6-AD0	RW	AK	D7-D0	AK	SP

▲1 ▲2 ▲3 ▲4 ▲5 ▲6 △7

- ▲1: IIC_IICSE0 = 1000x110
- ▲2: IIC_IICSE0 = 1000x000 (The WTIM0 bit is set to 1.)
- ▲3: IIC_IICSE0 = 1000xx00 (The WTIM0 bit is cleared and the STT0 bit is set to 1.)
- ▲4: IIC_IICSE0 = 1000x110
- ▲5: IIC_IICSE0 = 1000x000 (The WTIM0 bit is set to 1.)
- ▲6: IIC_IICSE0 = 1000xx00 (The SPT0 bit is set to 1.)
- △7: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(4) Start → Address → Data → ··· → Start → Address → Data → ··· → Stop (when WTIM0 = 1)

ST	AD6-AD0	RW	AK	D7-D0	AK	ST	AD6-AD0	RW	AK	D7-D0	AK	SP

▲1 ▲2 ▲3 ▲4 △5
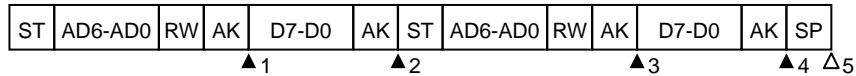
- ▲1: IIC_IICSE0 = 1000x110
- ▲2: IIC_IICSE0 = 1000xx00
- ▲3: IIC_IICSE0 = 1000x110
- ▲4: IIC_IICSE0 = 1000xx00 (The SPT0 bit is set to 1.)
- △5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(5) Start → Code → Data → Data → ··· → Stop (when WTIM0 = 0)

ST	AD6-AD0	RW	AK	D7-D0	AK	D7-D0	AK	SP

▲1 ▲2 ▲3 ▲4 △5
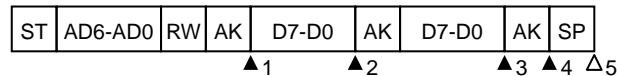
- ▲1: IIC_IICSE0 = 1010x110
- ▲2: IIC_IICSE0 = 1010x000
- ▲3: IIC_IICSE0 = 1010x000 (The WTIM0 bit is set to 1.)
- ▲4: IIC_IICSE0 = 1010xx00 (The SPT0 bit is set to 1.)
- △5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(6) Start → Code → Data → Data → ··· → Stop (when WTIM0 = 1)

ST	AD6-AD0	RW	AK	D7-D0	AK	D7-D0	AK	SP

▲1 ▲2 ▲3 △4
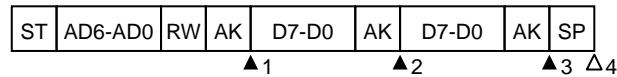
- ▲1: IIC_IICSE0 = 1010x110
- ▲2: IIC_IICSE0 = 1010x100
- ▲3: IIC_IICSE0 = 1010xx00 (The SPT0 bit is set to 1.)
- △4: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

4.5.2 Slave operation

(1) When slave address data is received (match with SVA0)

Figure 4-11. Timing for Slave Address Data Reception (1/2)

(a) Start → Address → Data → Data → ··· → Stop (when WTIM0 = 0)
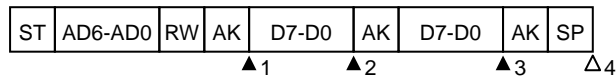
ST	AD6-AD0	RW	AK	D7-D0	AK	D7-D0	AK	SP

▲1 ▲2 ▲3 △4

▲1: IIC_IICSE0 = 0001x110
▲2: IIC_IICSE0 = 0001x000
▲3: IIC_IICSE0 = 0001x000
△4: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(b) Start → Address → Data → Data → ··· → Stop (when WTIM0 = 1)
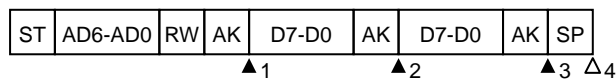
ST	AD6-AD0	RW	AK	D7-D0	AK	D7-D0	AK	SP

▲1 ▲2 ▲3 △4

▲1: IIC_IICSE0 = 0001x110
▲2: IIC_IICSE0 = 0001x100
▲3: IIC_IICSE0 = 0001xx00
△4: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(c) Start → Address → Data → ··· → Start → Address → Data → ··· → Stop (when WTIM0 = 0)
After restart, match with SVA0
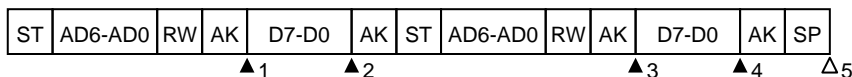
ST	AD6-AD0	RW	AK	D7-D0	AK	ST	AD6-AD0	RW	AK	D7-D0	AK	SP

▲1 ▲2 ▲3 ▲4 △5

▲1: IIC_IICSE0 = 0001x110
▲2: IIC_IICSE0 = 0001x000
▲3: IIC_IICSE0 = 0001x110
▲4: IIC_IICSE0 = 0001x000
△5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(d) Start → Address → Data → ··· → Start → Address → Data → ··· → Stop (when WTIM0 = 1)
After restart, match with SVA0

ST	AD6-AD0	RW	AK	D7-D0	AK	ST	AD6-AD0	RW	AK	D7-D0	AK	SP

▲1 ▲2 ▲3 ▲4 △5

▲1: IIC_IICSE0 = 0001x110
▲2: IIC_IICSE0 = 0001xx00
▲3: IIC_IICSE0 = 0001x110
▲4: IIC_IICSE0 = 0001xx00
△5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

Figure 4-11. Timing for Slave Address Data Reception (2/2)

(e) Start → Address → Data → ··· → Start → Code → Data → ··· → Stop (when WTIM0 = 0)
After restart, extension code reception

ST	AD6-AD0	RW	AK	D7-D0	AK	ST	AD6-AD0	RW	AK	D7-D0	AK	SP

▲1 ▲2 ▲3 ▲4 △5

▲1: IIC_IICSE0 = 0001x110
▲2: IIC_IICSE0 = 0001x000
▲3: IIC_IICSE0 = 0010x010
▲4: IIC_IICSE0 = 0010x000
△5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(f) Start → Address → Data → ··· → Start → Code → Data → ··· → Stop (when WTIM0 = 1)
After restart, extension code reception

ST	AD6-AD0	RW	AK	D7-D0	AK	ST	AD6-AD0	RW	AK	D7-D0	AK	SP

▲1 ▲2 ▲3 ▲4 ▲5 △6

▲1: IIC_IICSE0 = 0001x110
▲2: IIC_IICSE0 = 0001xx00
▲3: IIC_IICSE0 = 0010x010
▲4: IIC_IICSE0 = 0010x110
▲5: IIC_IICSE0 = 0010xx00
△6: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(g) Start → Address → Data → ··· → Start → Address → Data → ··· → Stop (when WTIM0 = 0)
After re start, address mismatch (other than extension code)

ST	AD6-AD0	RW	AK	D7-D0	AK	ST	AD6-AD0	RW	AK	D7-D0	AK	SP

▲1 ▲2 ▲3 △4

▲1: IIC_IICSE0 = 0001x110
▲2: IIC_IICSE0 = 0001x000
▲3: IIC_IICSE0 = 00000x10
△4: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(h) Start → Address → Data → ··· → Start → Address → Data → ··· → Stop (when WTIM0 = 1)
After re start, address mismatch (other than extension code)

ST	AD6-AD0	RW	AK	D7-D0	AK	ST	AD6-AD0	RW	AK	D7-D0	AK	SP

▲1 ▲2 ▲3 △4

▲1: IIC_IICSE0 = 0001x110
▲2: IIC_IICSE0 = 0001xx00
▲3: IIC_IICSE0 = 00000x10
△4: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

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(2) When an extension code is received

Figure 4-12. Timing for Extension Code Reception (1/2)

(a) Start → Code → Data → Data → ⋯ → Stop (when WTIM0 = 0)

ST	AD6-AD0	RW	AK	D7-D0	AK	D7-D0	AK	SP

▲1   ▲2   ▲3   △4

▲1: IIC_IICSE0 = 0010x010
▲2: IIC_IICSE0 = 0010x000
▲3: IIC_IICSE0 = 0010x000
△4: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(b) Start → Code → Data → Data → ⋯ → Stop (when WTIM0 = 1)
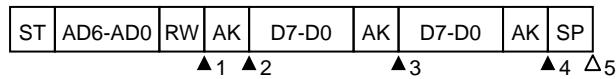
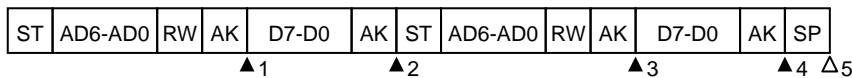| ST	AD6-AD0	RW	AK	D7-D0	AK	D7-D0	AK	SP

▲1 ▲2   ▲3   ▲4 △5

▲1: IIC_IICSE0 = 0010x010
▲2: IIC_IICSE0 = 0010x110
▲3: IIC_IICSE0 = 0010x100
▲4: IIC_IICSE0 = 0010xx00
△5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(c) Start → Code → Data → ⋯ → Start → Address → Data → ⋯ → Stop (when WTIM0 = 0)
After restart, match with SVA0
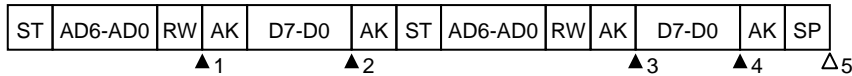
ST	AD6-AD0	RW	AK	D7-D0	AK	ST	AD6-AD0	RW	AK	D7-D0	AK	SP

▲1   ▲2   ▲3   ▲4   △5

▲1: IIC_IICSE0 = 0010x010
▲2: IIC_IICSE0 = 0010x000
▲3: IIC_IICSE0 = 0001x110
▲4: IIC_IICSE0 = 0001x000
△5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(d) Start → Code → Data → ⋯ → Start → Address → Data → ⋯ → Stop (when WTIM0 = 1)
After restart, match with SVA0

ST	AD6-AD0	RW	AK	D7-D0	AK	ST	AD6-AD0	RW	AK	D7-D0	AK	SP

▲1 ▲2   ▲3   ▲4   ▲5 △6
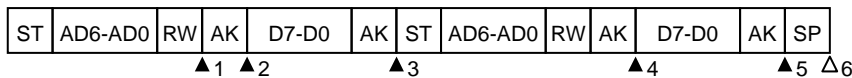
▲1: IIC_IICSE0 = 0010x010
▲2: IIC_IICSE0 = 0010x110
▲3: IIC_IICSE0 = 0010xx00
▲4: IIC_IICSE0 = 0001x110
▲5: IIC_IICSE0 = 0001xx00
△6: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

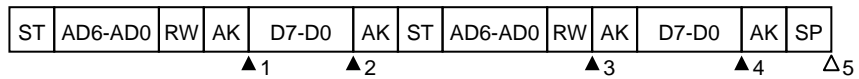**Figure 4-12. Timing for Extension Code Reception (2/2)**

(e) Start → Code → Data → ··· → Start → Code → Data → ··· → Stop (when WTIM0 = 0)
After restart, extension code reception
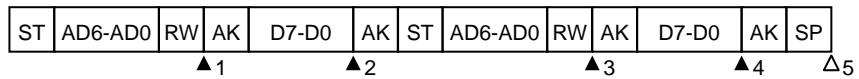
ST	AD6-AD0	RW	AK	D7-D0	AK	ST	AD6-AD0	RW	AK	D7-D0	AK	SP

▲1   ▲2   ▲3   ▲4   △5

▲1:   IIC_IICSE0 = 0010x010
▲2:   IIC_IICSE0 = 0010x000
▲3:   IIC_IICSE0 = 0010x010
▲4:   IIC_IICSE0 = 0010x000
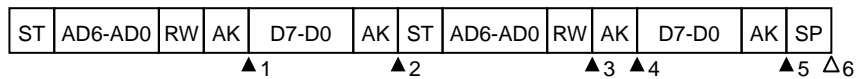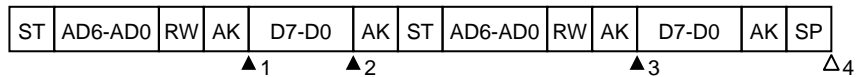△5:   IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(f) Start → Code → Data → ··· → Start → Code → Data → ··· → Stop (when WTIM0 = 1)
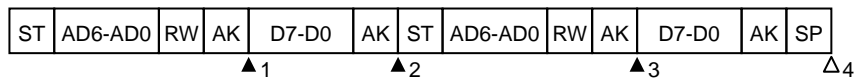**After restart, extension code reception**

ST	AD6-AD0	RW	AK	D7-D0	AK	ST	AD6-AD0	RW	AK	D7-D0	AK	SP

▲1 ▲2   ▲3   ▲4 ▲5   ▲6 △7
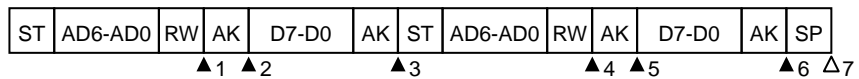
▲1:   IIC_IICSE0 = 0010x010
▲2:   IIC_IICSE0 = 0010x110
▲3:   IIC_IICSE0 = 0010xx00
▲4:   IIC_IICSE0 = 0010x010
▲5:   IIC_IICSE0 = 0010x110
▲6:   IIC_IICSE0 = 0010xx00
△7:   IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(g) Start → Code → Data → ··· → Start → Address → Data → ··· → Stop (when WTIM0 = 0)
After restart, address mismatch (other than extension code)

ST	AD6-AD0	RW	AK	D7-D0	AK	ST	AD6-AD0	RW	AK	D7-D0	AK	SP

▲1   ▲2   ▲3   △4
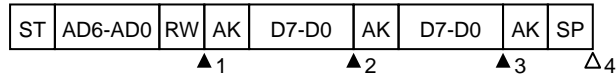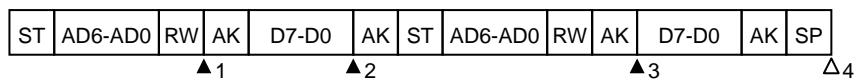
▲1:   IIC_IICSE0 = 0010x010
▲2:   IIC_IICSE0 = 0010x000
▲3:   IIC_IICSE0 = 00000x10
△4:   IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(h) Start → Code → Data → ··· → Start → Address → Data → ··· → Stop (when WTIM0 = 1)
After restart, address mismatch (other than extension code)

ST	AD6-AD0	RW	AK	D7-D0	AK	ST	AD6-AD0	RW	AK	D7-D0	AK	SP

▲1 ▲2   ▲3   ▲4   △5
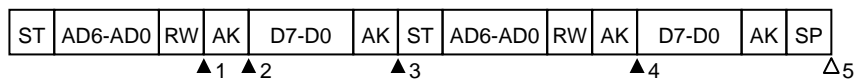
▲1:   IIC_IICSE0 = 0010x010
▲2:   IIC_IICSE0 = 0010x110
▲3:   IIC_IICSE0 = 0010xx00
▲4:   IIC_IICSE0 = 00000x10
△5:   IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

4.5.3 Operation at the time of an address mismatch

Figure 4-13. Timing in Address Mismatch

Start → Code → Data → Data → ⋯ → Stop

ST	AD6-AD0	RW	AK	D7-D0	AK	D7-D0	AK	SP

△1
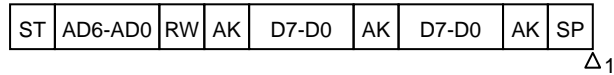
△1:   IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

4.5.4 Arbitration loss

(1) Operation as a slave after arbitration loss

Figure 4-14. Timing for Operation as a Slave After Arbitration Loss (1/2)

(a) When arbitration is lost during slave address data transmission (when WTIM0 = 0)

ST	AD6-AD0	RW	AK	D7-D0	AK	D7-D0	AK	SP

▲1   ▲2   ▲3   △4

▲1:   IIC_IICSE0 = 0101x110
      (Example: The ALD0 bit is read during interrupt servicing.)
▲2:   IIC_IICSE0 = 0001x000
▲3:   IIC_IICSE0 = 0001x000
△4:   IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(b) When arbitration is lost during slave address data transmission (when WTIM0 = 1)

ST	AD6-AD0	RW	AK	D7-D0	AK	D7-D0	AK	SP

▲1   ▲2   ▲3 △4

▲1:   IIC_IICSE0 = 0101x110
      (Example: The ALD0 bit is read during interrupt servicing.)
▲2:   IIC_IICSE0 = 0001x100
▲3:   IIC_IICSE0 = 0001xx00
△4:   IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

**(c) When arbitration is lost during extension code transmission (when WTIM0 = 0)**

ST	AD6-AD0	RW	AK	D7-D0	AK	D7-D0	AK	SP

▲1   ▲2   ▲3   △4

▲1:   IIC_IICSE0 = 0110x010 (Example: The ALD0 bit is read during interrupt
      servicing.)
▲2:   IIC_IICSE0 = 0010x000
▲3:   IIC_IICSE0 = 0010x000
△4:   IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

Figure 4-14. Timing for Operation as a Slave After Arbitration Loss (2/2)

(d) When arbitration is lost during extension code transmission (when WTIM0 = 1)
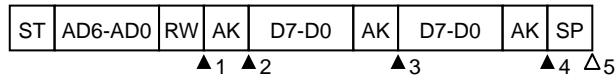
ST	AD6-AD0	RW	AK	D7-D0	AK	D7-D0	AK	SP

▲1 ▲2   ▲3   ▲4 △5

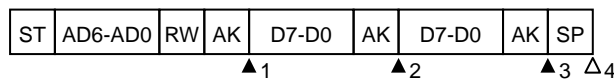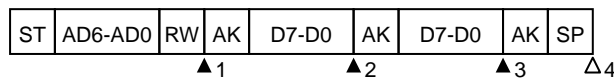▲1:   IIC_IICSE0 = 0110x010

(Example: The ALD0 bit is read during interrupt servicing.)

▲2:   IIC_IICSE0 = 0010x110

▲3:   IIC_IICSE0 = 0010x100

▲4:   IIC_IICSE0 = 0010xx00

△5:   IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(2) When participation in communication is disabled after arbitration loss

Figure 4-15. Timing When Participation in Communication Is Disabled After Arbitration Loss (1/3)

(a) When arbitration is lost during slave address data transmission (when WTIM0 = 1)
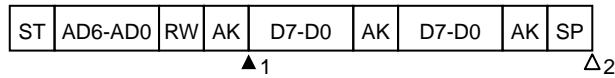
ST	AD6-AD0	RW	AK	D7-D0	AK	D7-D0	AK	SP

▲1   △2

▲1:   IIC_IICSE0 = 01000110

(Example: The ALD0 bit is read during interrupt servicing.)

△2:   IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(b) When arbitration is lost during data transfer (when WTIM0 = 0)

ST	AD6-AD0	RW	AK	D7-D0	AK	D7-D0	AK	SP

▲1   ▲2   △3

▲1:   IIC_IICSE0 = 10001110

▲2:   IIC_IICSE0 = 01000000

(Example: The ALD0 bit is read during interrupt servicing.)

△3:   IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(c) When arbitration is lost during data transfer (when WTIM0 = 1)

ST	AD6-AD0	RW	AK	D7-D0	AK	D7-D0	AK	SP

▲1   ▲2   △3
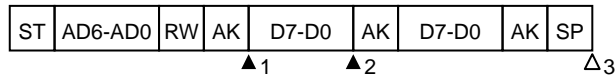
▲1:   IIC_IICSE0 = 10001110

▲2:   IIC_IICSE0 = 01000100

(Example: The ALD0 bit is read during interrupt servicing.)

△3:   IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(d) When arbitration of a restart condition is lost during data transfer
Other than extension code (Example: Mismatch with SVA0, WTIM0 = 1)

ST	AD6-AD0	RW	AK	D7-Dn	ST	AD6-AD0	RW	AK	D7-D0	AK	SP

▲1   ▲2   △3

▲1: IIC_IICSE0 = 1000x110

▲2: IIC_IICSE0 = 01000110

(Example: The ALD0 bit is read during interrupt servicing.)

△3: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

**Figure 4-15. Timing When Participation in Communication Is Disabled After Arbitration Loss (2/3)**

(e) When arbitration of a stop condition is lost during data transfer

ST	AD6-AD0	RW	AK	D7-Dn	SP

▲1   △2

▲1: IIC_IICSE0 = 1000x110

△2: IIC_IICSE0 = 01000001 (Only when the SPIE0 bit is set to 1.)

(f) When arbitration is lost because a restart condition could not be generated
due to a low data level (when WTIM0 = 0)

STT0 = 1

ST	AD6-AD0	RW	AK	D7-D0	AK	D7-D0	AK	D7-D0	AK	SP

▲1   ▲2 ▲3   ▲4   △5

▲1: IIC_IICSE0 = 1000x110

▲2: IIC_IICSE0 = 1000x000 (The WTIM0 bit is set to 1.)

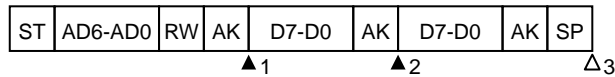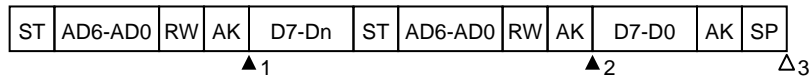▲3: IIC_IICSE0 = 1000xx00 (The WTIM0 bit is cleared and the STT0 bit is set to 1.)

▲4: IIC_IICSE0 = 01000000

(Example: The ALD0 bit is read during interrupt servicing.)

△5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(g) When arbitration is lost because a restart condition could not be generated
due to a low data level (when WTIM0 = 1)

STT0 = 1

ST	AD6-AD0	RW	AK	D7-D0	AK	D7-D0	AK	D7-D0	AK	SP

▲1   ▲2   ▲3   △4

▲1: IIC_IICSE0 = 1000x110

▲2: IIC_IICSE0 = 1000x100 (The STT0 bit is set to 1.)

▲3: IIC_IICSE0 = 01000100

(Example: The ALD0 bit is read during interrupt servicing.)

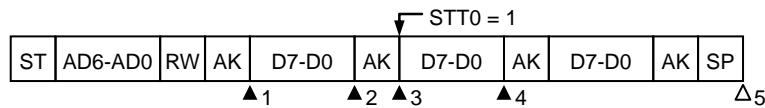△4: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(h) When arbitration is lost because a restart condition could not be generated
due to the generation of a stop condition (when WTIM0 = 0)

STT0 = 1

| ST | AD6-AD0 | RW | AK | D7-D0 | AK | SP |

▲1 ▲2 ▲3 △4

▲1: IIC_IICSE0 = 1000x110

▲2: IIC_IICSE0 = 1000x000 (The WTIM0 bit is set to 1.)

▲3: IIC_IICSE0 = 1000xx00 (The STT0 bit is set to 1.)

△4: IIC_IICSE0 = 01000001 (Only when the SPIE0 bit is set to 1.)

Figure 4-15. Timing When Participation in Communication Is Disabled After Arbitration Loss (3/3)

(i) When arbitration is lost because a restart condition could not be generated
due to the generation of a stop condition (when WTIM0 = 1)

STT0 = 1

| ST | AD6-AD0 | RW | AK | D7-D0 | AK | SP |

▲1 ▲2 △3

▲1: IIC_IICSE0 = 1000x110

▲2: IIC_IICSE0 = 1000xx00 (The STT0 bit is set to 1.)
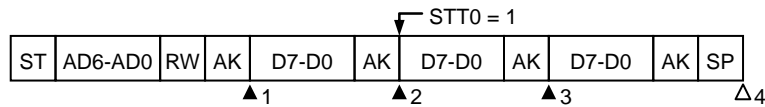
△3: IIC_IICSE0 = 01000001 (Only when the SPIE0 bit is set to 1.)

(j) When arbitration is lost because a stop condition could not be generated
due to a low data level (when WTIM0 = 0)

STT0 = 1

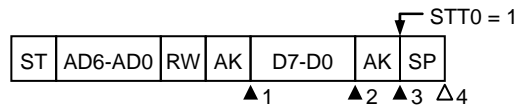| ST | AD6-AD0 | RW | AK | D7-D0 | AK | D7-D0 | AK | D7-D0 | AK | SP |

▲1 ▲2 ▲3 ▲4 △5
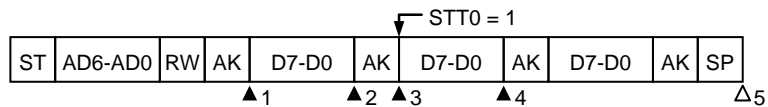
▲1: IIC_IICSE0 = 1000x110

▲2: IIC_IICSE0 = 1000x000 (The WTIM0 bit is set to 1.)

▲3: IIC_IICSE0 = 1000xx00 (The WTIM0 bit is cleared and the SPT0 bit is set to 1.)

▲4: IIC_IICSE0 = 01000000
(Example: The ALD0 bit is read during interrupt servicing.)

△5: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(k) When arbitration is lost because a stop condition could not be generated
due to a low data level (when WTIM0 = 1)

STT0 = 1

| ST | AD6-AD0 | RW | AK | D7-D0 | AK | D7-D0 | AK | D7-D0 | AK | SP |

▲1 ▲2 ▲3 △4

▲1: IIC_IICSE0 = 1000x110

▲2: IIC_IICSE0 = 1000xx00 (The SPT0 bit is set to 1.)

▲3: IIC_IICSE0 = 01000100
(Example: The ALD0 bit is read during interrupt servicing.)

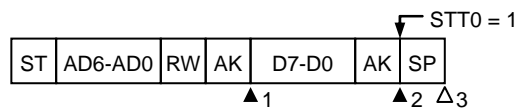△4: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

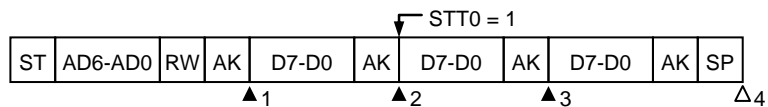**(3) When participation in communication is not performed after arbitration loss**

Figure 4-16. Timing When Participation in Communication Is Not Performed After Arbitration Loss

(a) When arbitration is lost during extension code transmission
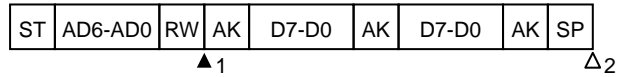
ST	AD6-AD0	RW	AK	D7-D0	AK	D7-D0	AK	SP

▲1 △2

▲1: IIC_IICSE0 = 0110x010

(Example: The ALD0 bit is read during interrupt servicing.)

The LREL0 bit is set to 1 by software.

△2: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

(b) When arbitration of a restart condition is lost during data transfer (extension code)

ST	AD6-AD0	RW	AK	D7-Dn	ST	AD6-AD0	RW	AK	D7-D0	AK	SP

▲1 ▲2 △3
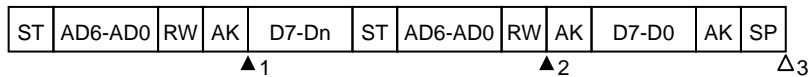
▲1: IIC_IICSE0 = 1000x110

▲2: IIC_IICSE0 = 0110x010

(Example: The ALD0 bit is read during interrupt servicing.)

The LREL0 bit is set to 0 by software.

△3: IIC_IICSE0 = 00000001 (Only when the SPIE0 bit is set to 1.)

4.6 Wake-up Operation

In a wake-up operation, an interrupt request signal is generated when the I^{2}C interface serves as a slave and the slave address and extension code are received.

An unnecessary interrupt is not generated unless the address matches, thus enhancing the efficiency of processing.

The wake-up standby state is set by the detection of a start condition.

Even during master operation (when a start condition has been issued), the master might be switched to a slave due to an arbitration loss. Therefore, the wake-up standby state needs to be set while an address is being transmitted.

Caution   The generation of a stop condition interrupt is enabled by setting the SPIE0 bit of the IIC_IICC0 register to 1, independent of the wake-up operation.

4.7 Acknowledge Signal (ACK)

The ACK signal is generated by pulling the SDA line low during the 9th high-level period of the clock on the SCL line.

When the ACKE0 bit of the IIC_IICC0 register is set to 1, generation of an ACK signal is enabled.

The TRC0 bit of the IIC_IICSE0 register is set to 0 or 1 according to the value of the 8th bit (LSB) of the address data. When the TRC0 bit is set to 0 (receiving side), the ACKE0 bit needs to be set to 1.

By setting the ACKE0 bit to 0, the slave receiving side (with the MSTS0 bit and TRC0 bit of the IIC_IICSE0 register set to 0) can request the master side not to start the next transfer if the next data is not required for some reason after the reception of multiple-byte data.

Similarly, by setting the ACKE0 bit to 0 to disable ACK signal generation, the master receiving side (with the MSTS0 bit set to 1 and the TRC0 bit set to 0) needs to warn the slave receiving side not to output MSB data on the SDA line if the next data is not required and a restart condition or stop condition needs to be issued.

4.8 Communication Reservation

If a device has failed to become either a master or a slave as a result of arbitration, or does not operate as a slave after an extension code has been received (if ACK is not returned and the bus is released by setting the LREL0 bit of the IIC_IICC0 register to 1), the device can participate in arbitration to become a master after the end of the current communication by reserving the next communication.

By setting the STT0 bit of the IIC_IICC0 register while the device is in the standby state, a start condition is automatically issued after the bus is released (after detection of a stop condition) and the device enters the wait state.

When a bus release detection (stop condition detection) interrupt is generated, the device starts address transfer as a master by writing to the IIC_IIC0 register.

At this time, the SPIE0 bit of the IIC_IICC0 register needs to be set to 1.

If the IIC_IIC0 register is written to before the stop condition detection interrupt is generated, the data is invalid.

4.9 Communication

4.9.1 Master operation

Figure 4- and Figure 4- show the communication procedure for master operation.

Figure 4-17. Start with Communication Reservation Enabled and Stop Condition Detected

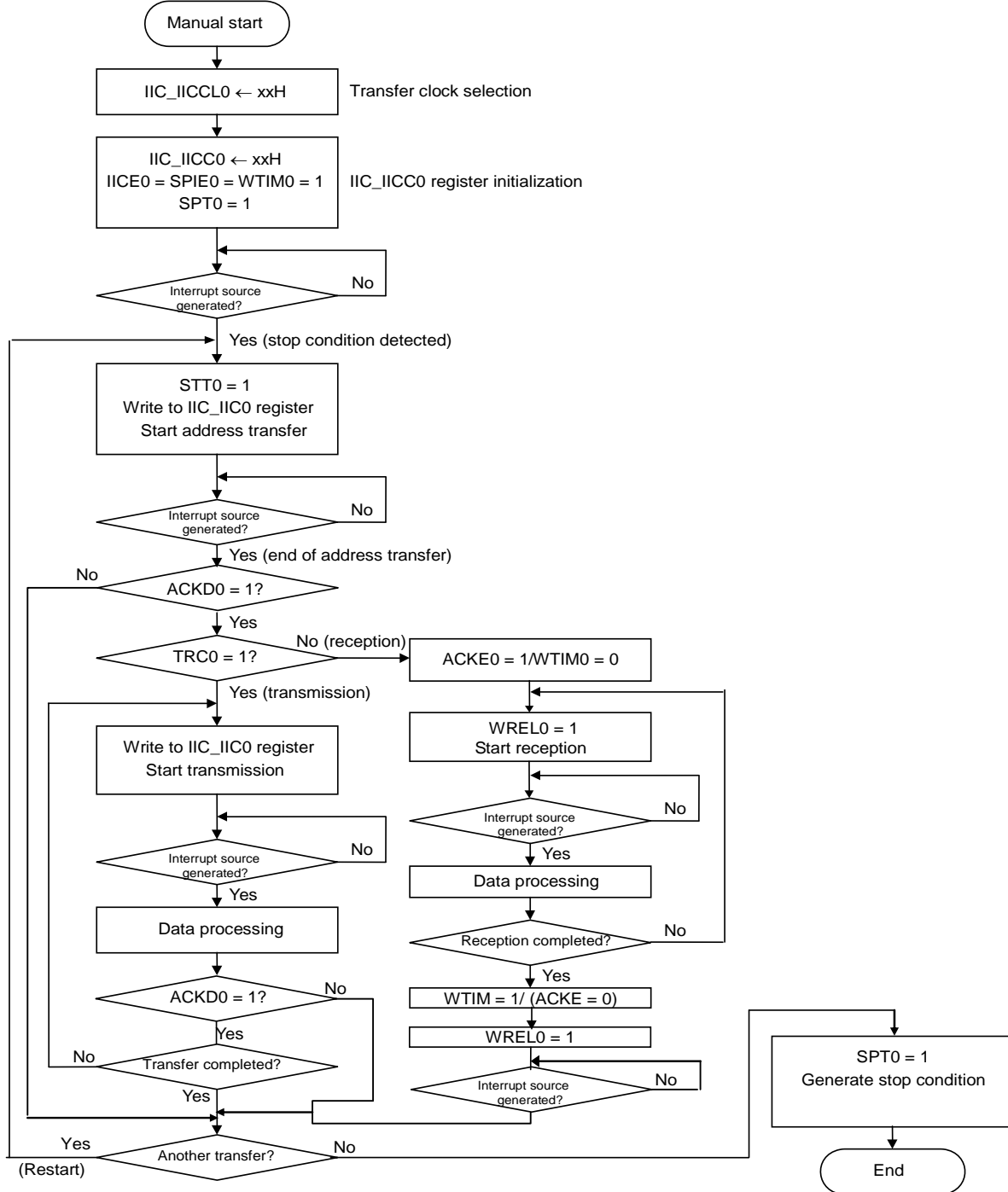**Figure 4-18. Start with Communication Reservation Disabled and Stop Condition Undetected**
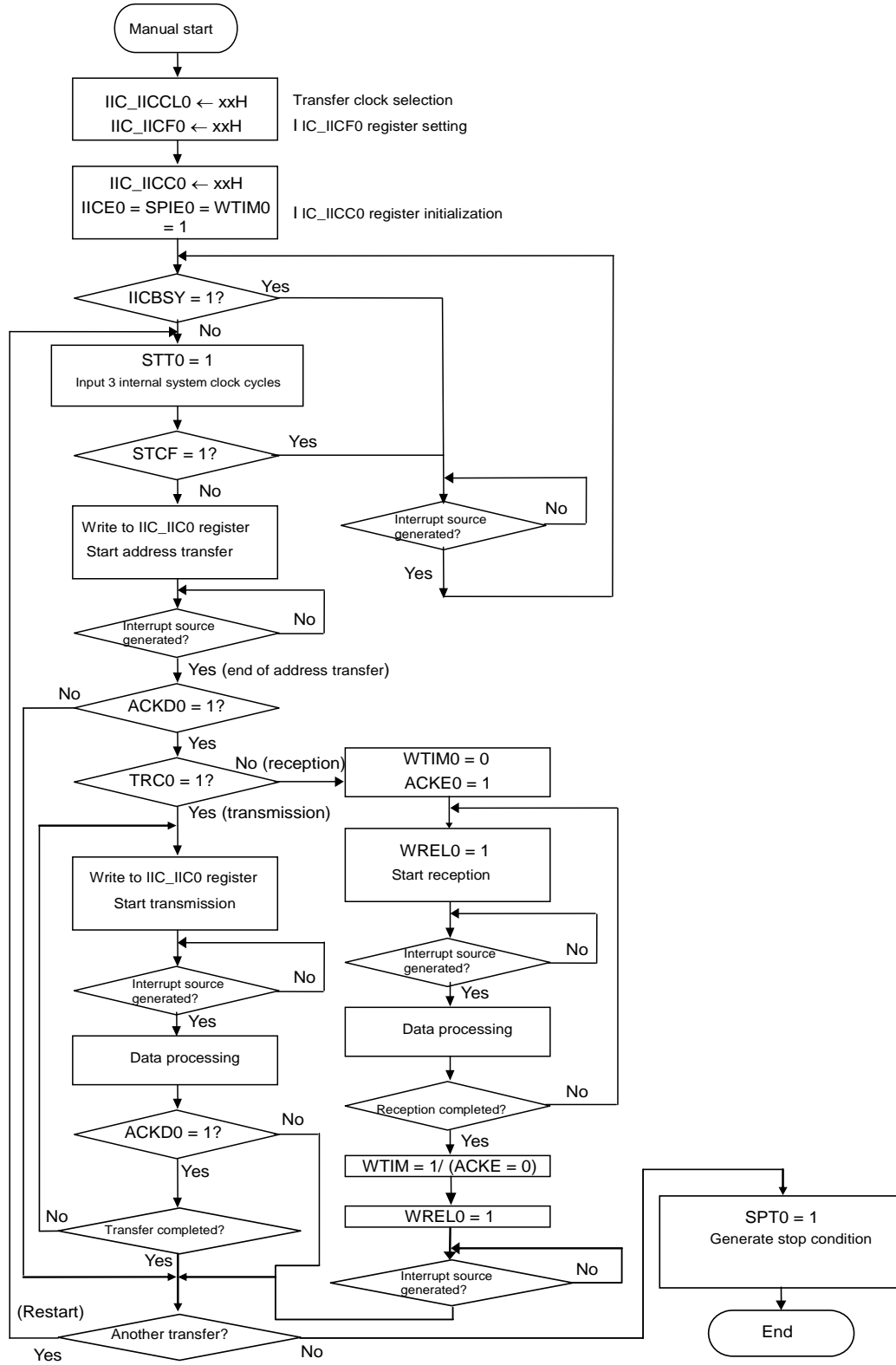
4.9.2 Slave operation

Figure 4-25 shows the communication procedure for slave operation.

Figure 4-19. Communication Procedure (Slave Operation)
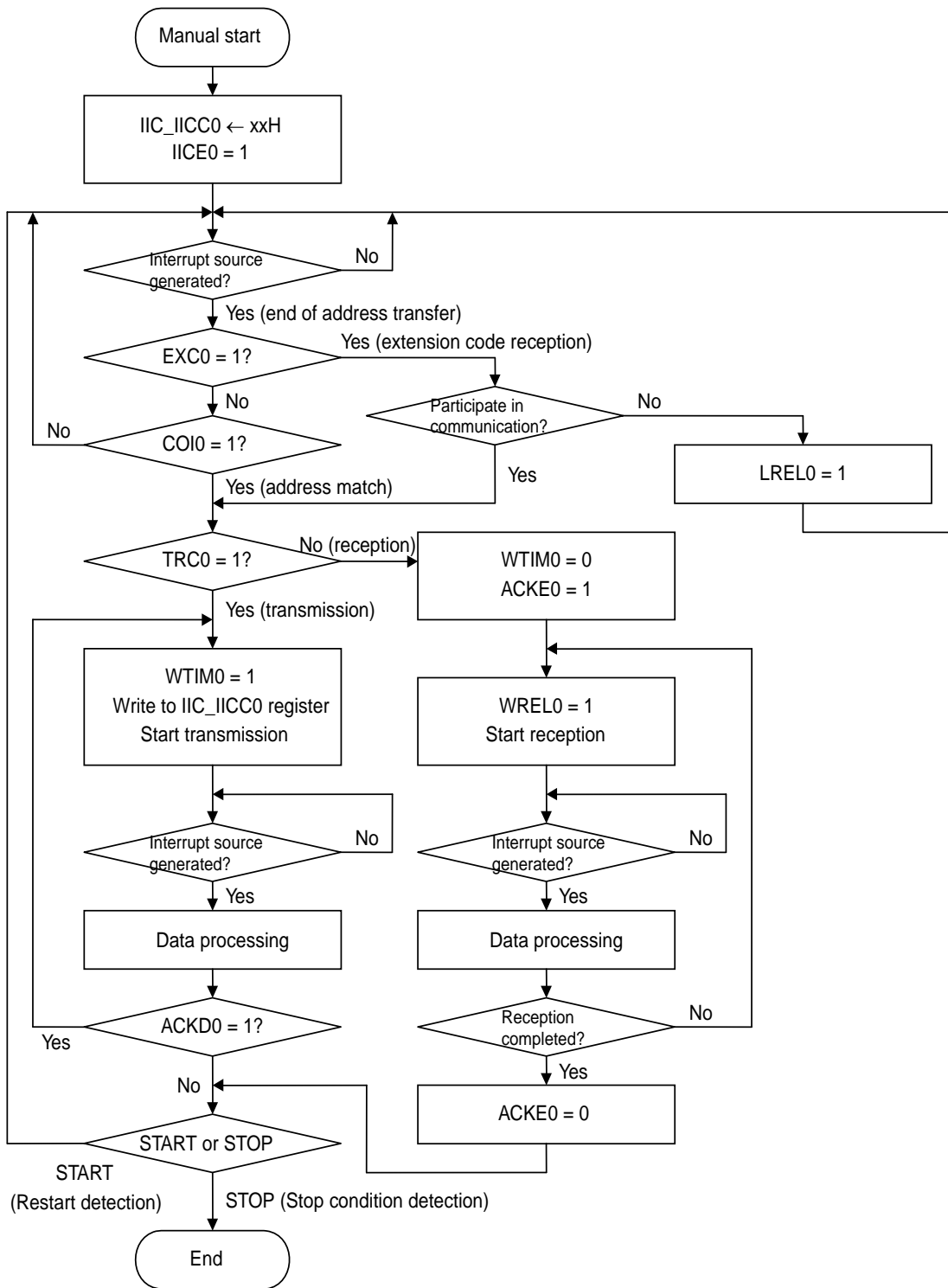
Revision History

Date	Revision	Comments
February 10, 2009	1.0	
April 27, 2009	2.0	Incremental update from comments to the 1.0.
June 8, 2009	3.0	Incremental update from comments to the 2.0.
September 30, 2009	4.0	Incremental update from comments to the 3.0.

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