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RENESAS

User's Manual

Multimedia Processor for Mobile Applications

Image Composer

EMMA Mobile™1

Document No. S19263EJ3V0UM00 (3rd edition)
Date Published September 2009

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M8E0904E

PREFACE

Readers

This manual is intended for hardware/software application system designers who wish to understand and use the image composer functions of EMMA Mobile1 (EM1), a multimedia processor for mobile applications.

Purpose

This manual is intended to explain to users the hardware and software functions of the image composer of EM1, and be used as a reference material for developing hardware and software for systems that use EM1.

Organization

This manual consists of the following chapters.

- Chapter 1 Overview
- Chapter 2 Registers
- Chapter 3 Description of functions
- Appendix A Terminology

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electricity, logic circuits, and microcontrollers.

To understand the functions of the image composer of EM1 in detail
→ Read this manual according to the **CONTENTS**.

To understand the other functions of EM1
→ Refer to the user's manual of the respective module.

To understand the electrical specifications of EM1
→ Refer to the Data Sheet.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH
Data type:	Word … 32 bits
	Halfword … 16 bits
	Byte … 8 bits

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name		Document No.
MC-10118A Data sheet		S19657E
μ PD77630A Data sheet		S19686E
User's manual	Audio/Voice and PWM Interfaces	S19253E
	DDR SDRAM Interface	S19254E
	DMA Controller	S19255E
	I^2C Interface	S19256E
	ITU-R BT.656 Interface	S19257E
	LCD Controller	S19258E
	MICROWIRE	S19259E
	NAND Flash Interface	S19260E
	SPI	S19261E
	UART Interface	S19262E
	Image Composer	This manual
	Image Processor Unit	S19264E
	System Control/General-Purpose I/O Interface	S19265E
	Timer	S19266E
	Terrestrial Digital TV Interface	S19267E
	Camera Interface	S19285E
	USB Interface	S19359E
	SD Memory Card Interface	S19361E
	PDMA	S19373E
	One Chip (MC-10118A)	S19598E
	One Chip (μ PD77630A)	S19687E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

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LIST OF FIGURES

LIST OF TABLES

CHAPTER 1 OVERVIEW

1.1 General

The image composer (IMC) generates images to be displayed in the LCD by the LCD controller.

1.2 Features

The main features of the IMC are as follows.

○ Supported image size
- Horizontal direction: Up to 2,046 pixels
- Vertical direction: Up to 2,046 lines

○ Data format
- Input: RGB565, RGB666, ARGB4444, YUV422[Note 1], YUV420[Note 2]
- Output: RGB565, RGB666

○ YUV-to-RGB conversion, dithering, gain offset
- Gain and offset can be adjusted for YUV components, from 0 to x2
- When the input data format is YUV, RGB conversion can be performed with two types of coefficients
- Dithering by using 2 × 2 matrix upon subtracting colors for converting images into RGB666

○ Overlay function
- Up to four layers can be synthesized. (Features of each layer are described later.)
- Position and size of synthesized planes can be set flexibly.
- Each layer can be defined independently in two dimensions, and formatting, mirror flipping, resizing, double buffering, and gain/offset adjustment can be set separately. (Whether this function is supported varies in each layer.)
- Transparent color and alpha blending can be used for the two front layers.

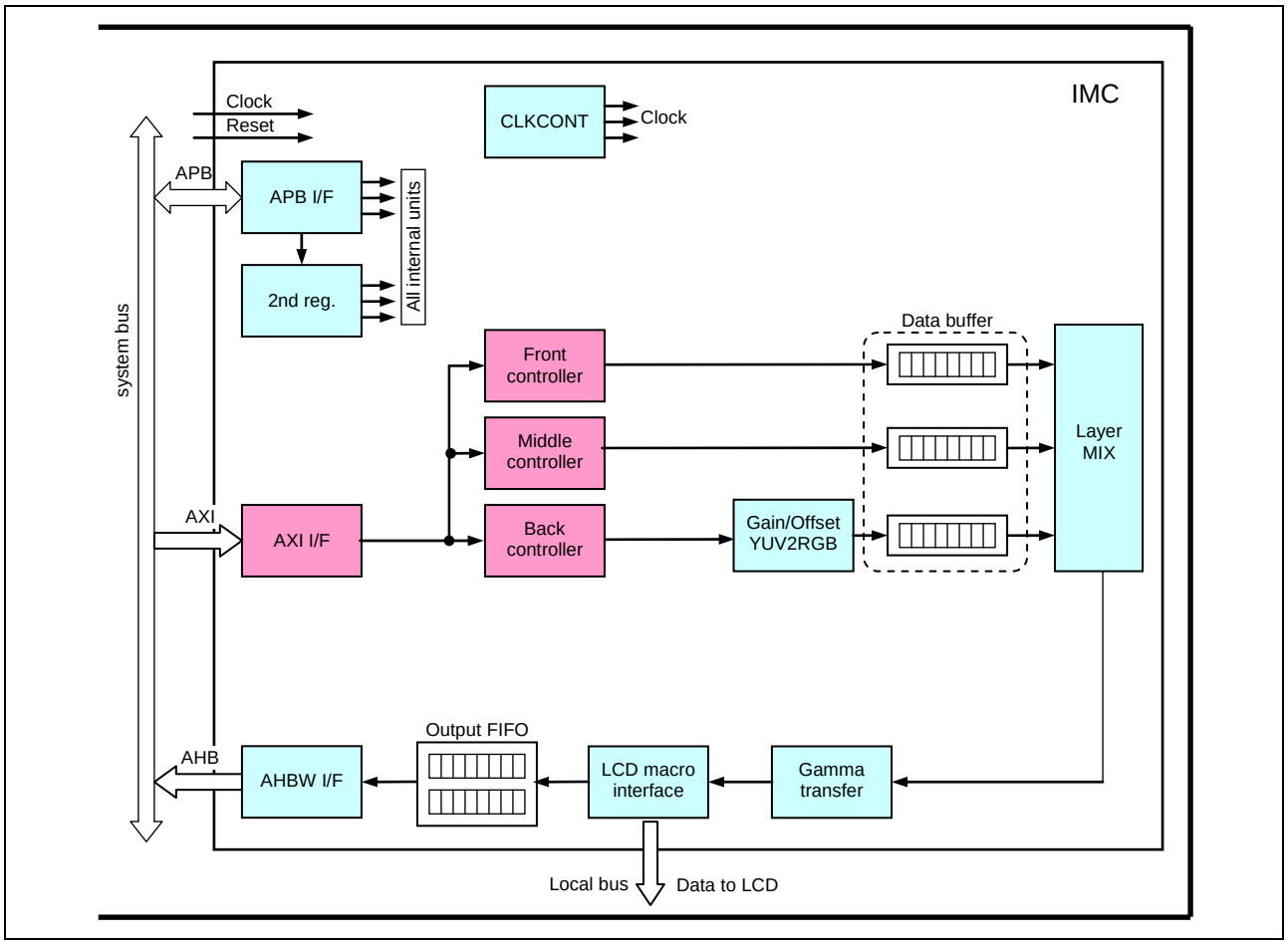
○ Gamma adjustment by table referencing

Notes 1. The YUV422 format has three storage methods: Pixel Interleave, in which 2-pixel data (Y component × 2, U component × 1, V component × 1) is stored as a set of one word, Semi-Planar, in which Y components are stored as a plane and UV components are stored as a plane, and Planar, in which YUV components are stored as three respective planes.

2. The YUV420 format has two storage methods: Semi-Planar, in which Y components are stored as a plane and UV components are stored as a plane and Planar, in which YUV components are stored as three respective planes.

1.3 Function Block Diagram

Figure 1-1. Function Block Diagram



CHAPTER 2 REGISTERS

The IMC registers can be accessed via the APB bus only in 32-bit (word) units.

2.1 Registers

Base address: 4026_0000H

Caution Among addresses 4026_0000H to 4026_FFFCH, the addresses not listed in the following tables are reserved. Write accessing reserved areas is prohibited. An undefined value is returned for read access.

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Address	Register Name	Symbol	R/W	Frame Sync	After Reset
Function setting registers					
0000H	Control register	IMC_CONTROL	R/W	×	0000_0000H
0004H	Update reserve register	IMC_REFRESH	R/W	–	0000_0000H
Image synthesis startup registers					
0010H	Startup register	IMC_START	R/W	○	0000_0000H
0014H	Status register	IMC_STATUS	R	○	0000_0000H
0018H	CPU double buffer control register	IMC_CPUBUFSEL	R/W	○	0000_0000H
Gamma correction registers					
0020H	Gamma correction control register	IMC_GAMMA_EN	R/W	×	0000_0000H
0024H	Gamma correction table address register	IMC_GAMMA_ADR	R/W	×	0000_0000H
0028H	Gamma correction table data register	IMC_GAMMA_DATA	R/W	×	0000_0000H
Registers for settings for immediate startup					
0040H	Display area address register	IMC_WB_AREAADR	R/W	×	0000_0000H
0044H	Address addition value register	IMC_WB_HOFFSET	R/W	×	0000_0000H
0048H	Format register	IMC_WB_FORMAT	R/W	×	0000_0000H
004CH	WB image size register	IMC_WB_SIZE	R/W	×	0000_0000H
Registers for setting common items to all layers					
0100H	Horizontal/vertical flip setting register	IMC_MIRROR	R/W	○	0000_0000H
0104H	Y gain offset register	IMC_YGAINOFFSET	R/W	×	0000_0080H
0108H	U gain offset register	IMC_UGAINOFFSET	R/W	×	0000_0080H
010CH	V gain offset register	IMC_VGAINOFFSET	R/W	×	0000_0080H
0110H	YUV2RGB conversion mode register	IMC_YUV2RGB	R/W	×	0000_0000H
0114H	Custom coefficient register (Coef R0)	IMC_COEF_R0	R/W	×	0000_0000H
0118H	Custom coefficient register (Coef R1)	IMC_COEF_R1	R/W	×	0000_0000H
011CH	Custom coefficient register (Coef R2)	IMC_COEF_R2	R/W	×	0000_0000H
0120H	Custom coefficient register (Coef R3)	IMC_COEF_R3	R/W	×	0000_0000H
0124H	Custom coefficient register (Coef G0)	IMC_COEF_G0	R/W	×	0000_0000H
0128H	Custom coefficient register (Coef G1)	IMC_COEF_G1	R/W	×	0000_0000H

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Address	Register Name	Symbol	R/W	Frame Sync	After Reset
Registers for setting common items to all layers					
012CH	Custom coefficient register (Coef G2)	IMC_COEF_G2	R/W	×	0000_0000H
0130H	Custom coefficient register (Coef G3)	IMC_COEF_G3	R/W	×	0000_0000H
0134H	Custom coefficient register (Coef B0)	IMC_COEF_B0	R/W	×	0000_0000H
0138H	Custom coefficient register (Coef B1)	IMC_COEF_B1	R/W	×	0000_0000H
013CH	Custom coefficient register (Coef B2)	IMC_COEF_B2	R/W	×	0000_0000H
0140H	Custom coefficient register (Coef B3)	IMC_COEF_B3	R/W	×	0000_0000H
Layer 0 setting registers					
0200H	Layer 0 control register	IMC_L0_CONTROL	R/W	●	0000_0000H
0204H	Layer 0 format register	IMC_L0_FORMAT	R/W	●	0000_0000H
0210H	Layer 0 transparent color control register	IMC_L0_KEYENABLE	R/W	●	0000_0000H
0214H	Layer 0 transparent color register	IMC_L0_KEYCOLOR	R/W	×	0000_0000H
0218H	Layer 0 alpha register	IMC_L0_ALPHA	R/W	●	0000_0000H
0220H	Layer 0 resize register	IMC_L0_RESIZE	R/W	●	0000_0000H
0230H	Layer 0 address addition value register	IMC_L0_OFFSET	R/W	●	0000_0000H
0234H	Layer 0 start address register	IMC_L0_FRAMEADR	R/W	●	0000_0000H
0250H	Layer 0 display position register	IMC_L0_POSITION	R/W	●	0000_0000H
0254H	Layer 0 display size register	IMC_L0_SIZE	R/W	●	0000_0000H
Layer 1A setting registers					
0300H	Layer 1A control register	IMC_L1A_CONTROL	R/W	●	0000_0000H
0304H	Layer 1x format register	IMC_L1X_FORMAT	R/W	●	0000_0000H
0310H	Layer 1A transparent color control register	IMC_L1A_KEYENABLE	R/W	●	0000_0000H
0314H	Layer 1x transparent color register	IMC_L1X_KEYCOLOR	R/W	×	0000_0000H
0318H	Layer 1A alpha register	IMC_L1A_ALPHA	R/W	●	0000_0000H
0320H	Layer 1x resize register	IMC_L1X_RESIZE	R/W	●	0000_0000H
0330H	Layer 1x address addition value register	IMC_L1X_OFFSET	R/W	●	0000_0000H
0334H	Layer 1A start address register	IMC_L1A_FRAMEADR	R/W	●	0000_0000H
0350H	Layer 1A display position register	IMC_L1A_POSITION	R/W	●	0000_0000H
0354H	Layer 1A display size register	IMC_L1A_SIZE	R/W	●	0000_0000H
Layer 1B setting registers					
0400H	Layer 1B control register	IMC_L1B_CONTROL	R/W	●	0000_0000H
0410H	Layer 1B transparent color control register	IMC_L1B_KEYENABLE	R/W	●	0000_0000H
0418H	Layer 1B alpha register	IMC_L1B_ALPHA	R/W	●	0000_0000H
0434H	Layer 1B start address register	IMC_L1B_FRAMEADR	R/W	●	0000_0000H
0450H	Layer 1B display position register	IMC_L1B_POSITION	R/W	●	0000_0000H
0454H	Layer 1B display size register	IMC_L1B_SIZE	R/W	●	0000_0000H

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Address	Register Name	Symbol	R/W	Frame Sync	After Reset
Layer 1C setting registers					
0500H	Layer 1C control register	IMC_L1C_CONTROL	R/W	●	0000_0000H
0510H	Layer 1C transparent color control register	IMC_L1C_KEYENABLE	R/W	●	0000_0000H
0518H	Layer 1C alpha register	IMC_L1C_ALPHA	R/W	●	0000_0000H
0534H	Layer 1C start address register	IMC_L1C_FRAMEADR	R/W	●	0000_0000H
0550H	Layer 1C display position register	IMC_L1C_POSITION	R/W	●	0000_0000H
0554H	Layer 1C display size register	IMC_L1C_SIZE	R/W	●	0000_0000H
Layer 2A setting registers					
0600H	Layer 2A control register	IMC_L2A_CONTROL	R/W	●	0000_0000H
0604H	Layer 2A format register	IMC_L2A_FORMAT	R/W	●	0000_0000H
0608H	Layer 2A double buffer control register	IMC_L2A_BUFSEL	R/W	●	0000_0000H
060CH	Layer 2A byte lane register	IMC_L2A_BYTELANE	R/W	×	0000_E4E4H
0620H	Layer 2A resize register	IMC_L2A_RESIZE	R/W	●	0000_0000H
0624H	Layer 2A horizontal/vertical flip control register	IMC_L2A_MIRROR	R/W	●	0000_0000H
0630H	Layer 2A address addition value register	IMC_L2A_OFFSET	R/W	●	0000_0000H
0634H	Layer 2A start address register (YP)	IMC_L2A_FRAMEADR_YP	R/W	●	0000_0000H
0638H	Layer 2A start address register (UP)	IMC_L2A_FRAMEADR_UP	R/W	●	0000_0000H
063CH	Layer 2A start address register (VP)	IMC_L2A_FRAMEADR_VP	R/W	●	0000_0000H
0640H	Layer 2A start address register (YQ)	IMC_L2A_FRAMEADR_YQ	R/W	●	0000_0000H
0644H	Layer 2A start address register (UQ)	IMC_L2A_FRAMEADR_UQ	R/W	●	0000_0000H
0648H	Layer 2A start address register (VQ)	IMC_L2A_FRAMEADR_VQ	R/W	●	0000_0000H
0650H	Layer 2A display position register	IMC_L2A_POSITION	R/W	●	0000_0000H
0654H	Layer 2A display size register	IMC_L2A_SIZE	R/W	●	0000_0000H
Layer 2B setting registers					
0700H	Layer 2B control register	IMC_L2B_CONTROL	R/W	●	0000_0000H
0704H	Layer 2B format register	IMC_L2B_FORMAT	R/W	●	0000_0000H
0708H	Layer 2B double buffer control register	IMC_L2B_BUFSEL	R/W	●	0000_0000H
070CH	Layer 2B byte lane register	IMC_L2B_BYTELANE	R/W	×	0000_E4E4H
0720H	Layer 2B resize register	IMC_L2B_RESIZE	R/W	●	0000_0000H
0724H	Layer 2B horizontal/vertical flip control register	IMC_L2B_MIRROR	R/W	●	0000_0000H
0730H	Layer 2B address addition value register	IMC_L2B_OFFSET	R/W	●	0000_0000H
0734H	Layer 2B start address register (YP)	IMC_L2B_FRAMEADR_YP	R/W	●	0000_0000H
0738H	Layer 2B start address register (UP)	IMC_L2B_FRAMEADR_UP	R/W	●	0000_0000H
073CH	Layer 2B start address register (VP)	IMC_L2B_FRAMEADR_VP	R/W	●	0000_0000H
0740H	Layer 2B start address register (YQ)	IMC_L2B_FRAMEADR_YQ	R/W	●	0000_0000H
0744H	Layer 2B start address register (UQ)	IMC_L2B_FRAMEADR_UQ	R/W	●	0000_0000H
0748H	Layer 2B start address register (VQ)	IMC_L2B_FRAMEADR_VQ	R/W	●	0000_0000H
0750H	Layer 2B display position register	IMC_L2B_POSITION	R/W	●	0000_0000H
0754H	Layer 2B display size register	IMC_L2B_SIZE	R/W	●	0000_0000H

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Address	Register Name	Symbol	R/W	Frame Sync	After Reset
Layer BG setting registers					
0804H	Layer BG format register	IMC_BG_FORMAT	R/W	●	0000_0000H
0820H	Layer BG resize register	IMC_BG_RESIZE	R/W	●	0000_0000H
0830H	Layer BG address addition value register	IMC_BG_OFFSET	R/W	●	0000_0000H
0834H	Layer BG start address register	IMC_BG_FRAMEADR	R/W	●	0000_0000H
Special register					
1000H	ARGB4444 mode register	IMC_ARGBMODE	R/W	×	0000_0000H
Interrupt control registers					
0900H	Interrupt status register	IMC_INTSTATUS	R	×	0000_0000H
0904H	Interrupt raw status register	IMC_INTRAWSTATUS	R	×	0000_0000H
0908H	Interrupt enable set register	IMC_INTENSET	R/W	×	0000_0000H
090CH	Interrupt enable clear register	IMC_INTENCLR	W	×	0000_0000H
0910H	Interrupt source clear register	IMC_INTFFCLR	W	×	0000_0000H
0914H	AHBR error address register	IMC_AHBRERRADR	R/W	×	0000_0000H
0918H	AHBW error address register	IMC_AHBWERRADR	R/W	×	0000_0000H

Registers marked with ○ in the Frame Sync column are registers with which setting changes made in the register take effect when the frame start signal is received from the LCD controller (V-sync register).

Registers marked with ● are registers with which setting changes made in the register take effect when the frame start signal is received from the LCD controller while the update reserve register is set (update target register).

Registers marked with × are registers with which setting changes made in the register take effect immediately (immediately-reflected register). Changing the settings during macro operation is prohibited.

When the IMC operates in immediate startup mode, startup by setting the startup register is regarded as the request for frame transmission start from the LCD controller, and register values are updated.

When a two-stage register is read, the values of the first-stage register (values to be updated at the next frame) are read out.

For details on the update register, see **0 3.4.2 Register** update.

2.2 Register Functions

2.2.1 Control register

This register (IMC_CONTROL: 4026_0000H) sets the basic IMC operation.

This is an immediately-reflected register, so changing the settings during operation (STATUS bit of IMC_STATUS register ≠ 0) is prohibited.

31	30	29	28	27	26	25	24
DBGMODE	Reserved						

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved			CLKCNT				

7	6	5	4	3	2	1	0
Reserved						FORMAT	STARTMODE

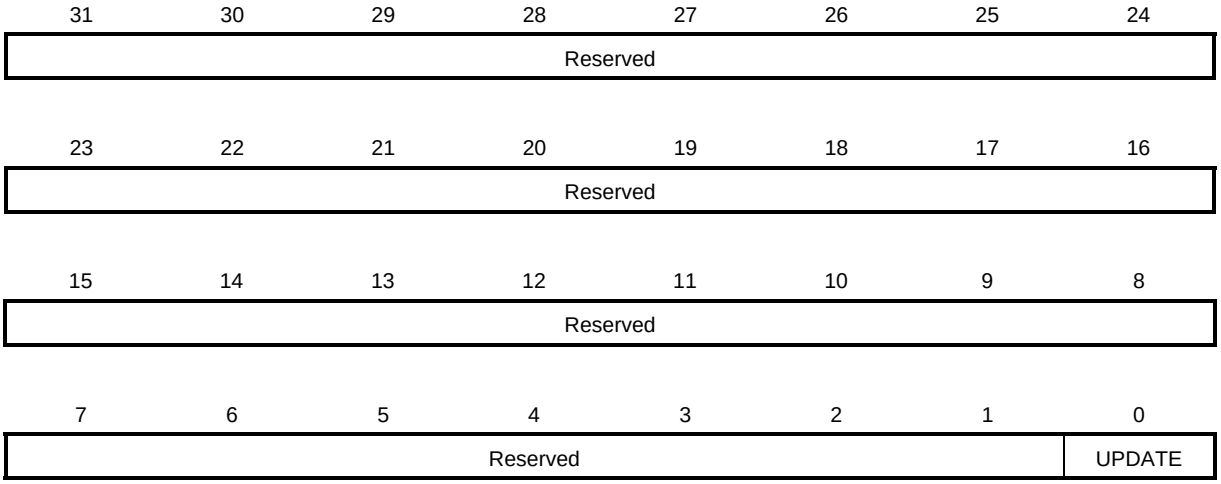
Name	R/W	Bit	After Reset	Function
DBGMODE	R/W	31	0	Sets the priority for supplying synthesized data to the LCD controller (with WB) 0: Availability of FIFO in LCD controller (IMC overrun is more likely to occur) 1: Availability of FIFO in LCD controller and transmit FIFO in IMC (IMC underrun is more likely to occur)
Reserved	R	30:13	0	Reserved. When these bits are read, 0 is returned for each bit.
CLKCNT	R/W	12:8	0	Enables the automatic clock control function in the IMC. 0: Disable (Clock is constantly supplied while the IMC is operating.) 1: Enable (Automatic clock control implemented in frame units.)
Reserved	R	7:2	0	Reserved. When these bits are read, 0 is returned for each bit.
FORMAT	R	1	0	Indicates the data format set by the LCD controller. 0: RGB666 1: RGB565 (IMC output format in LCD-synchronous mode)
STARTMODE	R/W	0	0	Sets the IMC startup mode. 0: LCD-synchronous mode (started by request from LCD controller) 1: Immediate startup mode (started by IMC_START register)

Bit	Block	Clock stop condition
bit 8	Front control	When Layer 0 not used
bit 9	Middle control	When Layer 1x not used
bit 10	Y2R	When YUV format not used
bit 11	Gamma correction	When Gamma correction function not used
bit 12	Write Back	When writeback function not used

When using the IMC with the settings made in the LCD controller, the startup signal is sent at the beginning of a frame transferred between the LCD controller and IMC. If STARTMODE = 0 in the IMC, the IMC starts operation at this timing.

2.2.2 Update reserve register

This register (IMC_REFRESH: 4026_0004H) is used to reflect the values set to the update target registers (registers marked with ● in the Frame Sync column in the register list) in the IMC, to the internal operation.

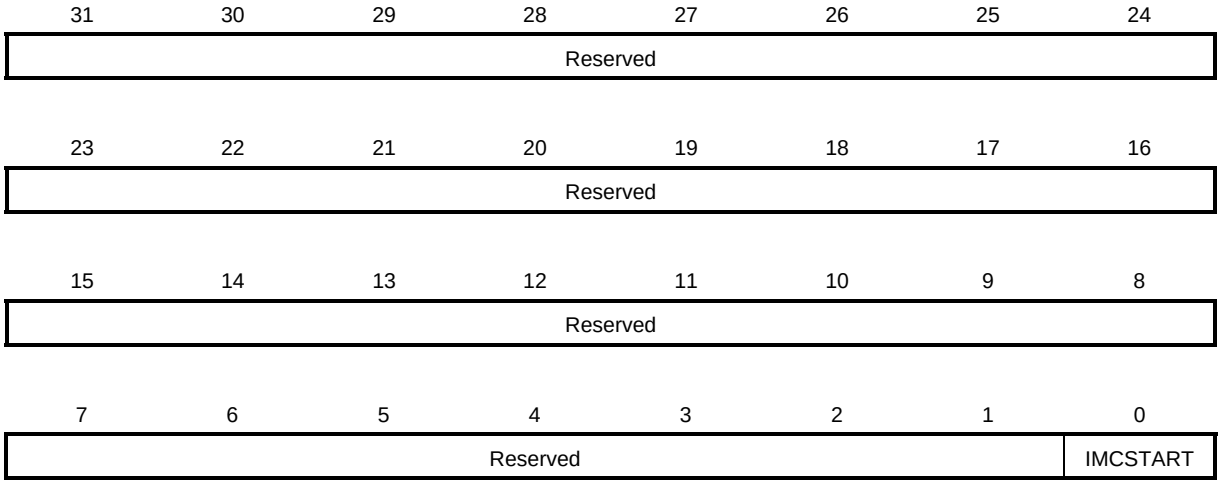


Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
UPDATE	R/W	0	0	Used to reserve register updates. 0: Does not update. 1: Update reserved.

An update end interrupt is issued when the register is updated. (The interrupt is issued immediately if the IMC has been started immediately while update reservation is set, or when the next frame begins if the IMC has been started in synchronization with the LCD controller.) The UPDATE bit is automatically cleared to 0 at the same time as update. Refer to **0 3.4.2 Register** update for details on the circuit structure.

2.2.3 Startup register

This register (IMC_START: 4026_0010H) is used to start the IMC in immediate startup mode (single startup). This is a V-sync register.

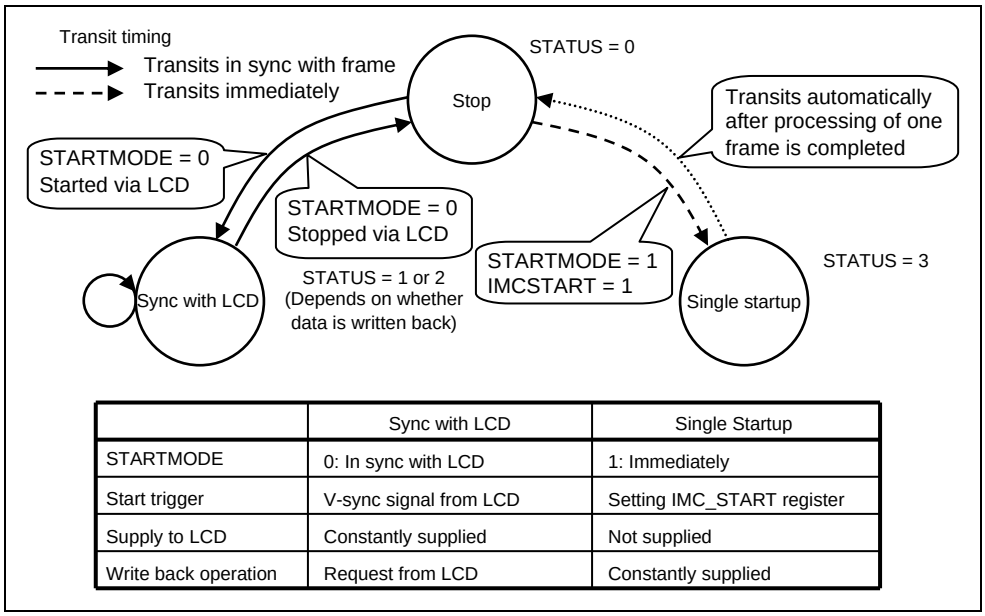


Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
IMCSTART	W	0	0	Starts the IMC in immediate startup mode (STARTMODE = 1). 1: Startup

When the STARTMODE bit of the control register (IMC_CONTROL) is set to 0 (LCD-synchronous operation), the setting of this register is ignored and the IMC is started in synchronization with the LCD operation. If this register is set to 1 while the STARTMODE bit is 1 (immediate startup), the IMC performs synthesis processing for one plane and stops automatically.

Writing to this register is ignored when the IMC cannot start, such as when the IMC is in the LCD-synchronous mode or being operating.

Figure 2-1. Status Transition

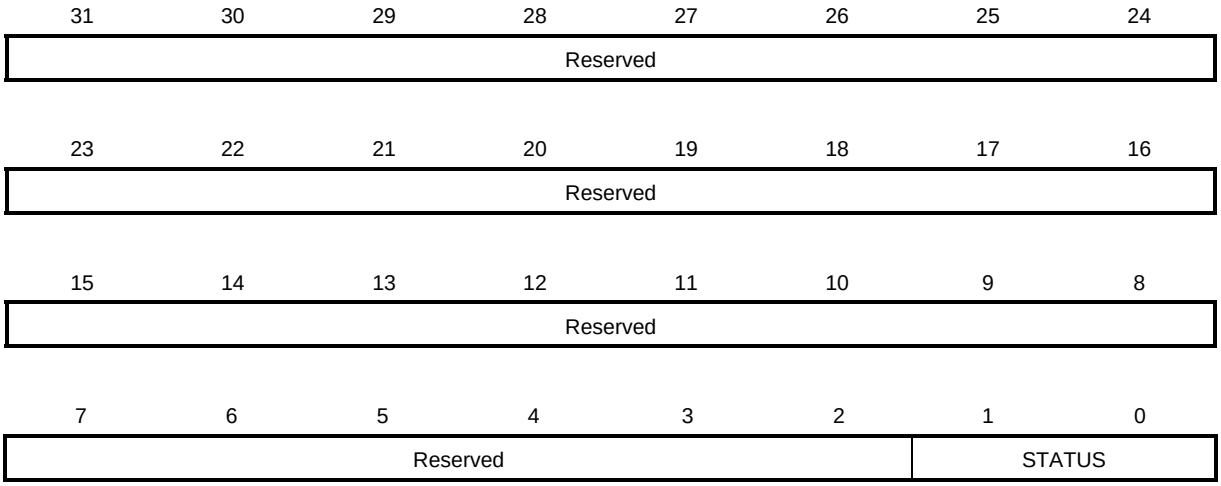


	Sync with LCD	Single Startup
STARTMODE	0: In sync with LCD	1: Immediately
Start trigger	V-sync signal from LCD	Setting IMC_START register
Supply to LCD	Constantly supplied	Not supplied
Write back operation	Request from LCD	Constantly supplied

2.2.4 Status register

This register (IMC_STATUS: 4026_0014H) indicates the IMC operating status. The IMC operating status can be checked by reading this register.

This is a V-sync register.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	0	Reserved. When these bits are read, 0 is returned for each bit.
STATUS	R	1:0	0	Indicates the IMC operating status. 00: Stopped 01: Supplying display data to the LCD controller (without WB). 10: Supplying display data to the LCD controller (with WB) 11: Operating in single startup mode (WB only).

2.2.5 CPU double buffer control register

This register (IMC_CPUBUFSEL: 4026_0018H) switches buffers P and Q when double buffer of layers 2A and 2B is controlled by the CPU. The setting of this register is applied to both layers 2A and 2B.

This is a V-sync register whose setting is reflected internally in synchronization with frame reception. It is not an update target register.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							BUFSEL

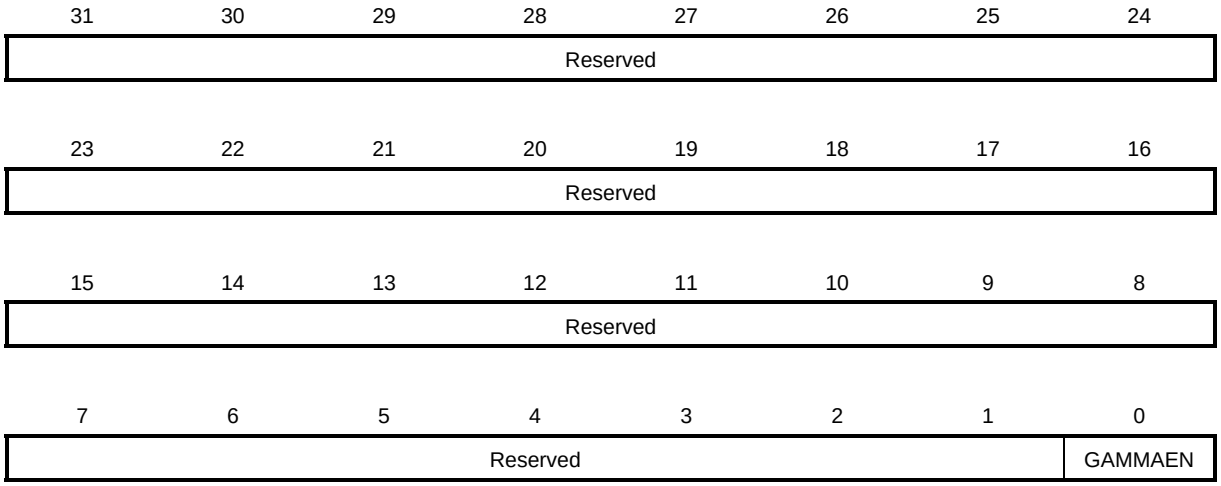
Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
BUFSEL	R/W	0	0	Selects buffer P or Q when double buffer of layers 2A and 2B is controlled by the CPU. 0: Buffer P 1: Buffer Q

This setting is ignored when double buffer of layers 2A and 2B is controlled in A/B-fixed mode.

2.2.6 Gamma correction control register

This register (IMC_GAMMA_EN: 4026_0020H) controls the gamma correction function. This is an immediately-reflected register, and changing the settings is prohibited while the IMC is operating.

For details on the gamma correction function, see **3.3 Gamma Correction Function**.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
GAMMAEN	R/W	0	0	Sets whether to enable gamma correction. 0: Disables gamma correction 1: Enables gamma correction

The gamma correction table values can be changed only when this register is set to 0.

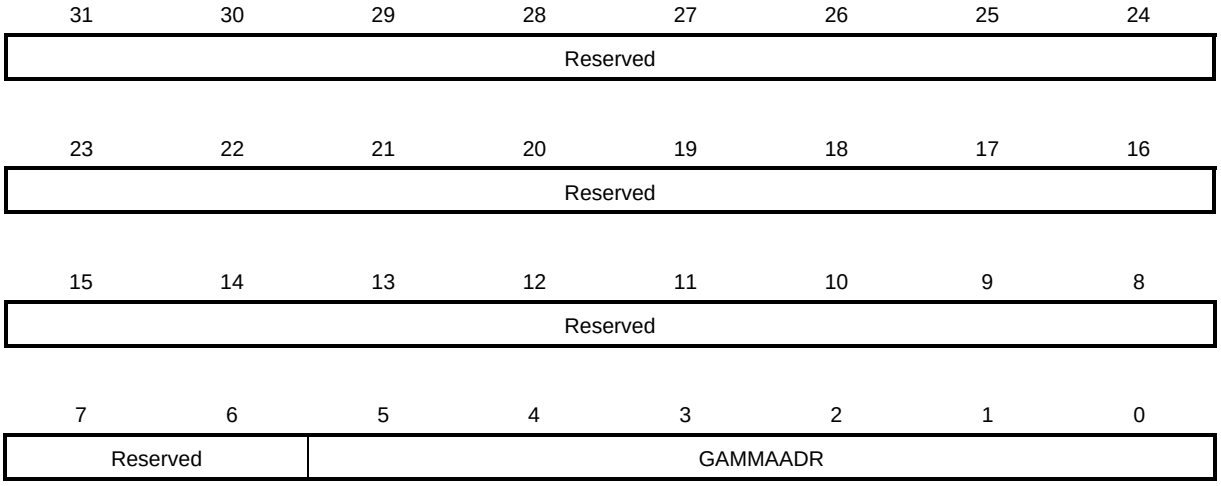
Before setting the gamma correction table values, set bit 11 (gamma correction CLK control) of the control register (IMC_CONTROL) to 0 (automatic control disabled, CLK constantly supplied).

2.2.7 Gamma correction table address register

This register (IMC_GAMMA_ADR: 4026_0024H) sets the gamma correction table address to be accessed for reading or writing.

This is an immediately-reflected register, and changing the settings is prohibited while the IMC is operating.

For details on the gamma correction function, see **3.3 Gamma Correction Function**.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:6	0	Reserved. When these bits are read, 0 is returned for each bit.
GAMMAADR	R/W	5:0	0	Sets the gamma correction table address to be accessed.

To accelerate writing to the gamma table, perform write to the IMC_GAMMA_DATA register; the values of this register are then incremented automatically.

Before setting the gamma correction table values, set bit 11 (gamma correction CLK control) of the control register (IMC_CONTROL) to 0 (automatic control disabled, CLK constantly supplied).

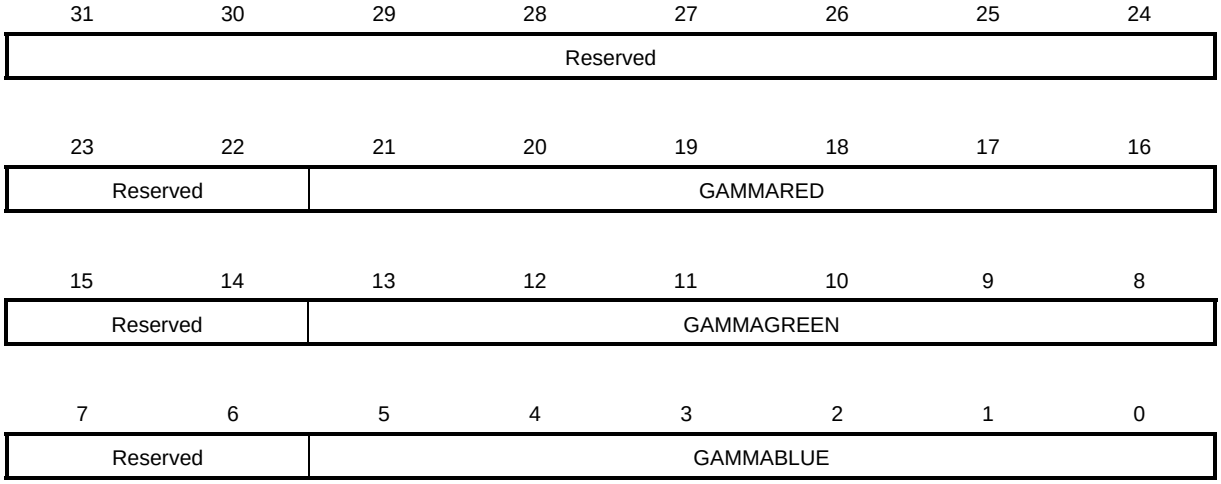
2.2.8 Gamma correction table data register

This register (IMC_GAMMA_DATA: 4026_0028H) is used to access the gamma correction table based on the address set with the GAMMAADR bit of the gamma correction table address register. The gamma correction table cannot be accessed when gamma correction is enabled. Setting this register is prohibited while gamma correction is enabled because the write operation is ignored and the read operation may read out invalid data.

This is an immediately-reflected register, and changing the settings is prohibited while the IMC is operating.

When this register is read, data is latched from the memory at the first read, and is read out via the APB bus at the second read. Therefore, be sure to read this register twice in succession and use the data acquired at the second read.

For details on the gamma correction function, see **3.3 Gamma Correction Function**.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:22	0	Reserved. When these bits are read, 0 is returned for each bit.
GAMMARED	R/W	21:16	0	Sets the correction value for the Red data at the address specified with GAMMAADR.
Reserved	R	15:14	0	Reserved. When these bits are read, 0 is returned for each bit.
GAMMAGREEN	R/W	13:8	0	Sets the correction value for the Green data at the address specified with GAMMAADR.
Reserved	R	7:6	0	Reserved. When these bits are read, 0 is returned for each bit.
GAMMABLUE	R/W	5:0	0	Sets the correction value for the Blue data at the address specified with GAMMAADR.

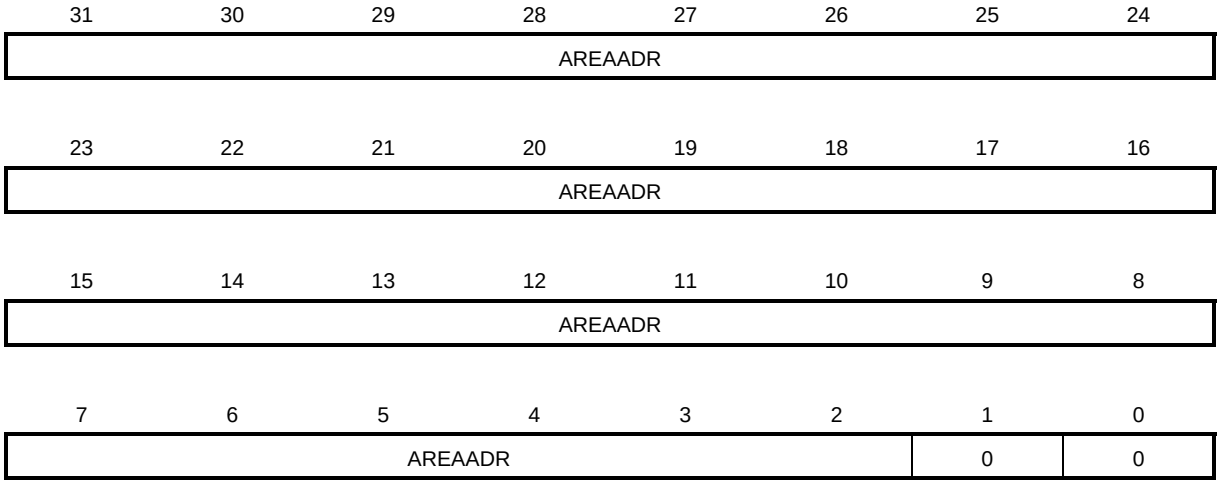
To accelerate writing to the gamma table, perform write to this register; the values of the IMC_GAMMA_ADR register are then incremented automatically. This setting does not affect the read operation.

Before setting the gamma correction table values, set bit 11 (gamma correction CLK control) of the control register (IMC_CONTROL) to 0 (automatic control disabled, CLK constantly supplied).

2.2.9 Display area address register

This register (IMC_WB_AREAADR: 4026_0040H) sets the start address of the frame buffer area for WB, when the IMC is operating in the immediate startup mode. This is an immediately-reflected register, so changing of settings during operation is prohibited.

When the IMC is operating in the LCD-synchronous mode, the values set in this register are ignored and the WB buffer area set by the LCD controller is used.



Name	R/W	Bit	After Reset	Function
AREAADR	R/W	31:0	0	Sets the first address of the frame buffer. (The lower 2 bits are fixed to 0.) For details, see **Figure 3-1. Frame Buffer Definition**.

2.2.10 Address addition value register

This register (IMC_WB_HOFFSET: 4026_0044H) sets the total byte count in the horizontal direction of the frame buffer area for WB, when the IMC is operating in the immediate startup mode. This is an immediately-reflected register, so changing of settings during operation is prohibited.

When the IMC is operating in the LCD-synchronous mode, the values set in this register are ignored and the WB buffer area horizontal size set by the LCD controller is used.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved			HOFFSET				

7	6	5	4	3	2	1	0
HOFFSET						0	0

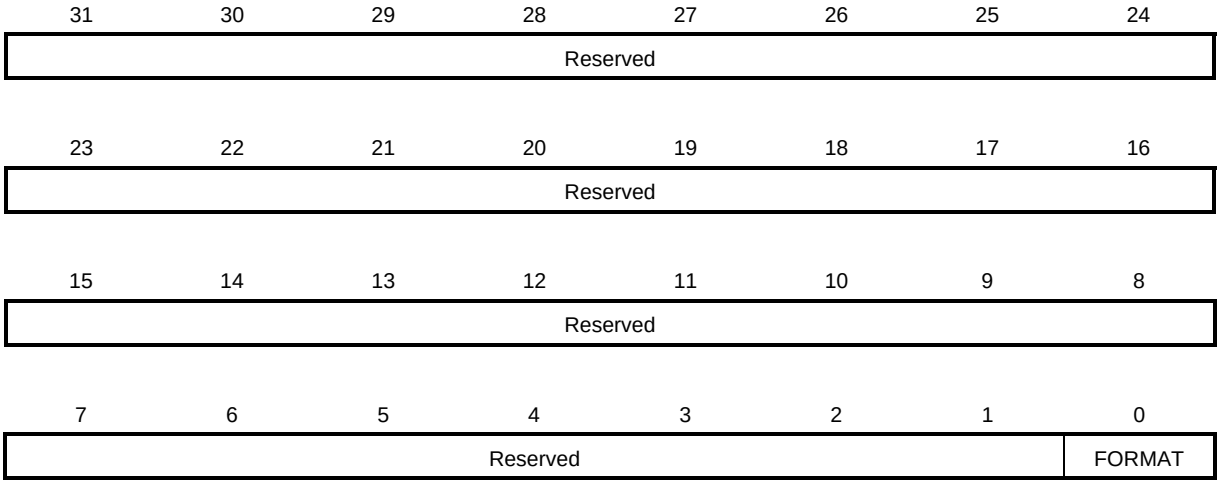
Name	R/W	Bit	After Reset	Function
Reserved	R	31:13	0	Reserved. When these bits are read, 0 is returned for each bit.
HOFFSET	R/W	12:0	0	Sets the total byte count in horizontal direction of the frame buffer area. (The lower 2 bits are fixed to 0.)

The address addition value which is required for storing valid pixel data varies depending on the horizontal pixel count set in the WB image size register and the value set in the format register. Observe the constraints on each image format and be sure not to set a value lower than the minimum value.

2.2.11 Format register

This register (IMC_WB_FORMAT: 4026_0048H) sets the format of data input to the frame buffer area for WB, when the IMC is operating in the immediate startup mode. This is an immediately-reflected register, so changing of settings during operation is prohibited.

When the IMC is operating in the LCD-synchronous mode, the values set in this register are ignored and the format of input data for WB set by the LCD controller is used.

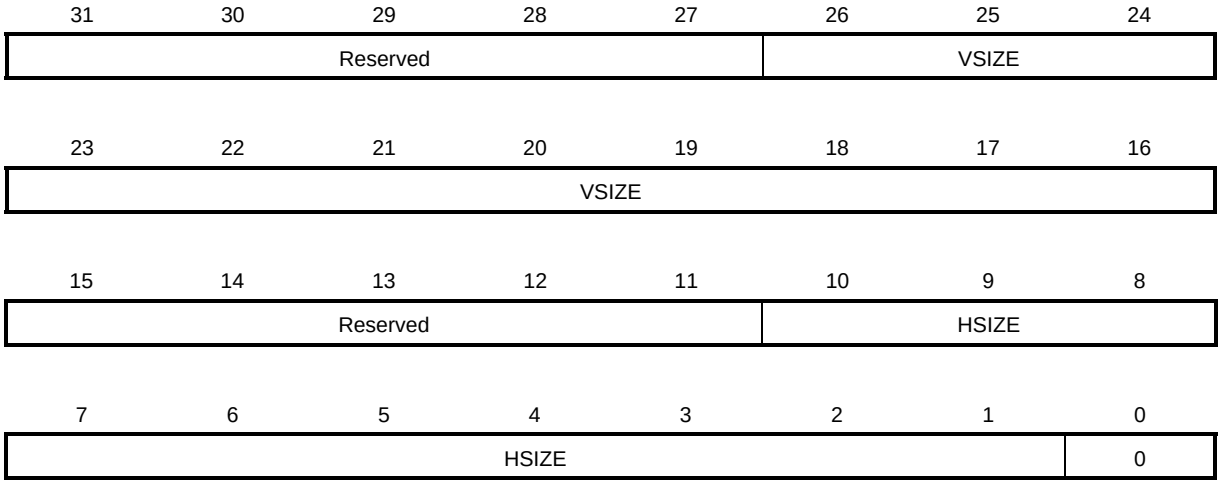


Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
FORMAT	R/W	0	0	Sets the input data format. For details, see **3.1.1 Supported image formats**. 0: RGB666 1: RGB565

2.2.12 WB image size register

This register (IMC_WB_SIZE: 4026_004CH) sets the size of WB images when the IMC is operating in the immediate startup mode. This is an immediately-reflected register, so changing of settings during operation is prohibited.

When the IMC is operating in the LCD-synchronous mode, the values set in this register are ignored and the display image size set by the LCD controller is used.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:27	0	Reserved. When these bits are read, 0 is returned for each bit.
VSIZE	R/W	26:16	0	Sets the vertical size of WB images (up to 2,046 lines, in line units)
Reserved	R	15:11	0	Reserved. When these bits are read, 0 is returned for each bit.
HSIZE	R/W	10:0	0	Sets the horizontal size of WB images (up to 2,046 pixels, in 2-pixel units, the lowest bit is fixed to 0)

2.2.13 Horizontal/vertical flip setting register

This register (IMC_MIRROR: 4026_0100H) is used to flip images output from the IMC (data after synthesis) horizontally or vertically.

Horizontal or vertical flip is performed after layers are overlaid, so care must be exercised when displaying layers including texts.

This is a V-sync register, so the setting takes effect at the beginning of the first frame after setting change.

31	30	29	28	27	26	25	24
Reserved							

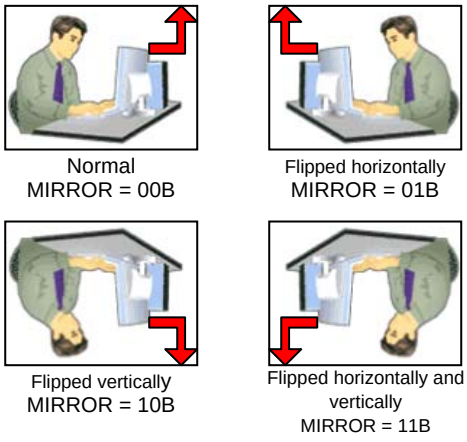
23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						MIRROR	

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	0	Reserved. When these bits are read, 0 is returned for each bit.
MIRROR	R/W	1:0	0	Sets flipping of images. 00: No flip 01: Horizontal flip 10: Vertical flip 11: Horizontal and vertical flip

Figure 2-2. Flipping of Images



2.2.14 Y gain offset register

This register (IMC_YGAINOFFSET: 4026_0104H) is used to adjust the gain for Y (luminance) by multiplying by 0 to 255/128 and adjusts the offset in the range of −128 to 127, for YUV format images to be input.

The YUV format can be specified for layers 2A and 2B, and the same setting is applied to both layers.

This is an immediately-reflected register, so changing of settings during operation is prohibited.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
YOFFSET							

7	6	5	4	3	2	1	0
YGAIN							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:16	0	Reserved. When these bits are read, 0 is returned for each bit.
YOFFSET	R/W	15:8	00H	Sets the offset for the Y value by using signed 8-bit data. (2's complement) (−128 to 127)
YGAIN	R/W	7:0	80H	Sets the offset for the Y value. Values from 0 to 255 can be set, and the gain is set value/128.

$$Yout = \left(\frac{YGAIN}{128} * Yin \right) + YOFFSET$$

Calculation of desired value: Multiply Yin by YGAIN divided by 128, rounding to one decimal place, and then add YOFFSET to calculate the approximate value (Yout) in the range of 0 to 255.

Caution When YGAIN = 0, the value set to the YOFFSET bit is used as unsigned 8-bit data (0 to 255), and Yout is assumed to be equal to YOFFSET.

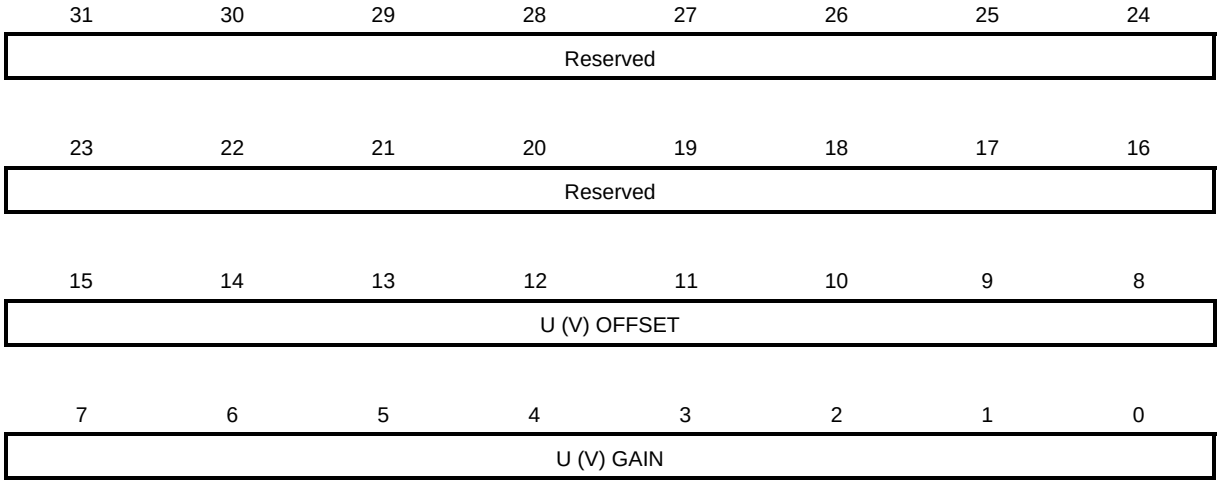
2.2.15 U (V) gain offset registers

These registers (IMC_UGAINOFFSET: 4026_0108H and IMC_VGAINOFFSET: 4026_010CH) are used to adjust the gain for U (color difference in blue) and V (color difference in red) by multiplying by 0 to 255/128 and the offset in the range of −128 to 127, for YUV format images to be input.

The YUV format can be specified for layers 2A and 2B, and the same setting is applied to both layers.

Since the U and V components are represented in offset binary coding with 80H positioned as the center, 80H is subtracted, converted into values ranging from −128 to 127, the gain is multiplied, and then the offset value and 80H are added.

These are immediately-reflected registers, so changing of settings during operation is prohibited.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:16	0	Reserved. When these bits are read, 0 is returned for each bit.
UOFFSET (VOFFSET)	R/W	15:8	00H	Sets the offset for the U (V) value by using signed 8-bit data. (−128 to 127)
UGAIN (VGAIN)	R/W	7:0	80H	Sets the offset for the U (V) value. Values from 0 to 255 can be set, and the gain is set value/128.

$$Uout = \left(\frac{UGAIN}{128} * (Uin - 80H) \right) + UOFFSET + 80H$$

$$Vout = \left(\frac{VGAIN}{128} * (Vin - 80H) \right) + VOFFSET + 80H$$

Calculation of desired value: Multiply (Uin − 80H) oy (Yin − 80H) by UGAIN or VGAIN divided by 128, rounding to one decimal place, and then add 80H and UOFFSET or VOFFSET to calculate the approximate value in the range of 0 to 255.

Cautions 1. When UGAIN/VGAIN = 0, the value set to the UOFFSET/VOFFSET bit is used as unsigned 8-bit data (0 to 255) and Uout is assumed to be equal to UOFFSET (Vout = VOFFSET).

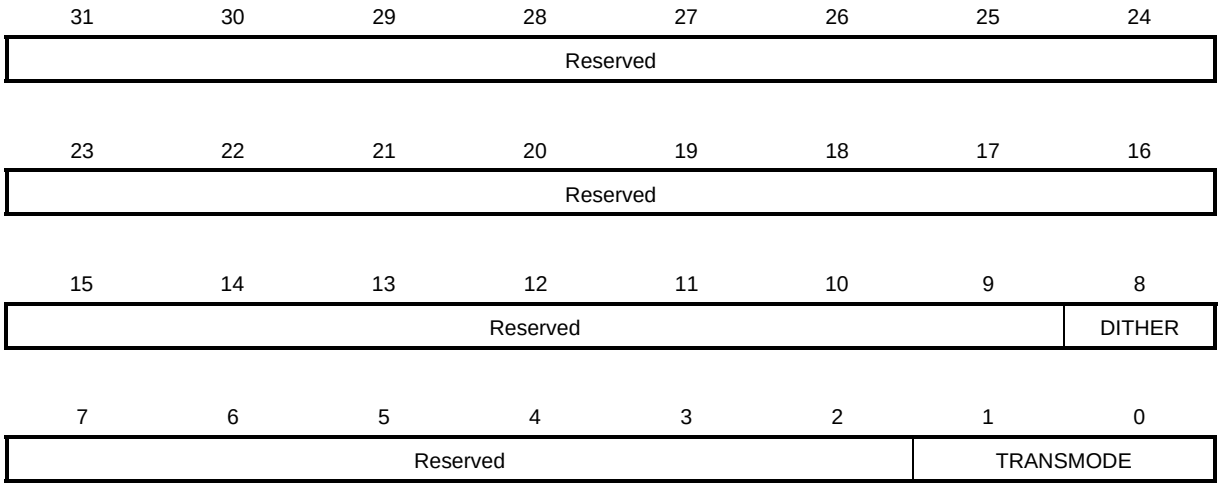
2. During multiplication, the fraction is dropped by adding 0.5. In the case of negative values, –0.5 is rounded up to 0.

2.2.16 YUV2RGB conversion mode register

This register (IMC_YUV2RGB: 4026_0110H) selects a calculation coefficient from ITU-R BT.601-compliant, ITU-R BT.709-compliant, custom coefficient (with or without Y value subtracted by 16) for converting YUV format input data into RGB format data.

The data format after conversion is RGB888, each data consists of 8 bits, and data is further converted into RGB666, which is to be used for overlay processing in the IMC. This register also sets whether to perform dithering during conversion.

This is an immediately-reflected register, so changing of settings during operation is prohibited.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:9	0	Reserved. When these bits are read, 0 is returned for each bit.
DITHER	R/W	8	0	Enables dithering. For details, see **3.1.5 Dithering**. 0: Does not perform dithering (rounding on or off). 1: Performs dithering.
Reserved	R	7:2	0	Reserved. When these bits are read, 0 is returned for each bit.
TRANS MODE	R/W	1:0	0	Selects the coefficient for YUV-to-RGB conversion. 00: ITU-R BT.601-compliant 01: ITU-R BT.709-compliant 10: Custom coefficient (Y value is subtracted by 16) 11: Custom coefficient (Y value is used as is)

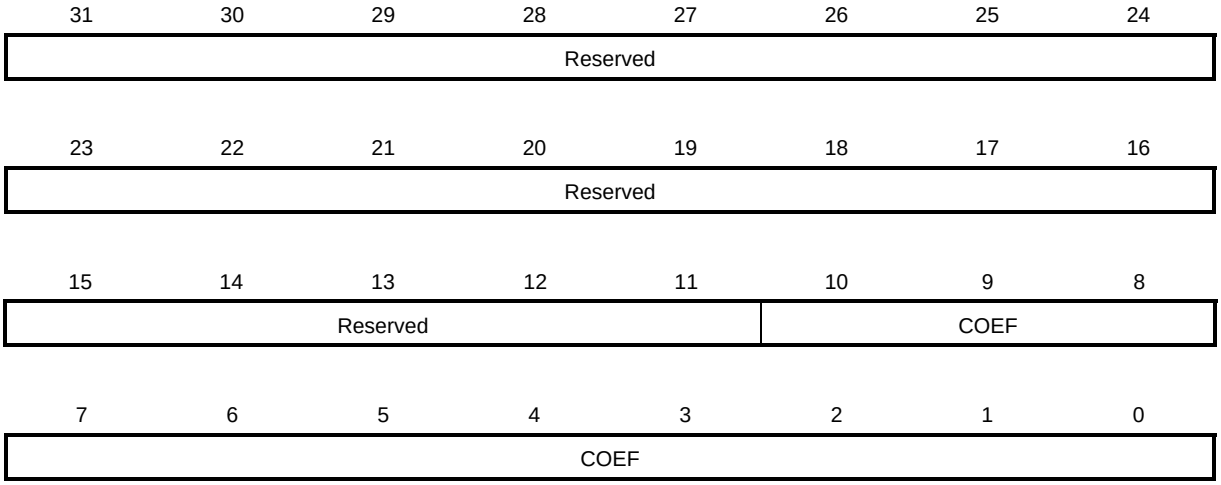
For details on conversion methods according to the TRANSMODE bit settings, see **2.2.17 Custom coefficient registers**.

2.2.17 Custom coefficient registers

(IMC_COEF_R0: 4026_0114H)	(IMC_COEF_G0: 4026_0124H)	(IMC_COEF_B0: 4026_0134H)
(IMC_COEF_R1: 4026_0118H)	(IMC_COEF_G1: 4026_0128H)	(IMC_COEF_B1: 4026_0138H)
(IMC_COEF_R2: 4026_011CH)	(IMC_COEF_G2: 4026_012CH)	(IMC_COEF_B2: 4026_013CH)
(IMC_COEF_R3: 4026_0120H)	(IMC_COEF_G3: 4026_0130H)	(IMC_COEF_B3: 4026_0140H)

These registers set the coefficient for YUV-to-RGB conversion. The set values are used for matrix calculation when the TRANSMODE bit is set to 2 or 3. The values set in these registers are ignored when the TRANSMODE bit is set to 0 or 1.

These are immediately-reflected register, so changing of settings during operation is prohibited.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:11	0	Reserved. When these bits are read, 0 is returned for each bit.
COEF	R/W	10:0	0	Signed 11-bit data (2's complement) (–1024 to 1023)

YUV-to RGB conversion is calculated with the 4 × 4 matrix calculation.

$$\begin{pmatrix} R \\ G \\ B \end{pmatrix} = \begin{pmatrix} R0 & R1 & R2 & R3 \\ G0 & G1 & G2 & G3 \\ B0 & B1 & B2 & B3 \end{pmatrix} * \begin{pmatrix} Y-16 \\ U-128 \\ V-128 \\ 1 \end{pmatrix} * \frac{1}{256}$$

When the TRANSMODE bit of the IMC_YUV2RGB register is set to 3, 16 is not subtracted from the Y value.

$$\begin{pmatrix} R \\ G \\ B \end{pmatrix} = \begin{pmatrix} R0 & R1 & R2 & R3 \\ G0 & G1 & G2 & G3 \\ B0 & B1 & B2 & B3 \end{pmatrix} * \begin{pmatrix} Y \\ U-128 \\ V-128 \\ 1 \end{pmatrix} * \frac{1}{256}$$

As a result, the RGB values are calculated as follows.

$$R = (R0*(Y-16) + R1*(U-128) + R2*(V-128) + R3)/256$$
$$G = (G0*(Y-16) + G1*(U-128) + G2*(V-128) + G3)/256$$ …16 is subtracted from Y value
$$B = (B0*(Y-16) + B1*(U-128) + B2*(V-128) + B3)/256$$
$$R = (R0*Y + R1*(U-128) + R2*(V-128) + R3)/256$$
$$G = (G0*Y + G1*(U-128) + G2*(V-128) + G3)/256$$ …Y value is used as is
$$B = (B0*Y + B1*(U-128) + B2*(V-128) + B3)/256$$

All twelve coefficients can be set by using signed 11-bit values (–1024 to 1023).

When the TRANSMODE of the IMC_YUV2RGB register is set to 0 (ITU-R BT.601-compliant) or 1 (ITU-R BT.709-compliant), each coefficient is automatically replaced by the following coefficients.

• ITU-BT601-compliant (TRANS MODE = 0)

$$\begin{pmatrix} R0 & R1 & R2 & R3 \\ G0 & G1 & G2 & G3 \\ B0 & B1 & B2 & B3 \end{pmatrix} = \begin{pmatrix} 298 & 0 & 409 & 0 \\ 298 & -100 & -208 & 0 \\ 298 & 517 & 0 & 0 \end{pmatrix}$$

Conversion is performed based on the above coefficient in the mode in which the Y value is subtracted by 16.

As a result, the RGB values are calculated as follows.

$$R = (298*(Y-16) + 0*U + 409*V + 0)/256$$
$$G = (298*(Y-16) - 100*U - 208*V + 0)/256$$
$$B = (298*(Y-16) + 517*U + 0*V + 0)/256$$

• ITU-BT709-compliant (TRANS MODE = 1)

$$\begin{pmatrix} R0 & R1 & R2 & R3 \\ G0 & G1 & G2 & G3 \\ B0 & B1 & B2 & B3 \end{pmatrix} = \begin{pmatrix} 298 & 0 & 459 & 0 \\ 298 & -55 & -137 & 0 \\ 298 & 541 & 0 & 0 \end{pmatrix}$$

Conversion is performed based on the above coefficient in the mode in which the Y value is subtracted by 16.

As a result, the RGB values are calculated as follows.

$$R = (298*(Y-16) + 0*U + 459*V + 0)/256$$
$$G = (298*(Y-16) - 55*U - 137*V + 0)/256$$
$$B = (298*(Y-16) + 541*U + 0*V + 0)/256$$

Since the U and V components are represented in offset binary coding in the circuit, with 80H positioned as the center, 128 is subtracted before RGB calculation and substituted into the above formulas. The RGB value after conversion is obtained by rounding the resultant to one decimal place and being clipped in the range of 0 to 255.

2.2.18 Layer control registers

Layer 0 control register (IMC_L0_CONTROL: 4026_0200H)
Layer 1A control register (IMC_L1A_CONTROL: 4026_0300H)
Layer 1B control register (IMC_L1B_CONTROL: 4026_0400H)
Layer 1C control register (IMC_L1C_CONTROL: 4026_0500H)
Layer 2A control register (IMC_L2A_CONTROL: 4026_0600H)
Layer 2B control register (IMC_L2B_CONTROL: 4026_0700H)

These registers set turning on/off of the overlay function for individual layer (six layers, except for the background). These are update target registers.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							LAYERON

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
LAYERON	R/W	0	0	Sets whether to enable synthesis of the target layers. 0: Disables layer 1: Enables layer

2.2.19 Layer format registers

Layer 0 format register (IMC_L0_FORMAT: 4026_0204H)
Layer 1x format register (IMC_L1X_FORMAT: 4026_0304H)
Layer 2A format register (IMC_L2A_FORMAT: 4026_0604H)
Layer 2B format register (IMC_L2B_FORMAT: 4026_0704H)
Layer BG format register (IMC_BG_FORMAT: 4026_0804H)

These registers set the format of data to be stored in each layer. These are update target registers. The supported format varies in each layer. The available formats are listed in the following tables.

Layer 0 and layer 1x format registers

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
FORM	R/W	0	0	Specifies the format of data to be stored in the target layer. 0: RGB666 1: RGB565

Layer 2A and layer 2B format registers

Name	R/W	Bit	After Reset	Function
Reserved	R	31:3	0	Reserved. When these bits are read, 0 is returned for each bit.
FORM	R/W	2:0	0	Specifies the format of data to be stored in the target layer. 000: RGB666 001: RGB565 010: YUV422 Interleave 011: YUV422 Semi-Planar 100: YUV422 Planar 101: YUV420 Semi-Planar 110 or 111: YUV420 Planar

Layer BG format register

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	0	Reserved. When these bits are read, 0 is returned for each bit.
FORM	R/W	1:0	0	Specifies the format of data to be stored in the target layer. 00: RGB666 01: RGB565 10: Fixed to black (ALL0) 11: Fixed background color (set by LCD_BACKCOLOR register)

2.2.20 Transparent color control registers

These registers (IMC_L0_KEYENABLE: 4026_0210H, IMC_L1A_KEYENABLE: 4026_0310H, IMC_L1B_ KEYENABLE: 4026_0410H and IMC_L1C_ KEYENABLE: 4026_0510H)) set turning on/off of the transparent color for individual layer (layer 0 and layers 1A to 1C). These are update target registers.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

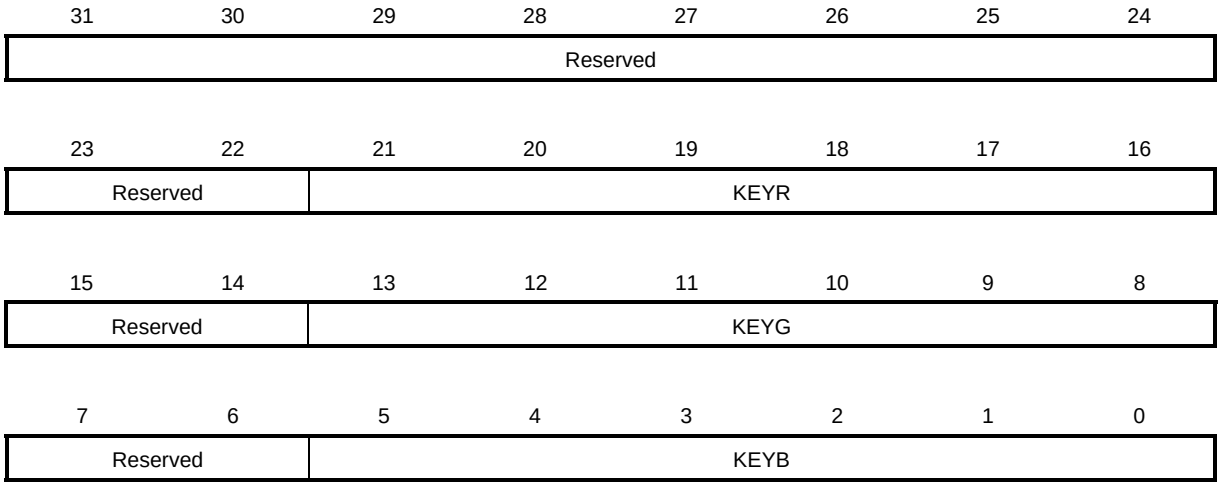
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							KEYEN

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
KEYEN	R/W	0	0	Sets turning on/off the transparent color for the target layer. 0: Transparent color function OFF 1: Transparent color function ON

2.2.21 Layer transparent color registers

These registers (IMC_L0_KEYCOLOR: 4026_0214H and IMC_L1X_KEYCOLOR: 4026_0314H) specify the key colors used for implementing the transparent color function for the target layer. These are immediately-reflected registers. The set values are commonly applied to layers 1A, 1B and 1C.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:22	0	Reserved. When these bits are read, 0 is returned for each bit.
KEYR	R/W	21:16	0	Specifies red data component for the transparent color.
Reserved	R	15:14	0	Reserved. When these bits are read, 0 is returned for each bit.
KEYG	R/W	13:8	0	Specifies green data component for the transparent color.
Reserved	R	7:6	0	Reserved. When these bits are read, 0 is returned for each bit.
KEYB	R/W	5:0	0	Specifies blue data component for the transparent color.

Caution When data in the target layer is of the RGB666 format, the condition for transparency processing is a match of all 18 bits. In the RGB565 format, the most significant bits of components of R and B are extended to the least significant bits, and if the values match the value of 6 bits in either of these registers, transparency processing is performed.

2.2.22 Alpha registers

These registers (IMC_L0_ALPHA: 4026_0218H, IMC_L1A_ALPHA: 4026_0318H, IMC_L1B_ALPHA: 4026_0418H and IMC_L1C_ALPHA: 4026_0518H) set items related to alpha blending for synthesis of the target layers.

These are update target registers.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							REVERSE

7	6	5	4	3	2	1	0
Reserved				ALPHA			

Name	R/W	Bit	After Reset	Function
Reserved	R	31:9	0	Reserved. When these bits are read, 0 is returned for each bit.
REVERSE	R/W	8	0	Reverse the ALPHA setting. Reads 63-ALPHA as newly set ALPHA.
Reserved	R	7:6	0	Reserved. When these bits are read, 0 is returned for each bit.
ALPHA	R/W	5:0	0	Sets the transparency. Setting range: 0 to 63 (0 = transparent, 63 = opaque) **Remark** 0 = opaque and 63 = transparent when REVERSE = 1.

Transparency of 0 to 100% is achieved by set values ranging from 0 to 63.

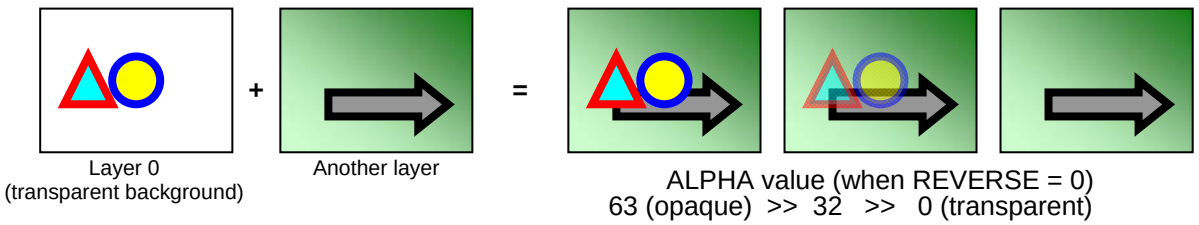
When calculating the desired value, PixOut after synthesis is as follows, where pixel data of the layer subject to transparency processing = PixA, and background = PixB.

- When ALPHA = 0 to 62

  PixOut = {ALPHA × PixA + (64 – ALPHA) × PixB} /64 (pixels = 6 bits, with rounding up or down)

- When ALPHA = 63

  PixOut = PixA. The element of PixB is not reflected in the overlaid result.



2.2.23 Resize registers

Layer 0 resize register (IMC_L0_RESIZE: 4026_0220H)
Layer 1x resize register (IMC_L1X_RESIZE: 4026_0320H)
Layer 2A resize register (IMC_L2A_RESIZE: 4026_0620H)
Layer 2B resize register (IMC_L2B_RESIZE: 4026_0720H)
Layer BG resize register (IMC_BG_RESIZE: 4026_0820H)

These registers enable resizing of overlaid layers.

Only resizing to double the simple copy is supported. Image data read from a frame buffer is copied to 2 pixels in horizontal and vertical directions and used as the output image. The display area is not doubled during synthesis, but data stored in the frame buffer is just enlarged to fit into the specified displayed area.

These are update target registers.

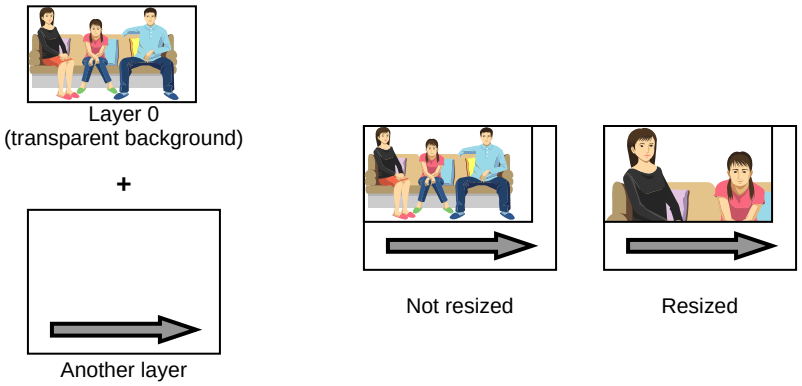
31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							RESIZEEN

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
RESIZEEN	R/W	0	0	Sets whether to enable the resize function. 0: Does not resize images. 1: Resize images.



2.2.24 Address addition value registers

Layer 0 address addition value register (IMC_L0_OFFSET: 4026_0230H)
Layer 1x address addition value register (IMC_L1X_OFFSET: 4026_0330H)
Layer 2A address addition value register (IMC_L2A_OFFSET: 4026_0630H)
Layer 2B address addition value register (IMC_L2B_OFFSET: 4026_0730H)
Layer BG address addition value register (IMC_BG_OFFSET: 4026_0830H)

These registers set the horizontal size of the frame buffer of the target layers.

Because the number of settable pixels varies in each layer, the bit width of address addition values also varies according to the layer. These are update target registers.

Layer 0 address addition value register

Name	R/W	Bit	After Reset	Function
Reserved	R	31:10	0	Reserved. When these bits are read, 0 is returned for each bit.
HOFFSET	R/W	9:0	0	Sets the address addition value for the target layer. (The lower 2 bits are fixed to 0.)

Layer 1x address addition value register

Name	R/W	Bit	After Reset	Function
Reserved	R	31:13	0	Reserved. When these bits are read, 0 is returned for each bit.
HOFFSET	R/W	12:0	0	Sets the address addition value for the target layer. (The lower 2 bits are fixed to 0.)

Layer 2A/2B/BG address addition value registers

Name	R/W	Bit	After Reset	Function
Reserved	R	31:13	0	Reserved. When these bits are read, 0 is returned for each bit.
HOFFSET	R/W	12:0	0	Sets the address addition value for the target layer. (The lower 2 bits are fixed to 0.)

For the definition of frame buffers, see **Figure 3-1. Frame Buffer Definition**.

2.2.25 Buffer start address registers

Layer 0 start address register	(IMC_L0_FRAMEADR: 4026_0234H)
Layer 1A start address register	(IMC_L1A_FRAMEADR: 4026_0334H)
Layer 1B start address register	(IMC_L1B_FRAMEADR: 4026_0434H)
Layer 1C start address register	(IMC_L1C_FRAMEADR: 4026_0534H)
Layer 2A start address register (YP)	(IMC_L2A_FRAMEADR_YP: 4026_0634H)
Layer 2A start address register (UP)	(IMC_L2A_FRAMEADR_UP: 4026_0638H)
Layer 2A start address register (VP)	(IMC_L2A_FRAMEADR_VP: 4026_063CH)
Layer 2A start address register (YQ)	(IMC_L2A_FRAMEADR_YQ: 4026_0640H)
Layer 2A start address register (UQ)	(IMC_L2A_FRAMEADR_UQ: 4026_0644H)
Layer 2A start address register (VQ)	(IMC_L2A_FRAMEADR_VQ: 4026_0648H)
Layer 2B start address register (YP)	(IMC_L2B_FRAMEADR_YP: 4026_0734H)
Layer 2B start address register (UP)	(IMC_L2B_FRAMEADR_UP: 4026_0738H)
Layer 2B start address register (VP)	(IMC_L2B_FRAMEADR_VP: 4026_073CH)
Layer 2B start address register (YQ)	(IMC_L2B_FRAMEADR_YQ: 4026_0740H)
Layer 2B start address register (UQ)	(IMC_L2B_FRAMEADR_UQ: 4026_0744H)
Layer 2B start address register (VQ)	(IMC_L2B_FRAMEADR_VQ: 4026_0748H)
Layer BG start address register	(IMC_BG_FRAMEADR: 4026_0834H)

These registers set the start address of the frame buffer of the target layers.

These are update target registers.

31	30	29	28	27	26	25	24
FRAMEADR							

23	22	21	20	19	18	17	16
FRAMEADR							

15	14	13	12	11	10	9	8
FRAMEADR							

7	6	5	4	3	2	1	0
FRAMEADR						0	0

Name	R/W	Bit	After Reset	Function
FRAMEADR	R/W	31:0	0	Sets the start address of the frame buffer of the target layer. (The lower 2 bits are fixed to 0.)

For the definition of frame buffers, see **Figure 3-1. Frame Buffer Definition**.

The start address register used for layer 2 varies depending on the image format. For details, see **Table 3-3. Formats and Start Address Setting Registers**.

2.2.26 Layer display position registers

Layer 0 display position register (IMC_L0_POSITION: 4026_0250H)
Layer 1A display position register (IMC_L1A_POSITION: 4026_0350H)
Layer 1B display position register (IMC_L1B_POSITION: 4026_0450H)
Layer 1C display position register (IMC_L1C_POSITION: 4026_0550H)
Layer 2A display position register (IMC_L2A_POSITION: 4026_0650H)
Layer 2B display position register (IMC_L2B_POSITION: 4026_0750H)

These registers set the overlay position when overlaying the target layers in pixel units.
These are update target registers

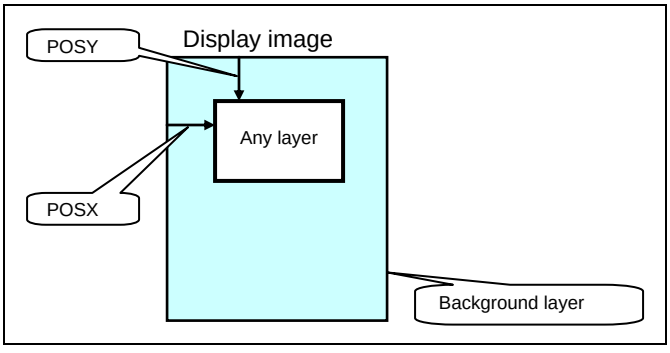
31	30	29	28	27	26	25	24
Reserved					POSY		

23	22	21	20	19	18	17	16
POSY							

15	14	13	12	11	10	9	8
Reserved					POSX		

7	6	5	4	3	2	1	0
POSX							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:27	0	Reserved. When these bits are read, 0 is returned for each bit.
POSY	R/W	26:16	0	Sets the Y coordinate at which layer display begins. (0 to 2,046 in pixel units)
Reserved	R	15:11	0	Reserved. When these bits are read, 0 is returned for each bit.
POSX	R/W	10:0	0	Sets the X coordinate at which layer display begins (0 to 2,046 in pixel units)



2.2.27 Layer display size registers

Layer 0 display size register (IMC_L0_SIZE: 4026_0254H)
Layer 1A display size register (IMC_L1A_SIZE: 4026_0354H)
Layer 1B display size register (IMC_L1B_SIZE: 4026_0454H)
Layer 1C display size register (IMC_L1C_SIZE: 4026_0554H)
Layer 2A display size register (IMC_L2A_SIZE: 4026_0654H)
Layer 2B display size register (IMC_L2B_SIZE: 4026_0754H)

These registers set the size of the overlaid layers, in pixel units.

Note that the size that can be displayed in each layer varies. These are update target registers.

Bits 31 to 24 and 15 to 8 are reserved. Writing any value other than 0 is prohibited. When these values are read, 0 is returned for each bit.

Layer 0 display size register

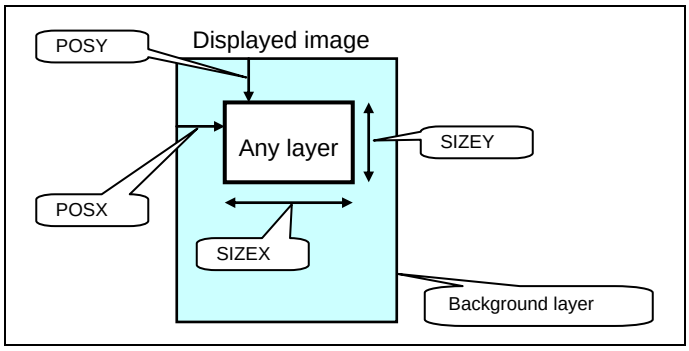
Name	R/W	Bit	After Reset	Function
SIZEY	R/W	23:16	0	Sets the vertical display size of the target layer. (0 to 255 in pixel units)
SIZEX	R/W	7:0	0	Sets the horizontal display size of the target layer. (0 to 255 in pixel units)

Layer 1x display size register

Name	R/W	Bit	After Reset	Function
SIZEY	R/W	26:16	0	Sets the vertical display size of the target layer. (0 to 2,046 in pixel units)
SIZEX	R/W	10:0	0	Sets the horizontal display size of the target layer. (0 to 2,046 in pixel units)

Layer 2x display size register

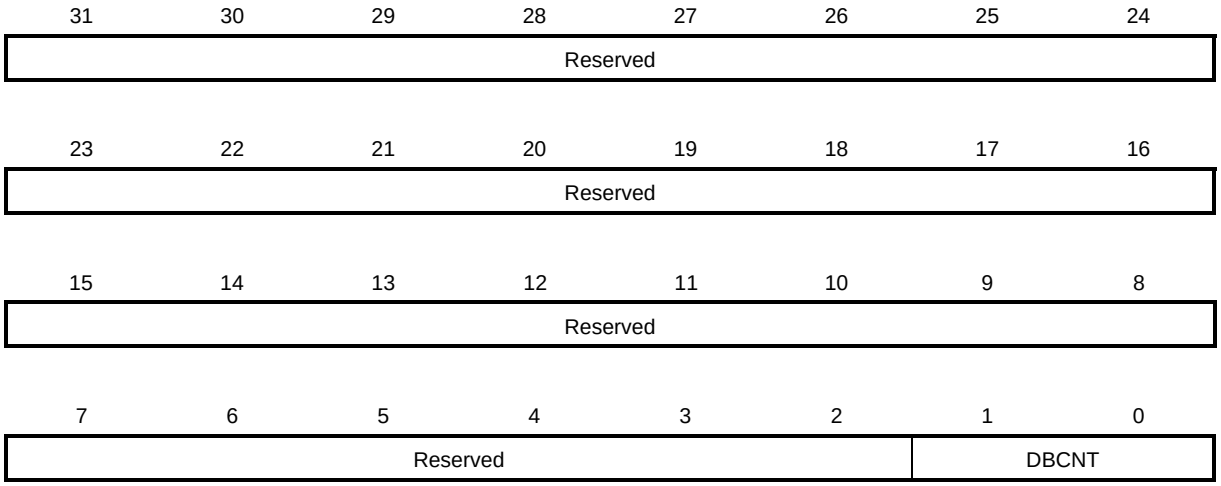
Name	R/W	Bit	After Reset	Function
SIZEY	R/W	26:16	0	Sets the vertical display size of the target layer. (0 to 2,046 in pixel units)
SIZEX	R/W	10:0	0	Sets the horizontal display size of the target layer. (0 to 2,046 in pixel units)



2.2.28 Layer 2 double buffer control registers

These registers (IMC_L2A_BUFSEL: 4026_0608H and IMC_L2B_BUFSEL: 4026_0708H) switch the P and Q planes in layers 2A and 2B.

These are update target registers.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	0	Reserved. When these bits are read, 0 is returned for each bit.
DBCNT	R/W	1:0	0	Selects how to control double buffers. 00: Fixed to plane P. 01: Fixed to plane Q. 10: Control via CPU (follows the IMC_CPUBUFSEL register settings) 11: Setting prohibited.

2.2.29 Layer 2 byte lane registers

These registers (IMC_L2A_BYTELANE: 4026_060CH and IMC_L2B_BYTELANE: 4026_070CH) switch byte sequence in data of 32 bits (word) when reading data of layers 2A and 2B from the frame buffer. These are immediately-reflected registers.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Y_BYTELANE							

7	6	5	4	3	2	1	0
UV_BYTELANE							

(1/2)

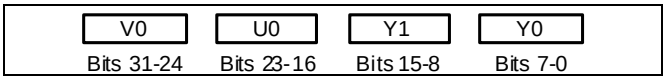
Name	R/W	Bit	After Reset	Function
Reserved	R	31:16	0	Reserved. When these bits are read, 0 is returned for each bit.
Y_BYTE LANE	R/W	15:8	E4H	• In YUV Interleave mode Y_BYTELANE Bits / Set Value 15:14 Bytes to which V0 is stored (0 to 3) 13:12 Bytes to which U0 is stored (0 to 3) 11:10 Bytes to which Y1 is stored (0 to 3) 9:8 Bytes to which Y0 is stored (0 to 3) • In YUV Semi-Planar/ Planar modes Y_BYTELANE Bits / Set Value 15:14 Bytes to which Y3 is stored (0 to 3) 13:12 Bytes to which Y2 is stored (0 to 3) 11:10 Bytes to which Y1 is stored (0 to 3) 9:8 Bytes to which Y0 is stored (0 to 3) • In other modes The set values are ignored.

(2/2)

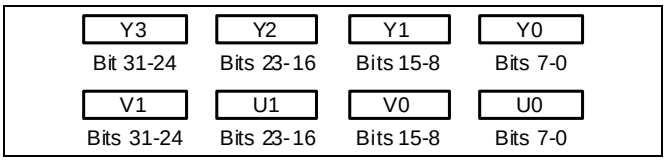
<table>
<tr><th>Name</th><th>R/W</th><th>Bit</th><th>After Reset</th><th>Function</th></tr>
<tr><td>UV_BYTE
LANE</td><td>R/W</td><td>7:0</td><td>E4H</td><td>• In YUV Semi-Planar mode
<table>
<tr><th>UV_BYTELANE Bits</th><th>Set Value</th></tr>
<tr><td>7:6</td><td>Bytes to which V1 is stored (0 to 3)</td></tr>
<tr><td>5:4</td><td>Bytes to which U1 is stored (0 to 3)</td></tr>
<tr><td>3:2</td><td>Bytes to which V0 is stored (0 to 3)</td></tr>
<tr><td>1:0</td><td>Bytes to which U0 is stored (0 to 3)</td></tr>
</table>
• In YUV Planar mode
<table>
<tr><th>UV_BYTELANE Bits</th><th>Set Value</th></tr>
<tr><td>7:6</td><td>Bytes to which V3/V3 is stored (0 to 3)</td></tr>
<tr><td>5:4</td><td>Bytes to which U2/V2 is stored (0 to 3)</td></tr>
<tr><td>3:2</td><td>Bytes to which U1/V1 is stored (0 to 3)</td></tr>
<tr><td>1:0</td><td>Bytes to which U0/V0 is stored (0 to 3)</td></tr>
</table>
• In other modes
The set values are ignored.</td></tr>
</table>

When the YUV format is set for layers 2A and 2B, the IMC changes the byte sequence when data is read from the memory, according to the BYTELANE set value. Set the BYTELANE so that the YUV data is reordered as expected by the IMC.

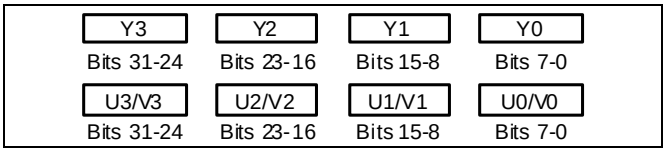
With YUV Interleave, the IMC expects the following byte sequence.



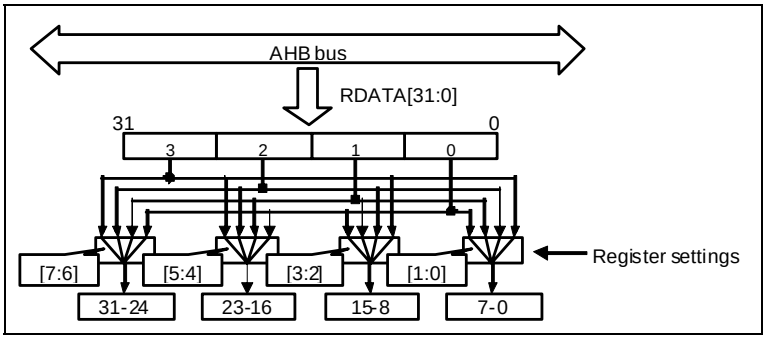
With YUV Semi-Planar, the IMC expects the following byte sequence.



With YUV Planar, the IMC expects the following byte sequence.



The following shows the operation with BYTELANE set values.



2.2.30 Layer 2 horizontal/vertical flip control registers

These registers (IMC_L2A_MIRROR: 4026_0624H and IMC_L2B_MIRROR: 4026_0724H) control horizontal/vertical flip of layers 2A and 2B.

These are update target registers.

31	30	29	28	27	26	25	24
Reserved							

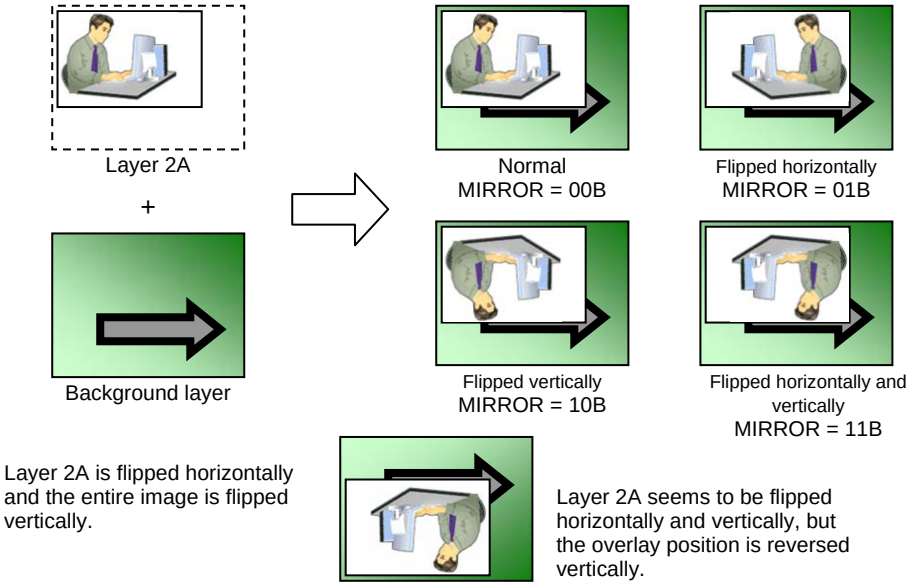
23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved						MIRROR	

Name	R/W	Bit	After Reset	Function
Reserved	R	31:2	0	Reserved. When these bits are read, 0 is returned for each bit.
MIRROR	R/W	1:0	0	Sets the image flip direction. 00: No flip 01: Horizontal flip 10: Vertical flip 11: Horizontal and vertical flip

Horizontal and vertical flip can be controlled for individual planes in layer 2. Flipping of layer 2 (setting with this register) and flipping of entire image (setting with IMC_MIRROR register) can be set at the same time, but setting both registers cancels the effect.



2.2.31 ARGB4444 mode register

This register (IMC_ARGBMODE: 4026_1000H) selects the layer that uses the ARGB4444 format.

For details on the operation, see **3.2.7 ARGB4444 format**.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved				L1C_ARGB	L1B_ARGB	L1A_ARGB	L0_ARGB

7	6	5	4	3	2	1	0
Reserved							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:12	0	Reserved. When these bits are read, 0 is returned for each bit.
L1C_ARGB	R/W	11	0	Enables the use of the ARGB4444 format for the relevant layer. The ARGB444 format is enabled when all these bits are set to 1, the transparent color is set for the layer (KEYENABLE register = 1), and RGB565 is selected for the layer.
L1B_ARGB	R/W	10	0	
L1A_ARGB	R/W	9	0	
L0_ARGB	R/W	8	0	
Reserved	R/W	7:0	0	Reserved. When these bits are read, 0 is returned for each bit. (Setting prohibited.)

2.2.32 Interrupt setting registers

These registers set various interrupt parameters. The IMC can issue five types of interrupts. Control of each interrupt is assigned to each bit of the interrupt setting registers. For details, see **Table 2-1 Interrupts**.

Table 2-1. Interrupts

Interrupt Name	Source	Bit Assignment
AHBR error response interrupt	Issued when a response other than OKAY is received from the AHB read side.	4
AHBW error response interrupt	Issued when a response other than OKAY is received from the AHB write side.	3
WB end interrupt	Issued when writeback to a cache frame is completed.	2
Overrun interrupt	Issued when writeback to a cache frame overruns.	1
Register update end interrupt	Issued when the update target register is updated.	0

A WB end interrupt occurs when the IMC finishes writing data to a cache frame. There is a latency until the written data is actually stored in the memory, because write is performed via a bus bridge or bus switch.

When AHB (R/W) abnormal response occurrence interrupt receives all except for the OKAY response of the AHB bus (Error/Retry/Split), interrupt is issued. There is a possibility that unjust data access occurred, but without stopping processing, IMC keeps moving just as it is. The AHB address value when interrupting and occurring, is stocked in an error address register.

An AHBR error response interrupt is generated when a response other than OKAY (EXOKAY, SLVERR, or DECERR) is returned from the AXI bus. At this time, the valid address is not stored but 0000_0000H is held in the error address register, and only the LOCK bit is set.

Details on the interrupt setting registers are described below.

(1) Interrupt status register

This is a read-only register (IMC_INTSTATUS: 4026_0900H) that indicates the status of interrupt sources. The statuses of the interrupt sources enabled with the interrupt enable set register can be read.

This is an immediately-reflected register, so changing of settings during operation is prohibited.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved			AHBRERR	AHBWERR	WBEND	OVERRUN	REFRESH

Name	R/W	Bit	After Reset	Function
Reserved	R	31:5	0	Reserved. When these bits are read, 0 is returned for each bit.
AHBRERR	R	4	0	Indicates the status of an AHBR error response interrupt. 0: No interrupt source 1: Interrupt source occurred
AHBWERR	R	3	0	Indicates the status of an AHBW error response interrupt. 0: No interrupt source 1: Interrupt source occurred
WBEND	R	2	0	Indicates the status of a WB end interrupt. 0: No interrupt source 1: Interrupt source occurred
OVERRUN	R	1	0	Indicates the status of an overrun interrupt. 0: No interrupt source 1: Interrupt source occurred
REFRESH	R	0	0	Indicates the status of a register update end interrupt. 0: No interrupt source 1: Interrupt source occurred

(2) Interrupt raw status register

This is a read-only register (IMC_INTRAWSTATUS: 4026_0904H) that indicates the statuses of interrupt sources. The bits corresponding to the interrupt sources are set regardless of the settings of the interrupt enable set register and the interrupt enable clear register.

This is an immediately-reflected register, so changing of settings during operation is prohibited.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved			AHBRERR RAW	AHBWERR RAW	WBEND RAW	OVERRUN RAW	REFRESH RAW

Name	R/W	Bit	After Reset	Function
Reserved	R	31:5	0	Reserved. When these bits are read, 0 is returned for each bit.
AHBRERRRAW	R	4	0	Indicates the raw status of an AHBR error response interrupt. 0: No interrupt source 1: Interrupt source occurred
AHBWERRRAW	R	3	0	Indicates the raw status of an AHBW error response interrupt. 0: No interrupt source 1: Interrupt source occurred
WBENDRAW	R	2	0	Indicates the raw status of a WB end interrupt. 0: No interrupt source 1: Interrupt source occurred
OVERRUNRAW	R	1	0	Indicates the raw status of an overrun interrupt. 0: No interrupt source 1: Interrupt source occurred
REFRESHRAW	R	0	0	Indicates the raw status of a register update end interrupt. 0: No interrupt source 1: Interrupt source occurred

(3) Interrupt enable set register

This register (IMC_INTENSET: 4026_0908H) enables issuance of interrupt requests. Only data of bits to which 1 is written is updated. When the bit corresponding to an interrupt source is set to 1 in this register, the interrupt source is set, the relevant interrupt request is issued and the corresponding bit of the interrupt status register is set to 1. If no bits are set in this register, no interrupt requests are issued even if the interrupt source is set, but the corresponding bit of the interrupt raw status register is set to 1.

This is an immediately-reflected register, so changing of settings during operation is prohibited.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved			AHBRERREN	AHBWEREN	WBENDEN	VERRUNEN	REFREHEN

Name	R/W	Bit	After Reset	Function
Reserved	R	31:5	0	Reserved. When these bits are read, 0 is returned for each bit.
AHBRERREN	R	4	0	Indicates whether issuance of AHBR error response interrupt requests is enabled. 0: Not enabled 1: Enabled
	W	4	–	1: Cancels interrupt masking.
AHBWERRN	R	3	0	Indicates whether issuance of AHBW error response interrupt requests is enabled. 0: Not enabled 1: Enabled
	W	3	–	1: Cancels interrupt masking.
WBENDEN	R	2	0	Indicates whether issuance of WB end interrupt requests is enabled. 0: Not enabled 1: Enabled
	W	2	–	1: Cancels interrupt masking.
OVERRUNEN	R	1	0	Indicates whether issuance of overrun interrupt requests is enabled. 0: Not enabled 1: Enabled
	W	1	–	1: Cancels interrupt masking.
REFRESHEN	R	0	0	Indicates whether issuance of register update end interrupt requests is enabled. 0: Not enabled 1: Enabled
	W	0	–	1: Cancels interrupt masking.

(4) Interrupt enable clear register

This is a write-only register (IMC_INTENCLR: 4026_090CH) that disables issuance of interrupt sources. Only data of bits to which 1 is written is updated. When the bit corresponding to an interrupt source in this register is set to 1, no interrupt requests are issued even if the interrupt source is generated. The status of the corresponding bit in the interrupt status register also remains unchanged. If no bits are set in this register, an interrupt request is issued and the corresponding bit of the interrupt status register is set to 1 when the interrupt source is set, and the corresponding bit of the interrupt status register is set to 1.

This is an immediately-reflected register, so changing of settings during operation is prohibited.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved			AHBRERR MASK	AHBWERR MASK	WBEND MASK	OVERRUN MASK	REFRESH MASK

Name	R/W	Bit	After Reset	Function
Reserved	–	31:5	0	Reserved.
AHBRERRMASK	W	4	0	Disables issuance of AHBR error response interrupt requests. 1: Masks the interrupt.
AHBWERRMASK	W	3	0	Disables issuance of AHBW error response interrupt requests. 1: Masks the interrupt.
WBENDMASK	W	2	0	Disables issuance of WB end interrupt requests. 1: Masks the interrupt.
OVERRUNMASK	W	1	0	Disables issuance of overrun interrupt requests. 1: Masks the interrupt.
REFRESHMASK	W	0	0	Disables issuance of register update end interrupt requests. 1: Masks the interrupt.

(5) Interrupt source clear register

This is a write-only register (IMC_INTFFCLR: 4026_0910H) that requests clearing of interrupt sources. Only data of bits to which 1 is written is updated. Setting the bit corresponding to an interrupt source to 1 clears the interrupt source.

If setting of an interrupt source due to the internal operation and clearing of an interrupt source by writing to this register are performed at the same time, setting takes precedence.

This is an immediately-reflected register, so changing of settings during operation is prohibited.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

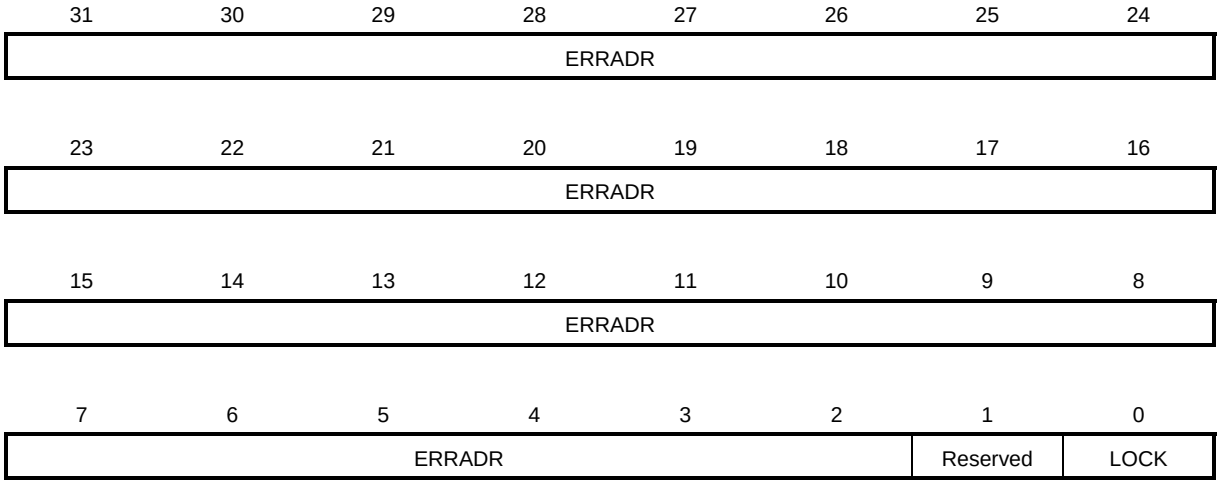
7	6	5	4	3	2	1	0
Reserved			AHBRERR CLR	AHBWERR CLR	WBEND CLR	OVERRUN CLR	REFRESH CLR

Name	R/W	Bit	After Reset	Function
Reserved	–	31:5	0	Reserved.
AHBRERRCLR	W	4	0	Requests clearing of an AHBR error response interrupt source. 1: Clears the interrupt source.
AHBWERRCLR	W	3	0	Requests clearing of an AHBW error response interrupt source. 1: Clears the interrupt source.
WBENDCLR	W	2	0	Requests clearing of a WB end interrupt source. 1: Clears the interrupt source.
OVERRUNCLR	W	1	0	Requests clearing of an overrun interrupt source. 1: Clears the interrupt source.
REFRESHCLR	W	0	0	Requests clearing of a register update end interrupt source. 1: Clears the interrupt source.

(6) Error address registers

These registers (IMC_AHBRERRADR : 4026_0914H and IMC_AHBWERRADR : 4026_0918H) retain the current HADDR status when an AHB bus response ERROR, RETRY or SPLIT is received during DMA transfer. During burst transfer, the value of the address at which the error response occurred plus 4 is stored. Since the IMC has two AHB buses, the error address register is provided individually for the read and write sides.

This is an immediately-reflected register, so changing of settings during operation is prohibited.



Name	R/W	Bit	After Reset	Function
ERRADR	R	31:2	0	Stores HADDR upon occurrence of an error response.
Reserved	R	1	0	Reserved. When this bit is read, 0 is returned.
LOCK	R/W	0	0	Checks the error status. 0: Stores the address when an error response occurs. 1: An error response occurred and the address was stored.

Caution If an error response occurs while the LOCK bit is set to 0, the current HADDR status is stored in the ERRADR bit and the LOCK bit is set to 1. While the LOCK bit is set to 1, ERRADR is not updated even if an error response occurs.
To acquire the error status again, set the LOCK bit to 0.
Writing 1 to the LOCK bit does not affect the setting.

CHAPTER 3 DESCRIPTION OF FUNCTIONS

3.1 Image Formats

3.1.1 Supported image formats

The IMC supports seven types of image formats. The buffer start address and address addition value are used for defining frame buffers in a memory space, the alignment of the required number of buffer start addresses and address addition values vary in each format. Figure 3-1 shows the definition of a frame buffer, and Table 3-1 lists the supported formats.

Figure 3-1. Frame Buffer Definition

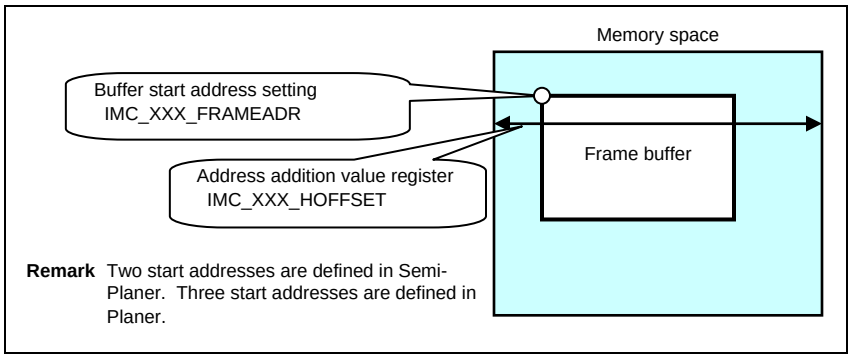


Table 3-1. Formats Supported by IMC

Format Name	Buffer Start Address	Address Addition Value Restriction[Note 1]	Minimum Horizontal Pixel Unit[Note 2]
RGB565	PLANE_ADR	Should be aligned to 1 word	2 pixels
RGB666	PLANE_ADR	Should be aligned to 9 words	16 pixels
YUV422 Pixel Interleave	PLANE_ADR	Should be aligned to 1 word	2 pixels
YUV422 Semi-Planar	YPLANE_ADR UVPLANE_ADR	Should be aligned to 1 word	4 pixels
YUV422 Planar	YPLANE_ADR UPLANE_ADR VPLANE_ADR	Should be aligned to 2 words (A U/V plane uses half the set value.)	8 pixels
YUV420 Semi-Planar	YPLANE_ADR UVPLANE_ADR	Should be aligned to 1 word	4 pixels
YUV420 Planar	YPLANE_ADR UPLANE_ADR VPLANE_ADR	Should be aligned to 2 words (A U/V plane uses half the set value.)	8 pixels

Notes 1. The address addition value is restricted so as to store image data pixels in memory without leaving spaces. For odd pixels, the number of words larger that those listed in the table, including the odd pixels can be set.

2. The minimum horizontal pixel unit is defined in image formats, but the IMC is the read side and drops data, a unit smaller than those listed in the table can be set.

The selectable format varies in each layer (layer 0, 1A, 1B, 1C, 2A, 2B and BG) defined in the IMC. Table 3-2 lists the layers and selectable format. See **Figure 3-3. Layer Definition**.

Table 3-2. Format Selectable for Each Layer

Layer Type	Supported Format
Layer 0	RGB565, RGB666
Layer 1A	RGB565, RGB666 (Same setting is applied to three planes in layer 1)
Layer 1B	
Layer 1C	
Layer 2A	Any format
Layer 2B	Any format
Layer BG	RGB565, RGB666, fixed colors[Note 1]
Synthesis result (LCD display data)[Note 2]	RGB565, RGB666

Notes 1. Fixed colors are determined by RGB666-format values set in the LCD controller (LCD_BACKCOLOR register value).

2. Set the synthesis result format in the LCD controller (LCD_IFORMAT register) in LCD-synchronous mode. In immediate startup mode, it is set according to the setting of the IMC_WB_FORMAT register.

Layer 2 can select any image format. The register that defines the start addresses of frame buffers varies depending on the specified format. Table 3-3 lists the definitions of start addresses in each format.

Table 3-3. Formats and Start Address Setting Registers

Selected Format	Number of Planes	Setting Method	
		Stored Data	Register That Sets Start Address
RGB565/RGB666	1	RGB plane	Address register for Y
YUV422 Pixel Interleave	1	YUV plane	Address register for Y
YUV422 Semi-Planar YUV420 Semi-Planar	2	Y plane	Address register for Y
		UV plane	Address register for U
YUV422 Planar YUV420 Planar	3	Y plane	Address register for Y
		U plane	Address register for U
		V plane	Address register for V

3.1.2 Conversion rule

The format of each layer is converted into RGB666 when data is captured into the IMC.

The data format is unified and images are synthesized, the resulted data is converted into the format for synthesized images set in the LCD (RGB565 or RGB666), and then supplied to the LCD controller and written back to the cache frame. Table 3-4 lists the format conversion rules.

Table 3-4. Format Conversion Rules

Conversion from Each Format into RGB666	
RGB565	Adds the MSB to the LSB of R and B.
YUV422 Pixel Interleave YUV422 Semi-Planar YUV422 Planar YUV420 Semi-Planar YUV420 Planar	The following three steps are performed sequentially. • Gain/offset adjustment (8-bit accuracy before and after adjustment) • YUV-to-RGB conversion (8-bit accuracy before and after adjustment) • Converts into RGB666 by dithering (Can be turned off) **Remark** For details on dithering, see **3.1.5 Dithering**.
Conversion from RGB666 into RGB565	
RGB666	Discards the LSB of R and B.

3.1.3 Gain and offset adjustment

The gain and offset of YUV format data can be adjusted in the range from 0 to x255/x128.

Each item can be set with the Y gain offset register (IMC_YGAINOFFSET), U gain offset register (IMC_UGAINOFFSET) and V gain offset register (IMC_VGAINOFFSET). For details on the set values and adjusted items, see the descriptions of each register.

Table 3-5. Gain/Offset Adjustment Register

Setting Register	Symbol	Refer to:
Y gain offset register	IMC_YGAINOFFSET	**2.2.14 Y gain offset register**
U gain offset register	IMC_UGAINOFFSET	**2.2.15 U (V) gain offset registers**
V gain offset register	IMC_VGAINOFFSET	

3.1.4 YUV-to-RGB conversion

YUV format data can be converted into the RGB format by using arithmetic calculation.

The IMC can select a calculation coefficient from ITU-R BT.601-compliant, ITU-R BT.709-compliant, custom coefficient (with or without Y value subtracted by 16) for YUV-to-RGB format conversion, by setting the IMC_YUV2RGB register.

When using a custom coefficient for conversion, separately set the coefficient in the IMC_COEF_[RGB][0-3] registers.

For details on conversion formulas, see **2.2.17 Custom coefficient registers**.

3.1.5 Dithering

Dithering is a method of pseudo tone processing. With dithering, the rounding error in lower bits, which occurs when dropping the data tone (masking colors), is dispersed to the surrounding pixels. Dithering allows the expression of natural colors with low tone.

When converting a YUV format into RGB666, the IMC can perform dithering after conversion with a 3 × 4 matrix calculation. The IMC employs systematic 2 × 2 dithering.

Table 3-6. Dithering Table Values

	LSB on Horizontal Coordinate of Synthesized Image	
LSB on Vertical Coordinate of Synthesized Image	0	1
0	0	2
1	3	1

Dithering is performed for each pixel of synthesized images to be output from the IMC.

First, select a table value listed in **Table 3-6 Dithering Table Values**, based on the position of the current pixel to be processed(coordinate based on the synthesized image). This table value is used to switch how the lower 2 bits are handled during 8-to-6-bit conversion. During ordinary conversion with rounding off, the value is rounded up if bit 1 of the original 8-bit data is 1, or rounded off if it is 0 (02H is added and then the lower 2 bits are dropped). With dithering by the IMC, the table value is added and then the lower 2 bits are dropped. As a result, data is rounded with the probability shown in **Table 3-7 Probability of Dithering Error Dispersion**.

Table 3-7. Probability of Dithering Error Dispersion

Lower 3 Bits of Original Data	Probability for Round up	Probability for Round off
0	0/4	4/4
1	1/4	3/4
2	2/4	2/4
3	3/4	1/4

Remark The probability in the above table means the probability with which rounding up or off is performed for vertical and horizontal 2 pixels, four pixels in total.

The detailed operation performed during dithering conversion is shown below.

Figure 3-2. Color Masking by Dithering

■ Converting 8-bit Red data into 6-bit data

Original data before dithering performed (8 bits of red component)

	0	1	2	3	4	5
0	13H	14H	14H	21H	28H	3AH
1	32H	2CH	33H	40H	51H	55H
2	F4H	F0H	F1H	DDH	FAH	FAH
3	E0H	E5H	CCH	C2H	FAH	FAH

Dithering table values for each coordinate

	0	1	2	3	4	5
0	0	2	0	2	0	2
1	3	1	3	1	3	1
2	0	2	0	2	0	2
3	3	1	3	1	3	1

■ Dithering procedures

- First, expand the dithering table to the size of the layer to be processed (right table).
- Calculate the value of upper-left pixel (V, H) = (0, 0).
- Add table value “0” to 13H and drop the lower 2 bits. As a result, 4H is obtained.
- Next, calculate the second pixel (0, 1).
- Add table value “2” to 14H (original data) and drop the lower 2 bits. As a result, 5H is obtained.
- Pixels are processed as shown above and corrected to be 6-bit tones.

■ Comparison between results of converted data with dithering performed and converted data with rounding on/off

Converted data with dithering performed (6 bits of red component)

	0	1	2	3	4	5
0	04H	05H	05H	08H	0AH	0FH
1	0DH	0BH	0DH	10H	15H	15H
2	3DH	3CH	3CH	37H	3EH	3FH
3	38H	39H	33H	30H	3FH	3EH

Converted data with rounding on/off

	0	1	2	3	4	5
0	05H	05H	05H	08H	0AH	0FH
1	0DH	0BH	0DH	10H	14H	15H
2	3DH	3CH	3CH	37H	3FH	3FH
3	38H	39H	33H	31H	3FH	3FH

* Shaded pixels do not match the corresponding pixels of data with dithering performed

As shown in the right-bottom area, for example, where an intermediate color is filled (lower 2 bits of the original 8-bit data are not 0), differences between the intermediate tone resulting from dithering and converted data with rounding on/off appear significantly.

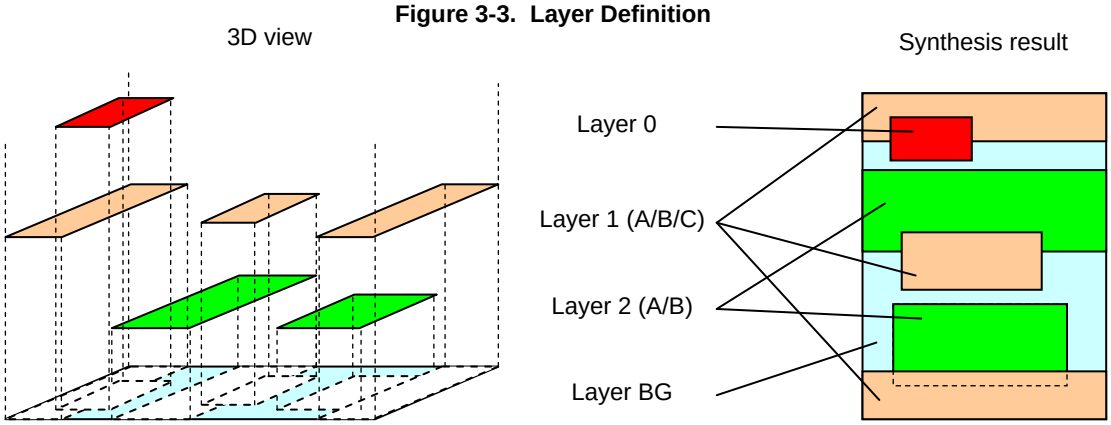
3.2 Image Synthesis Function

3.2.1 Layer definition

The IMC can handle four layers in the depth direction (front and back): layers 0, 1, 2, and background. Layer 1 has three planes at the same depth, and layer 2 has two planes at the same depth. The positional relationship between layers is fixed. The supported formats and settable parameters vary in each layer.

Figure 3-3 shows the concept of layers, and Table 3-8 lists the parameter features.

Figure 3-3. Layer Definition



If layers that are defined at the same depth (layers 1A/1B/1C and layers 2A/2B) are set to overlap, a priority is given to layer 1A, layer 1B and layer 1C, in that order.

If layers that are defined at the same depth (layers 1A/1B/1C and layers 2A/2B) are set to different display positions, a selection priority is given to layer 1A, layer 1B and layer 1C, in that order. Between layers 2A and 2B, layer 2A is given a priority.

As shown in Figure 3-4, for example, if layers 1B and 1C are overlapped and the transparent background is set to layer 1B, layer 1B is brought to the front at the position where two layers overlap. Layer 1C hidden behind the transparent portions of layer 1B is not displayed but the background is displayed.

Layer synthesis processing can overlap up to three planes (layer 0 + layer 1x + layer 2x or layer BG).

Figure 3-4. Duplicated Setting of Layers at the Same Depth

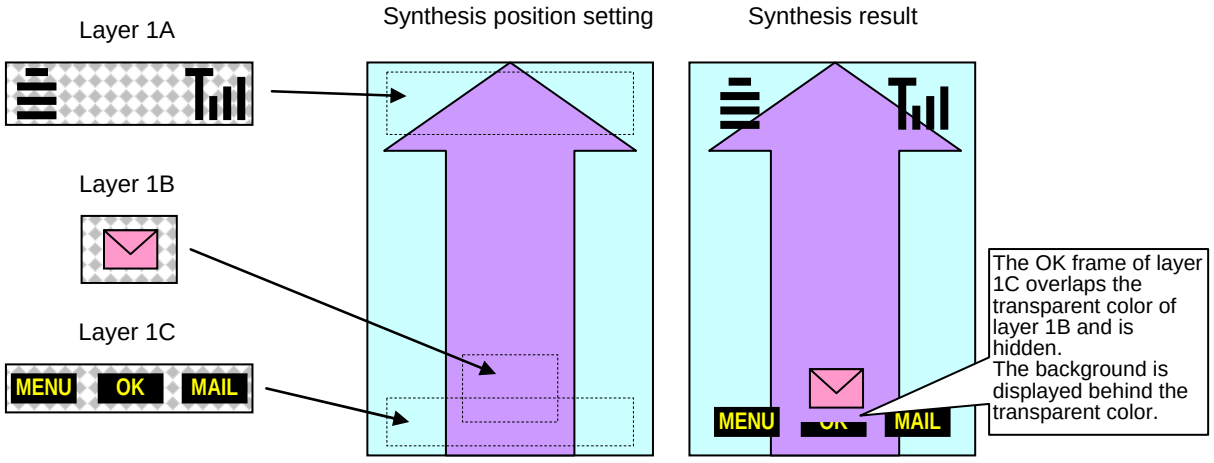


Table 3-8. Setting Parameters

	Layer 0	Layer 1A	Layer 1B	Layer 1C	Layer 2A	Layer 2B	Layer BG
Settings related to frame buffer definition	Start address	Start address	Start address	Start address	Start address Note 1	Start address Note 1	Start address
	Address addition	Address addition (common to three layers)			Address addition	Address addition	Address addition
Supported format	RGB565/ RGB666	RGB565/RGB666 (common to three layers)			Any	Any	Fixed colors of RGB565/ RGB666
Settings for displayed screen	Position (X/Y) Size (X/Y)	Position (X/Y) Size (X/Y)	Position (X/Y) Size (X/Y)	Position (X/Y) Size (X/Y)	Position (X/Y) Size (X/Y)	Position (X/Y) Size (X/Y)	–
Display size limitation (X,Y)	255, 255	1023, 2046	1023, 2046	1023, 2046	2046, 2046	2046, 2046	2046, 2046
Transparent color and alpha blending	○	○ Note 2	○ Note 2	○ Note 2	×	×	×
Flipping of individual layer	×	×	×	×	○	○	×
Flipping of synthesized image	○ (Can be set for individual synthesized image)						
Simple double resizing	○	○ (common to three layers)			○	○	○
Double buffer control	×	×	×	×	○	○	×
Gain/offset adjustment	×	×	×	×	○ (only for YUV, common to layers)		×
Display ON/OFF control	○	○	○	○	○	○	×
Gamma correction	○ (Can be set for individual synthesized image)						

○: Supported, ×: Not supported, −: No function

Notes 1. Since layer 2 supports the YUV formats, three registers are provided for Y, U and V. Layer 2 also supports the double buffer, therefore, it has six setting registers in total.

2. Turning on/off of the transparent color function can be set separately for layers 1A, 1B and 1C, but the transparent color values are commonly applied to three layers.

3.2.2 Transparent colors (key color)

Transparent colors can be set separately for layers 0 and 1. When arbitrary values of pixel data expressed in the RGB format are defined as a transparent color and pixel data values of the target layer match the transparent color set value, transparency processing is performed and the background layer can be seen through. The setting registers for each layer are listed below.

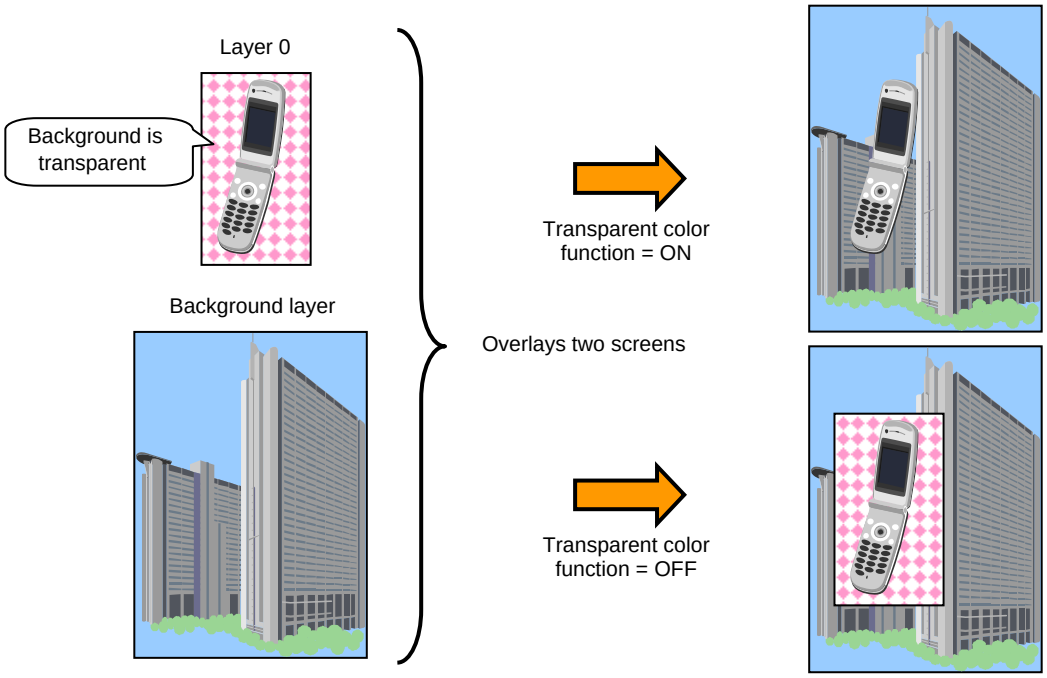
Table 3-9. Transparent Color Setting Registers

Layer Type	Setting Register Name	Refer to:
Layer 0	IMC_L0_KEYENABLE	**2.2.20 Transparent color control registers**
Layer 1A	IMC_L1A_KEYENABLE	
Layer 1B	IMC_L1B_KEYENABLE	
Layer 1C	IMC_L1C_KEYENABLE	
Layer 0	IMC_L0_KEYCOLOR	**2.2.21 Layer transparent color registers**
Layer 1x	IMC_L1X_KEYCOLOR	

Refer to descriptions on each register for details on the register settings.

Figure 3-5 shows how images are synthesized with the transparent color function.

Figure 3-5. Transparent Color Function



3.2.3 Alpha blending

Alpha blending can be set separately for the A, B and C planes of layers 0 and 1. Alpha blending is a method of processing to opaque images, in 64 steps. When alpha blending is enabled for a target layer, opaque processing is performed for all the layer planes and the background layer can be seen through.

The setting registers for each layer are listed below. (This function can be enabled together with the transparent color function.)

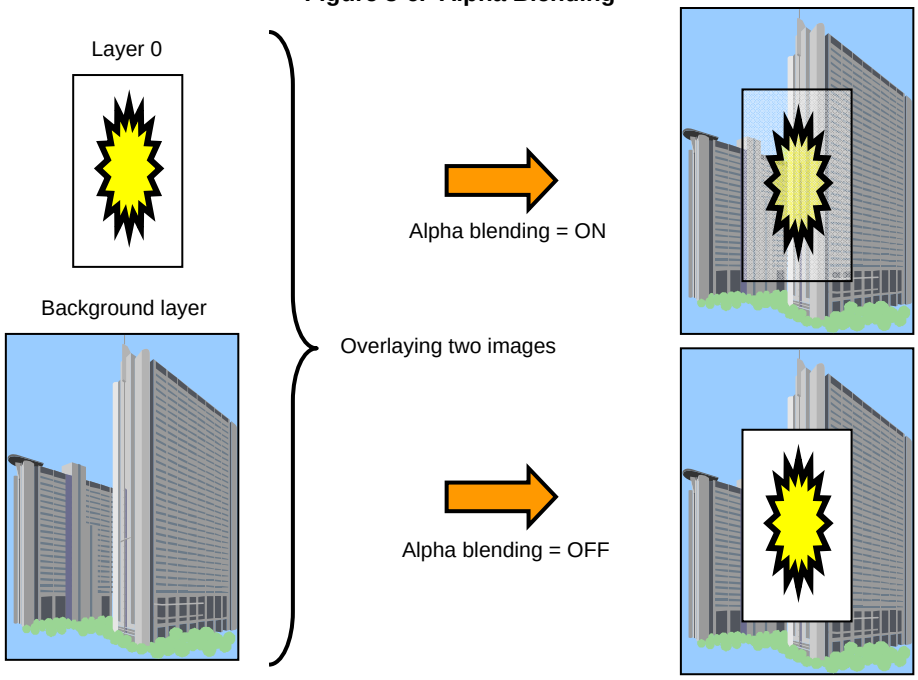
Table 3-10. Alpha Blending Setting Registers

Layer Type	Setting Register Name	Refer to:
Layer 0	IMC_L0_ALPHA	**2.2.22 Alpha registers**
Layer 1A	IMC_L1A_ALPHA	
Layer 1B	IMC_L1B_ALPHA	
Layer 1C	IMC_L1C_ALPHA	

Refer to descriptions on each register for details on register settings.

Figure 3-6 shows how images are synthesized with the alpha blending function.

Figure 3-6. Alpha Blending



[Calculation of desired values when layers 0 and 1x overlap and alpha blending is enabled for both layers]

The IMC first processes the backward data. When synthesizing layers 0, 1 and BG, layers 1 and BG are synthesized first. If alpha blending settings have been made for layer 1, blending is performed according to the set values. Synthesis with layer 0 is then performed for the resulted 6-bit value.

This processing can be expressed with the following general expression (when ALPHA = 63, the forward layer is used because no layers are opaque).

PixTemp = {L1_ALPHA × PixL1 + (64 − L1_ALPHA) × PixBG} / 64

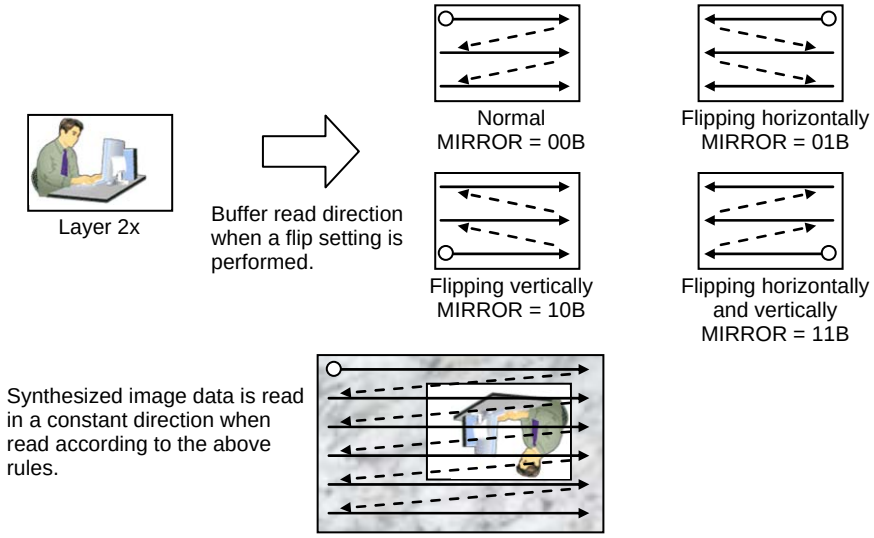
PixOut = {L0_ALPHA × PixL0 + (64 − L0_ALPHA) × PixBG} / 64

3.2.4 Image flip

Flipping images horizontally or vertically can be set separately for the A and B planes of layer 2. When horizontal or vertical flipping is set to layer 2, the display position does not change but only image data of layer 2 is flipped.

Aside from this function, a similar flip setting can be performed for images output by the IMC (synthesized images). With this processing, the synthesized and displayed position appears to be flipped.

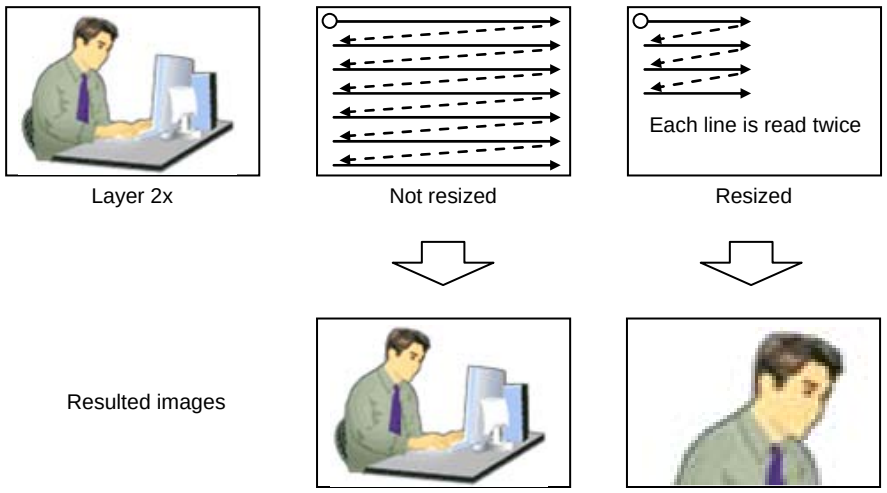
Figure 3-7. Operation When Image Flipping Is Enabled



3.2.5 Simple resizing

The simple doubling function is provided for each layer so as to reduce the image data size in frame buffers and the data amount read from buffers. Data read by the IMC from a frame buffer is simply doubled horizontally. Data in the vertical direction is read from the same line, in 2-line units. As a result, the bus bandwidth required for reading data can be halved.

Figure 3-8. Operation When Simple Resizing Is Enabled

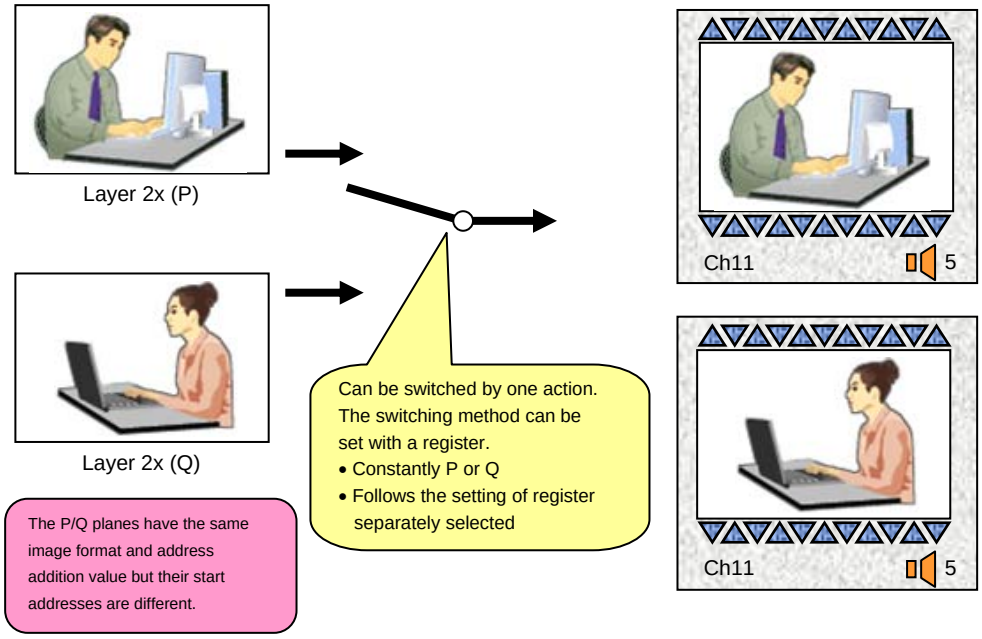


3.2.6 Double buffer

Planes A and B of layer 2 can have two sets of definitions, P and Q, for individual frame buffer.

Which of P and Q is selected can be set with the double buffer control register (IMC_L2A/B_BUFSEL) for each layer. The fixed P/Q, CPU control or A3D control can be set. When CPU control is set, layers 2A and 2B can be changed at the same time, by separately setting the CPU double buffer control register (IMC_CPUBUFSEL).

Figure 3-9. Operation When Double Buffer Function Is Enabled



3.2.7 ARGB4444 format

This section explains the functions supported by ARGB4444. With the ARGB4444 format, transparent colors and alpha blending settings can be set individually for four layers 0, 1A, 1B and 1C.

Layers 0 and 1x are set to the ARGB4444 format as a result of ANDing the following conditions.

- The ARGB bit of the ARGB4444 mode register is set to 1 for the relevant layer.
- The transparent color function is enabled for the relevant layer (KEYEN bit of IMC_Lx_KEYENABLE register = 1)
- RGB565 is selected for the relevant layer (FORM bit of IMC_Lx_FORMAT register = 1)

When the alpha-blending value is set to 0 (ALPHA bit of IMC_Lx_ALPHA register) for the relevant layer, the IMC judges that the image is transparent before starting image synthesis and does not read the data from the memory. As a result, the image is not displayed even if ARGB4444 is selected.

The ARGB4444 data storage format is explained below.

With the ARGB4444 format, four elements of each pixel (ALPHA value, RED value, GREEN value and BLUE value) are each stored in 4 bits, and one pixel is expressed by using 16 bits. Only 12 bits can be used for expressing colors but the transparency can be set in 16 steps per pixel, so this format is suitable for images such as OSD that can be expressed by simple colors.

15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
ALPHA	RED	GREEN	BLUE

In the IMC circuit, the higher 2 bits are extended toward the lower side for four elements and one element is expressed by using 6-bit data. The existing settings of ALPHA and KEYCOLOR are ignored in the layer for which ARGB4444 is selected.

DATA[3]	DATA[2]	DATA[1]	DATA[0]

↓

DATA[3]	DATA[2]	DATA[1]	DATA[0]	DATA[3]	DATA[2]

The following shows an image in which ARGB4444 is applied.

[Display conditions]

The above image is composed of four layers: Layers 0 (upper left), 1A (upper right), 1B (bottom left), and 1C (bottom right).

The transparency of frames drawn in red, green and yellow and characters written in blue is set to 0% (α = 0xF; opaque), the transparency of spaces between the red frame and green frame is set to 100% (α =0x0; transparent), the transparency of spaces between the green frame and yellow frame is set to 75% (α = 0x4), and the transparency of areas other than the blue characters inside the yellow frame is set to 50% (α = 0x8). All the pixels other than those of frames and characters are set to magenta.

3.3 Gamma Correction Function

3.3.1 Gamma correction

The IMC performs gamma correction by table referencing. The tables used for conversion include 6 bits each for RGB (equivalent to 64 addresses), and can be accessed via the APB bus. Three areas in a 1-port SRAM, each of which consists of 6 bits × 64 words, are used for storing table data. RGB data before correction is handled as the table memory addresses, and the read values are handled as RGB data after correction.

Since it is a 1-port SRAM, accessing via the APB bus is possible only when gamma correction is disabled in the gamma correction control register (IMC_GAMMA_EN). Accessing via the APB bus is not guaranteed when gamma correction is enabled.

The gamma correction table address register (LCD_GAMMA_ADR) and gamma correction table data register (LCD_GAMMA_DATA) are used for accessing the table memory via APB. To write data to the table, first write the address where the target data is stored, to the gamma correction table address register. Next, write the data to the gamma correction table data register. Data is then written to the table memory indirectly. The gamma correction table address register is automatically incremented when the gamma correction table data register is written, so the table data register can be written successively.

To read data from the table memory, the procedure is the same but the registers must be read twice. First, set the address from which the target data is read, to the gamma correction table address register. Next, read the gamma correction table data register twice. Data is then read from the table memory indirectly, upon the second read.

To set the gamma correction table values, set bit 11 (gamma correction CLK control) of the control register (IMC_CONTROL) to 0 (automatic control disabled, CLK constantly supplied).

Bits 21 to 16, bits 13 to 8 and bits 5 to 0 of the gamma correction table data register are assigned for accessing the table memory of red, green, and blue, respectively.

The following shows the structure of the gamma correction table. R*n*, G*n*, and B*n* indicate the correction values for red, green and blue.

Figure 3-10. Gamma Correction Tables

Address	Table for Red (5 … 0)	Table for Green (5 … 0)	Table for Blue (5 … 0)
0	R0	G0	B0
1	R1	G1	B1
:	:	:	:
n	R*n*	G*n*	B*n*
:	:	:	:
63	R63	G63	B63
	21 … 16	13 … 8	5 … 0 (Corresponding to register bits)

3.3.2 Usage of gamma correction function

The following explains the usage of the gamma correction function.

<1> Set IMC_GAMMA_EN to 0. (Setting during IMC operation is prohibited.)

<2> Set IMC_GAMMA_ADR to 0H.

<3> Write to IMC_GAMMA_DATA the value converted from input value 0.
(IMC_GAMMA_ADR is automatically incremented to 1.)

<4> Write the values converted from input values 1 to 63.

<5> After writing values to all the tables, set IMC_GAMMA_EN to 1.

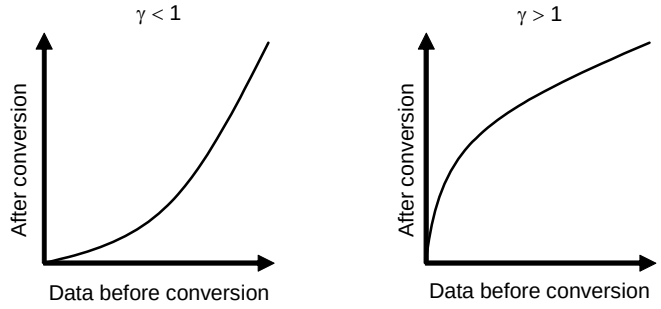
Gamma correction is then performed for images output from the IMC.

Even if <3> and <4> are not performed in succession, an arbitrary address can be set each time (by repeating <2> and <3>).

Generally, the relationship between a gamma value (γ) and I/O can be expressed as follows (as reference for calculating table values).

$$Out = In^{\frac{1}{\gamma}}$$

Figure 3-11. Gamma Correction



The IMC performs gamma adjustment by referencing tables for any value. Therefore, adjustment such as negative-positive reverse, can be set freely, without being constrained by the above conversion formula.

3.4 Operation Timing

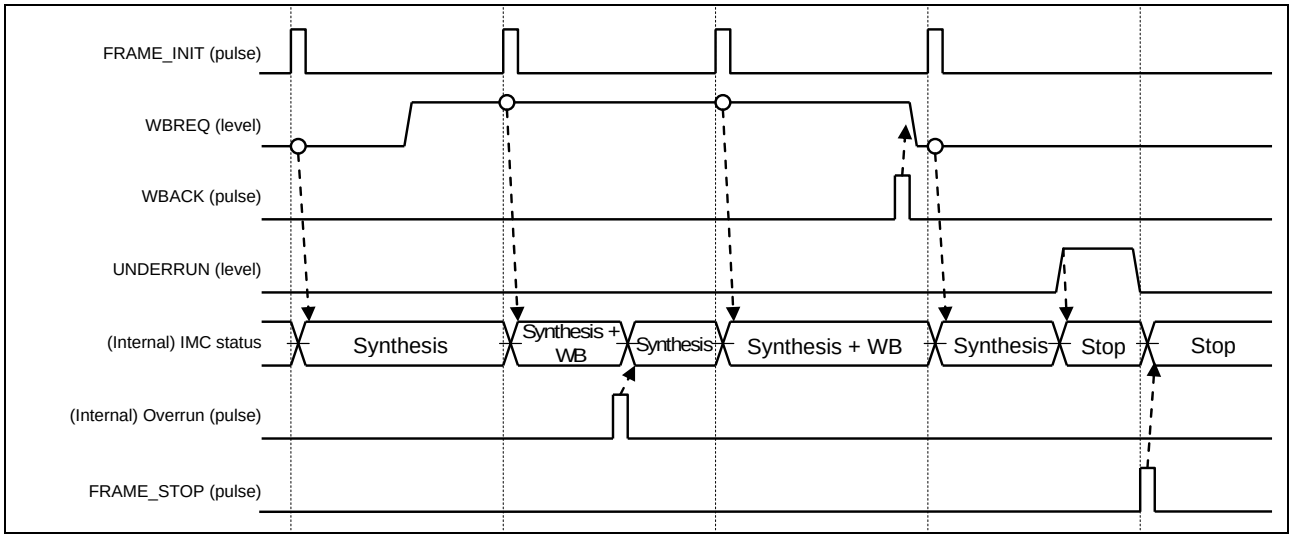
3.4.1 LCD interface

When operating in the LCD-synchronous mode, the IMC starts in synchronization with frame output by the LCD controller. The trigger signal is a pulse signal from the FRAMEINIT pin. A pulse signal from the FRAMESTOP pin is used as the operation stop request signal from the LCD controller. The IMC stops operating when it receives this pulse.

The IMC determines whether to perform WB processing at the same time as supplying data to the LCD controller, based on the level of the WBREQ pin when the trigger signal is generated. When WB processing is performed, WBACK is issued to indicate completion of WB from the IMC and WBTRACEEND (indicating that no data remains on the bus and therefore the power of the LOGIC1 domain can be turned off) is issued to indicate that the last data in the cache has been completely received in the MEMC. WBTRACEEND is used as an interrupt source for the LCD controller.

The IMC has a mechanism to terminate a frame when UNDERRUN, which indicates the occurrence of an LCD controller buffer underrun, is received. Figure 3-12 shows the timing of a series of control operations performed between the LCD controller and IMC.

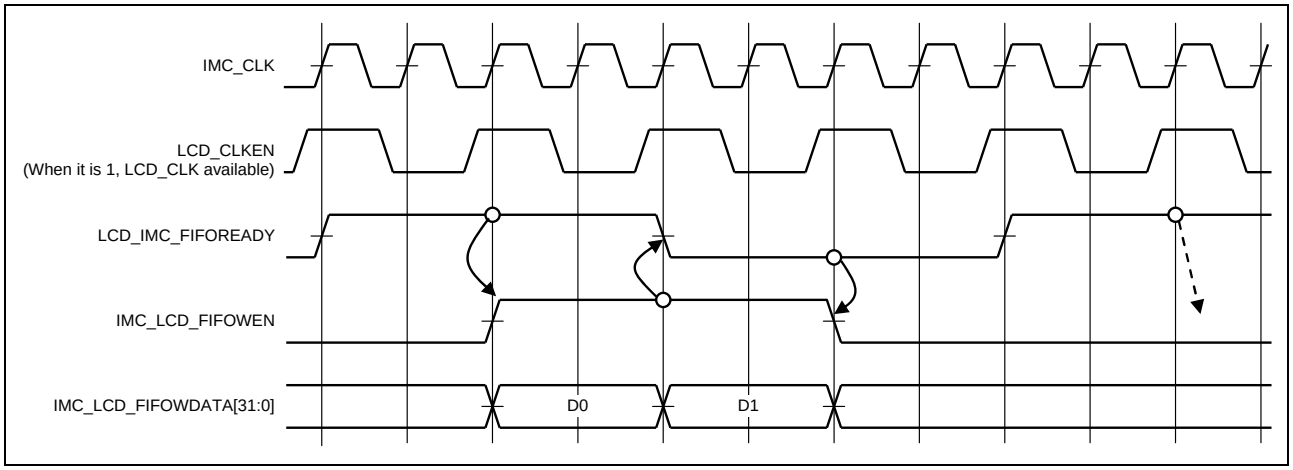
Figure 3-12. Startup Timing Between IMC and LCD Controller



The display data interface between the IMC and the LCD controller operates in accordance with the following rules.

- The LCD controller is synchronized with LCD_CLKEN so as to operate on half the frequency of IMC_CLK.
- The LCD controller sets FIFOREADY if the FIFO has an empty space of 8 words.
- When the IMC detects that FIFOREADY is set to 1, it sets FIFOWEN and FIFOWDATA, if there is data that can be output.
- If no data is ready on the IMC side, no data is output even if the LCD controller is in the READY state.

Figure 3-13. Timing of Display Data Interface Between IMC and LCD Controller



3.4.2 Register update

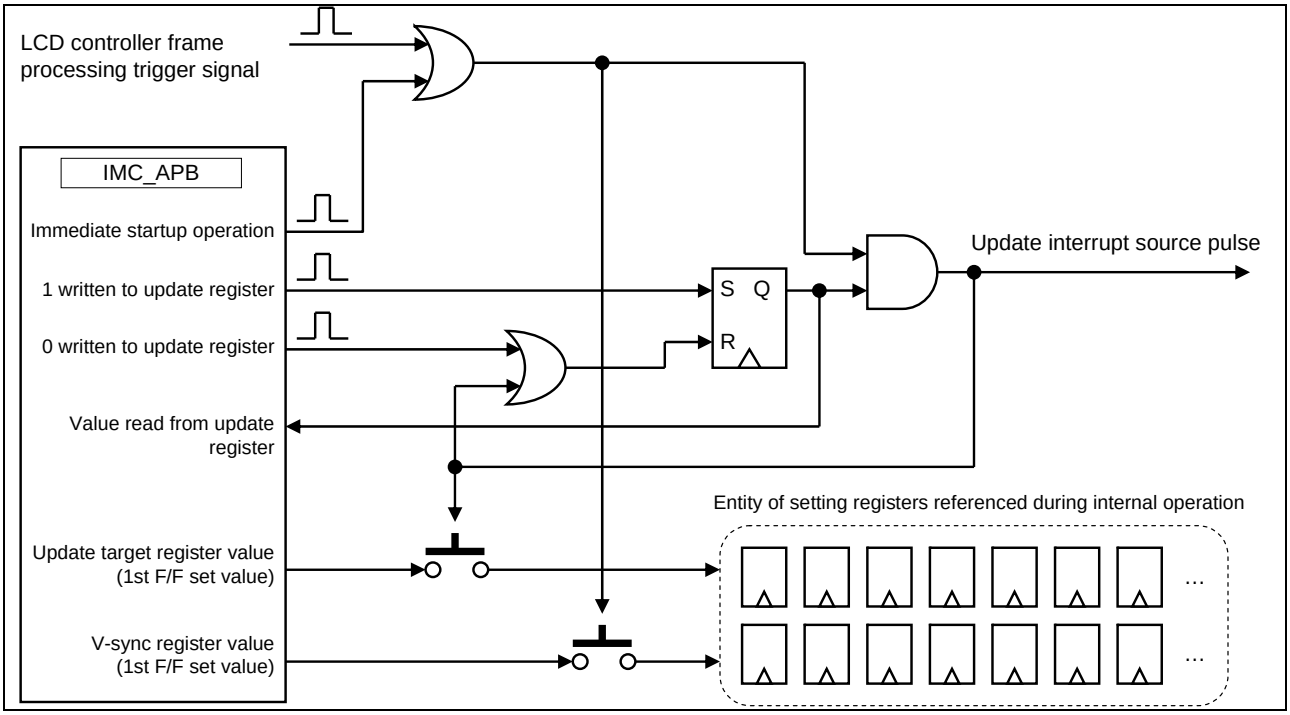
The IMC registers are updated (the set value is reflected in the internal operations) at three types of timing. According to the type, each register is classified as the immediately-reflected register, V-sync register, or update target register.

The entity of the F/Fs of immediately-reflected registers exists in the IMC_APB block, and their values are updated immediately when they are accessed via the APB bus. Each sub-module in the IMC operates by directly referencing the values of the F/Fs.

The V-sync and update target registers have the first F/F in the IMC_APB block, and the second F/F, which is referenced during actual circuit operation, in each block. The V-sync registers and update target registers are classified according to the conditions under which the set value is copied from the first F/F to the second F/F. With the V-sync registers, the value is copied when frame processing starts. With the update target registers, the value is copied if the register has been reserved for update when frame processing starts.

Figure 3-14 shows the circuit diagram of these registers and the update reserved register (IMC_REFRESH: 4026_0004H).

Figure 3-14. Relationship Between Update Register and V-Sync/Update Target Registers



APPENDIX A TERMINOLOGY

Frame buffer

Memory area for storing images. In the IMC, it may see a specific memory area.

Layer

Image of a plane

Overlay

Processing to overlay multiple layers to generate a new image

BG (background)

In the IMC, it means the background layer.

Alpha blending (α blending)

Function to modify the transparency of images during overlay to make multiple images to be seen through

Key color (mask color, transparent color)

Function to specify transparent colors during overlay to make the backward layers to be seen through as they are

Color space conversion

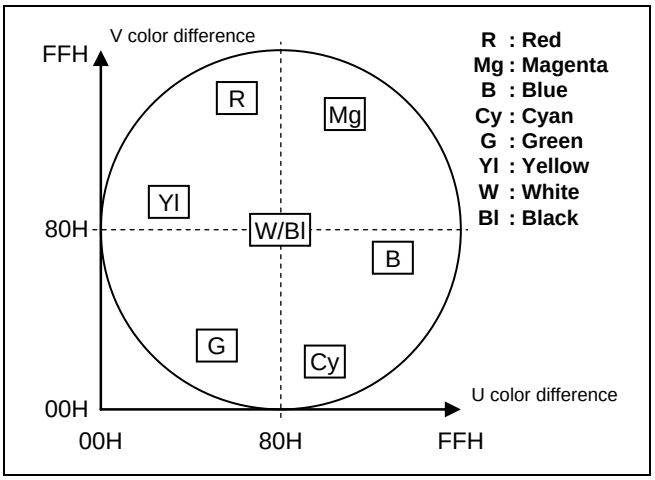
Two methods are available to express color data in numeric values: one is RGB, which uses three primary colors - red, green and blue, and the other is YUV, which uses the luminance (γ) and color difference components (U and V). Conversion between these formats is called color space conversion.

RGB565/666

When color data is expressed in the RGB format, the format in which each component is scaled by 6 bits is called RGB666, and the format in which G is scaled by 6 bits and R and B are scaled by 5 bits is called RGB565.

YUV422/420 (YUV444)

When color data is expressed in a YUV format, the format that defines a single color difference component for one luminance component is called YUV444, the format that defines a single color difference component for luminance data of two horizontal pixels is called YUV422, and the format that defines a single color difference component for luminance data of two horizontal and vertical pixels, four pixels in total, is called YUV420. The hue expressed with UV is illustrated as shown below. (The U and V components are represented in offset binary coding with 80H positioned as the center.)



Dithering

The method of displaying colors by combining displayable colors to express intermediate colors with few available colors. The image is displayed less sharp, but this method shows images as if the number of displayable colors is increased.

The IMC employs the systematic dithering method using a 2 × 2 matrix, when converting 8-bit data obtained by YUV-to-RGB conversion into 6-bit data to be used internally in circuits (color masking).

WB (Writeback)

Processing to write back display image data created by the IMC into the frame cache area which is specified in a system memory space. The written back data is used in the direct path mode in the LCD controller.

Revision History

Date	Revision	Comments
February 10, 2009	1.0	–
April 27, 2009	2.0	Incremental update from comments to the 1.0..
September 30, 2009	3.0	Incremental update from comments to the 2.0..

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