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RENESAS

User's Manual

Multimedia Processor for Mobile Applications

LCD Controller

EMMA Mobile1

Document No. S19258EJ3V0UM00 (3rd edition)
Date Published June 2009

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M8E 02. 11-1

PREFACE

Readers

This manual is intended for hardware/software application system designers who wish to understand and use the LCD controller functions of EMMA Mobile1 (EM1), a multimedia processor for mobile applications.

Purpose

This manual is intended to explain to users the hardware and software functions of the LCD controller of EM1, and be useful as reference material for developing hardware and software for systems that use EM1.

Organization

This manual consists of the following chapters.

- Chapter 1 Overview
- Chapter 2 Pin functions
- Chapter 3 Registers
- Chapter 4 Description of functions
- Chapter 5 Usage procedures

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electricity, logic circuits, and microcontrollers.

To understand the functions of the LCD controller of EM1 in detail

→ Read this manual according to the **CONTENTS**.

To understand the other functions of EM1

→ Refer to the user's manual of the respective module.

To understand the electrical specifications of EM1

→ Refer to the Data Sheet.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB
	Decimal ... xxxx
	Hexadecimal ... xxxxH
Data type:	Word … 32 bits
	Halfword … 16 bits
	Byte … 8 bits

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name		Document No.
MC-10118A Data sheet		S19657E
μ PD77630A Data sheet		S19686E
User's manual	Audio/Voice and PWM Interfaces	S19253E
	DDR SDRAM Interface	S19254E
	DMA Controller	S19255E
	I^2C Interface	S19256E
	ITU-R BT.656 Interface	S19257E
	LCD Controller	This manual
	MICROWIRE	S19259E
	NAND Flash Interface	S19260E
	SPI	S19261E
	UART Interface	S19262E
	Image Composer	S19263E
	Image Processor Unit	S19264E
	System Control/General-Purpose I/O Interface	S19265E
	Timer	S19266E
	Terrestrial Digital TV Interface	S19267E
	Camera Interface	S19285E
	USB Interface	S19359E
	SD Memory Card Interface	S19361E
	PDMA	S19373E
	One Chip (MC-10118A)	S19598E
	One Chip (μ PD77630A)	S19687E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

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LIST OF TABLES

CHAPTER 1 OVERVIEW

The LCD controller outputs synchronization signals and video signals to an LCD panel externally connected to EM1.

Since the LCD controller usually operates in association with the image composer module, some descriptions in this user's manual assume that the reader knows the functions of the image composer module. Also see the **Multimedia Processor for Mobile Applications - Image Composer User's Manual (S19263E)**.

1.1 Features

The main features of the LCD controller are as follows.

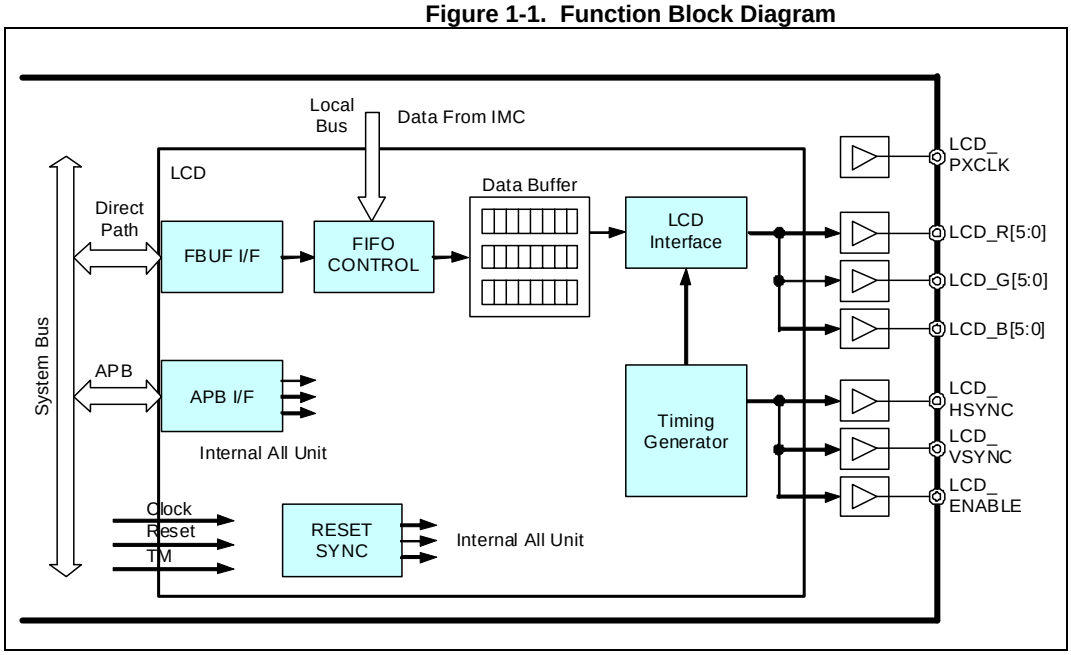
- ○ Supported LCD panel specifications
  - ～WVGA (800×480
  - TFT colors: 16 bpp (65,536 colors) and 18 bpp (up to 260,000 colors)
- ○ LCD interface
  - Pixel clock output (LCD_PXCLK)
  - Horizontal synchronization signal (LCD_HSYNC)
  - Vertical synchronization signal (LCD_VSYNC)
  - Data bus enable (LCD_ENABLE)
  - Data bus (LCD_R[5:0], LCD_G[5:0], LCD_B[5:0])
- ○ Data format
  - Output to LCD panel: RGB565 or RGB666 selectable
  - Input from memory: RGB565 or RGB666 selectable
    Operating in conjunction with the IMC, formats of YUV422/YUV420 (YUV Interleave, Y/UV2 plane, Y/U/V3 plane) can also be supported.

Signal Name	Limit
LCD_CLK (Main Operation) LCD_CCLK (Bus Access)	Max 166MHz
LCD_PCLK (APB Register)	Max 133MHz (LCD_CLK and identical clock or synchronous 2 division clock)

Caution The LCD controller supports an LCD panel with up to 1,024 × 1,024 pixels. If data is displayed with the maximum size, the traffic volume of transfer from frame buffer is increased significantly, which raises the occupancy rate of the system bus. Determine the size of the LCD panel to be used, by taking into consideration the bus transfer bandwidth that can be used by function blocks other than the LCD controller can be used.

1.2 Function Block Diagram

Figure 1-1. Function Block Diagram



The movement outline of each process is indicated below.

LCD has clock input of 3 systems of the LCD_CLK (LCD_CCLK) and LCD_PCLK and LCD_LCLK. A frequency, LCD_LCLK, 6-50MHz and LCD_PCLK, 83MHz and LCD_CLK are 166MHz. Synchronization is related in LCD_PCLK and LCD_CLK. LCD_LCLK, asynchronousness. LCD_CCLK is completely an identical source with LCD_CLK, but control is a possible clock for power-saving correspondence separately from LCD macro.

○RESET Sync

LCD_RESETSYNC synchronizes (2 steps flip-flop) a RSTZ signal by each clock and supplies the module which moves by each clock with a reset signal.

○Frame Buffer Interface

LCD_FBIF is connected with MEMC macro and does a data lead from Direct Path. This is synchronous with LCD_CCLK.

○FIFO Control

Data writing in to LCD built-in FIFO is performed, but LCD_FIFO_CONT sometimes reads from the occasion read from FBUF and IMC macro by an operation mode. It falls below FIFO space situation management and all kinds, and it's managed and auto-action shifting between terminal modes after Write Back execution is performed. This is synchronous with LCD_CLK.

○LCD Interface

LCD_LCDIF is connected with a LCD panel. The image data stocked in a data buffer is output in the outside LCD panel. More expansion resizing processing of Unpacking of image data and horizontal direction and change when being different in the input/output format, are performed. This is synchronous with LCLK.
The data for cursors supplied from Timing Generator is drawn.

○Data Buffer

LCD_FIFOWRAPPER has a FIFO memory for image data stocks built-in. A memory is 32 bits x 256 words of 2port SRAM, and writing in is synchronous with LCD_CLK, and is performed, and reading is synchronous with LCD_LCLK, and is performed.

CHAPTER 2 PIN FUNCTIONS

2.1 LCD Interface Pins

Pin Name	I/O	After Reset	Function	Alternate Function Pin
LCD_PXCLK	Output	0	Pixel clock	GIO_P50
LCD_R[5:0]	Output	0	Red data	GIO_P[56:51]
LCD_G[5:0]	Output	0	Green data	GIO_P[62:57]
LCD_B[5:0]	Output	0	Blue data	GIO_P[68:63]
LCD_HSYNC	Output	0	Horizontal synchronization	GIO_P69
LCD_VSYNC	Output	0	Vertical synchronization	GIO_P70
LCD_ENABLE	Output	0	Data enable	GIO_P71

CHAPTER 3 REGISTERS

3.1 Registers

Base address: 4027_0000H

Remark Among addresses 4027_0000H to 4027_FFFCH, the addresses not listed in the following tables are reserved. Do not access reserved registers. An undefined value is returned for a read access.

Registers marked with ○ in the Frame Sync column are two-stage registers with which settings made in the registers are latched to the macro and take effect when the frame start signal immediately after the setting change is received; that is, the beginning of a frame processed in the LCD module and it is independent from the VSYNC pin operation. The timing is the same as occurrence of a frame interrupt.

Registers marked with × are registers with which setting changes made in the register take effect immediately. Changing the settings during display output is prohibited.

(1/2)

Address	Register Name	Symbol	R/W	Frame Sync	After Reset
0000H	Control register	LCD_CONTROL	R/W	×	0000_0000H
0004H	Simple QoS setting register	LCD_QOS	R/W	×	0000_0000H
0008H	Data request cycle register	LCD_DATAREQ	R/W	×	0000_0000H
0010H	Display register	LCD_LCDOUT	R/W	○	0000_0000H
0014H	Access bus select register	LCD_BUSSEL	R/W	○	0000_0000H
0018H	Status register	LCD_STATUS	R	○	0000_0000H
001CH	Fixed-color output value register	LCD_BACKCOLOR	R/W	○	0000_0000H
0020H	Display area address register	LCD_AREAADR	R/W	○	0000_0000H
0024H	Address addition value register	LCD_HOFFSET	R/W	○	0000_0000H
0028H	Input format register	LCD_IFORMAT	R/W	○	0000_0000H
002CH	Simple resize register	LCD_RESIZE	R/W	○	0000_0000H
0030H	Horizontal direction total register	LCD_HTOTAL	R/W	×	0000_0000H
0034H	Horizontal direction display area register	LCD_HAREA	R/W	×	0000_0000H
0038H	Horizontal synchronization edge 1 register	LCD_HEDGE1	R/W	×	0000_0000H
003CH	Horizontal synchronization edge 2 register	LCD_HEDGE2	R/W	×	0000_0000H
0040H	Vertical direction total register	LCD_VTOTAL	R/W	×	0000_0000H
0044H	Vertical direction display area register	LCD_VAREA	R/W	×	0000_0000H
0048H	Vertical synchronization edge 1 register	LCD_VEDGE1	R/W	×	0000_0000H
004CH	Vertical synchronization edge 2 register	LCD_VEDGE2	R/W	×	0000_0000H
0050H-005CH	Reserved	–	–	–	–

(2/2)

Address	Register Name	Symbol	R/W	Frame Sync	After Reset
0060H	Interrupt status register	LCD_INTSTATUS	R	×	0000_0000H
0064H	Interrupt raw status register	LCD_INTRAWSTATUS	R	×	0000_0000H
0068H	Interrupt enable set register	LCD_INTENSET	R/W	×	0000_0000H
006CH	Interrupt enable clear register	LCD_INTENCLR	W	×	0000_0000H
0070H	Interrupt source clear register	LCD_INTFFCLR	W	×	0000_0000H
0074H	Frame count interrupt setting register	LCD_FRAMECOUNT	R/W	×	0000_0000H

3.2 Register Functions

3.2.1 Control register

This register (LCD_CONTROL:4027_0000H) controls the basic LCD controller operation.

Changing the settings during LCD controller operation is prohibited.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved			OFORMAT	CLKPOL	HPOL	VPOL	ENPOL

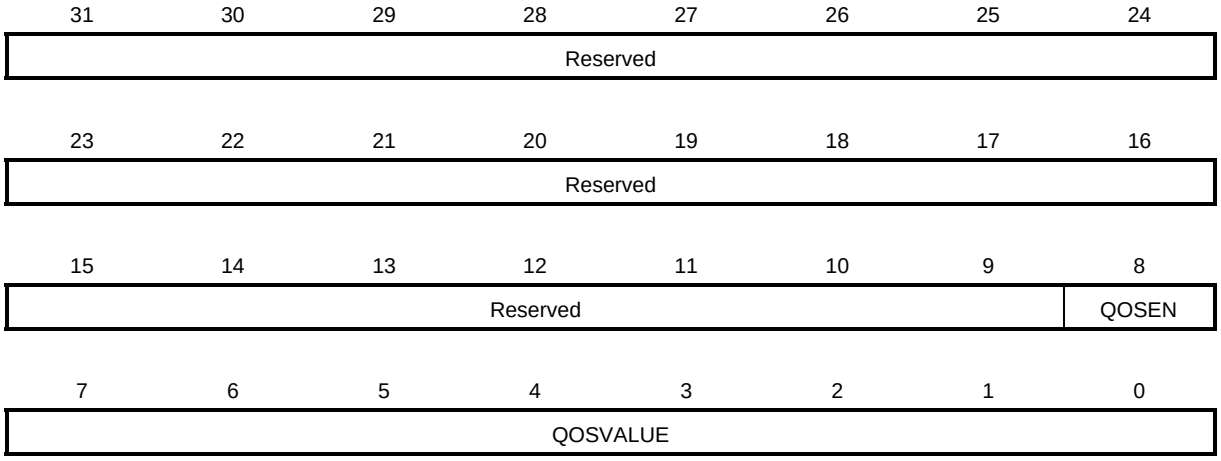
Name	R/W	Bit	After Reset	Function
Reserved	R	31:5	0	Reserved. When these bits are read, 0 is returned for each bit.
OFORMAT	R/W	4	0	Sets the format of data output from pins. For details, see **4.1.2 Format conversion**. 0: RGB666 1: RGB565
CLKPOL	R/W	3	0	Sets the LCD clock detection edge. For details, see **4.1.3 LCD clock**. 0: Rising edge 1: Falling edge
HPOL	R/W	2	0	Sets the polarity of horizontal synchronization signals. For details, see **4.1.5 Horizontal synchronization signal**.) 0: Positive logic 1: Negative logic Positive logic is assumed when a low-level pulse is output during a horizontal blanking interval.
VPOL	R/W	1	0	Sets the polarity of vertical synchronization signals. For details, see **4.1.6 Vertical synchronization signal**. 0: Positive logic 1: Negative logic Positive logic is assumed when a low level pulse is output during a vertical blanking interval.
ENPOL	R/W	0	0	Sets the active level of enable signals. For details, see **4.1.7 Enable signal**. 0: High 1: Low

3.2.2 Simple QoS setting register

This register (LCD_QOS: 4027_0004H) sets the simple QoS function of EM1.

The simple QoS function is used to prevent overrun and underrun from occurring in an image system function block.

When a QoS request is issued from an image system function block, the bus switch temporarily gives a higher priority for accesses from that QoS request function block, which reduces the access latency.

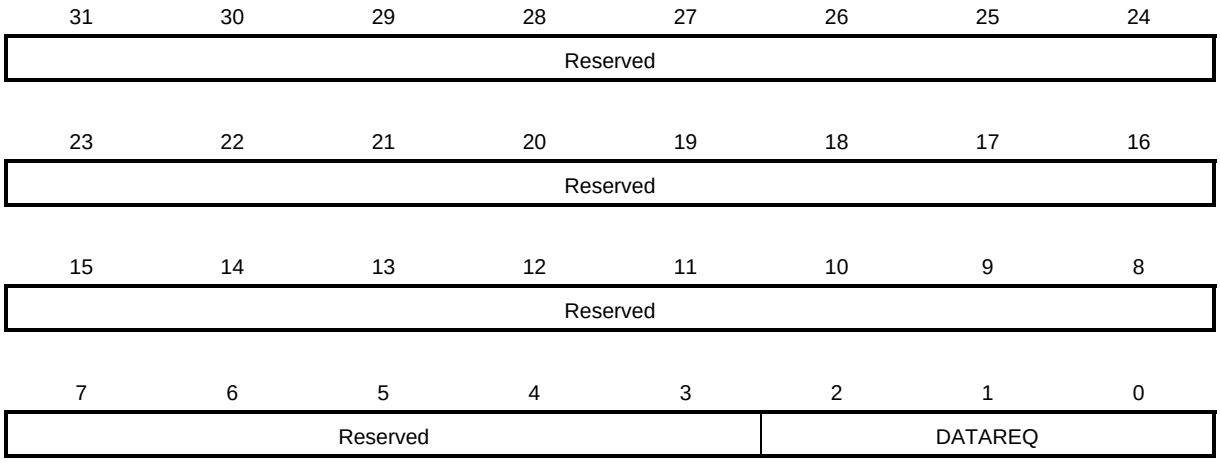


Name	R/W	Bit	After Reset	Function
Reserved	R	31:9	0	Reserved. When these bits are read, 0 is returned for each bit.
QOSEN	R/W	8	0	Sets whether to enable the simple QoS function. 0: Disable 1: Enable
QOSVALUE	R/W	7:0	0	A QoS request is issued when the free space in FIFO lowers the value set in this register.

3.2.3 Data request cycle register

This register (LCD_DATAREQ: 4027_0008H) sets the timing at which a request for reading data from a frame buffer is issued.

The set values are determined based on the available space in the data buffer in the LCD controller.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:3	0	Reserved. When these bits are read, 0 is returned for each bit.
DATAREQ	R/W	2:0	0	Sets the available FIFO space used for determining data request output timing. For details, see **4.2.5 Data request cycle setting**. 000: 96.8% (248 words) 001: 50.0% (128 words) 010: 37.5% (96 words) 011: 25.0% (64 words) 100: 18.8% (48 words) 101: 12.5% (32 words) 110: 6.25% (16 words) 111: 3.13% (8 words)

When using Direct Path, 8 words are read by once's data request. Therefore an original value of DATAREQ is 248 words which subtracted 8 from 256 with the FIFO size.

When using Local Bus, a data request to IMC uses this register set value.

3.2.4 Display register

This register (LCD_LCDOUT: 4027_0010H) is used to start data output to the LCD panel.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

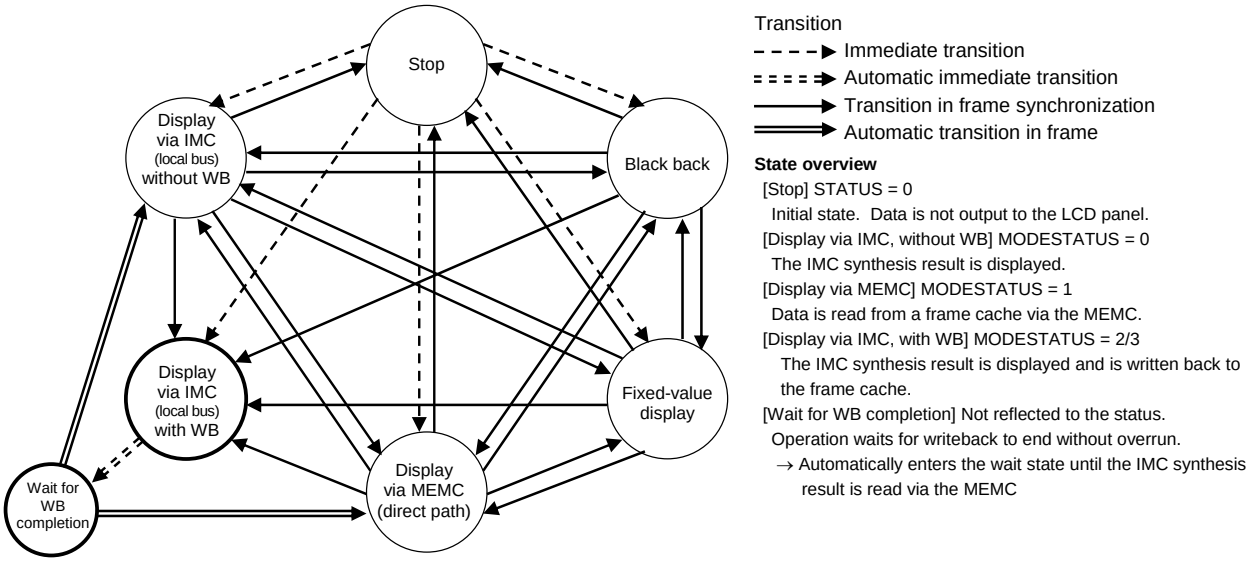
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							LCDOUT

Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
LCDOUT	R/W	0	0	Starts display on the LCD panel. 0: Stops display. 1: Starts display.

Startup (LCDOUT = 1) takes effect immediately, but stop (LCDOUT = 0) takes effect in frame synchronization. Up to one frame period may be required from issuing of a stop request to the actual stop. The timing at which the LCD display actually stops can be checked by detecting a display stop interrupt.

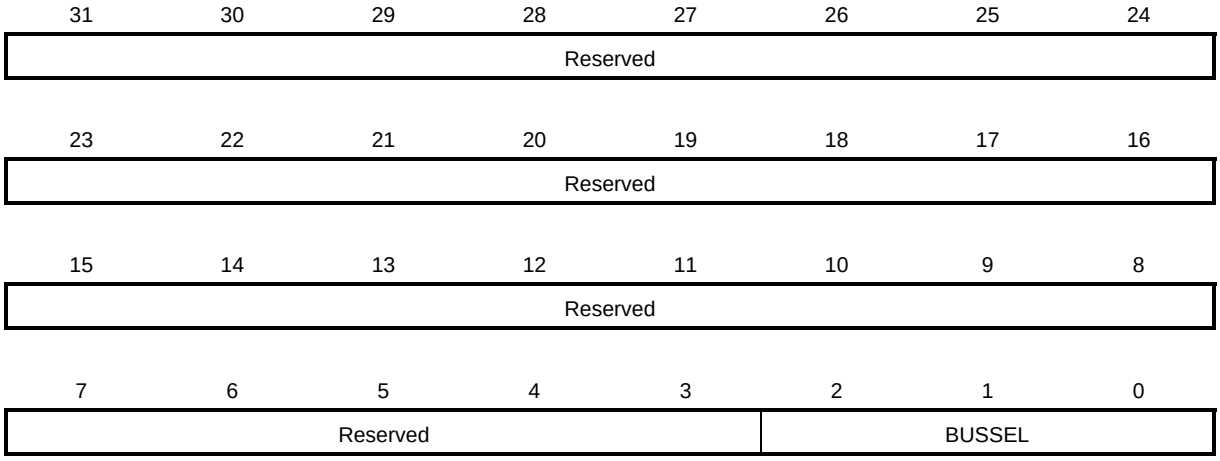
Figure 3-1. Status Transition



3.2.5 Access bus select register

This register (LCD_BUSSEL: 4027_0014H) switches the operation modes - normal operation mode in which data is displayed on the LCD via the IMC, or VGA standby mode on the MEMC via the Direct path or the mode in which fixed values are output for display.

Mode transition triggered by setting this register is performed in frame synchronization. The values set to the BUSSEL bit take effect at the next vertical synchronization interrupt, and are reflected in the MODESTATUS bit described later.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:3	0	Reserved. When these bits are read, 0 is returned for each bit.
BUSSEL	R/W	2:0	0	Sets the LCD controller operation mode. 000: Local bus between IMC and LCD controller (without WB) 001: Direct path between MEMC and LCD controller. 010: Local bus + WB. Waits for WB completion and automatically switches to local bus mode (without WB). 011: Local bus + WB. Waits for WB completion and automatically switches to Direct Path. 100: Black back display mode 101: Fixed-value display mode (RGB values are set with the LCD_BACKCOLOR register.) 110, 111: Setting prohibited

When the BUSSEL bit is set to 2 or 3, the LCD controller issues a data request to the IMC, at the same time as issuing a WB request. When WB operation requested here completes, the local bus (without WB) (when BUSSEL = 2) , Direct path (when BUSSEL = 3) is automatically selected for the next frame transfer.

If the WB operation fails (IMC buffer overrun), the LCD controller again issues a data request and a WB request to the IMC at the next frame.

For details on the BUSSEL setting and transition of internal states, see エラー! 参照元が見つかりません。.

3.2.6 Status register

This register (LCD_STATUS: 4027_0018H) indicates the LCD controller operating status. The LCD controller status can be checked by polling this register. The LCD controller status in a frame is reflected when a frame interrupt occurs.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved					MODESTATUS		

7	6	5	4	3	2	1	0
Reserved						STATUS	

Name	R/W	Bit	After Reset	Function
Reserved	R	31:11	0	Reserved. When these bits are read, 0 is returned for each bit.
MODESTATUS	R	10:8	0	Indicates the LCD controller operating status. (Updated upon a frame synchronization interrupt.) 000: Operating in local bus (without WB) between IMC and LCD controller. 001: Operating in local bus between MEMC and Direct path 010: WB has performed in local bus and waiting for WB completion. Following WB completion, the LCD controller automatically enters operation in local bus mode. 011: WB has performed in local bus and waiting for WB completion. The frame following WB completion is automatically set to 001. 100: Operating in black back display mode. 101: Operating in fixed-value display mode (RGB values are set with the LCD_BACKCOLOR register.) 110, 111: –
Reserved	R	7:1	0	Reserved. When these bits are read, 0 is returned for each bit.
STATUS	R	0	0	Indicates the LCD status. 0: LCD display is off. 1: LCD display is on.

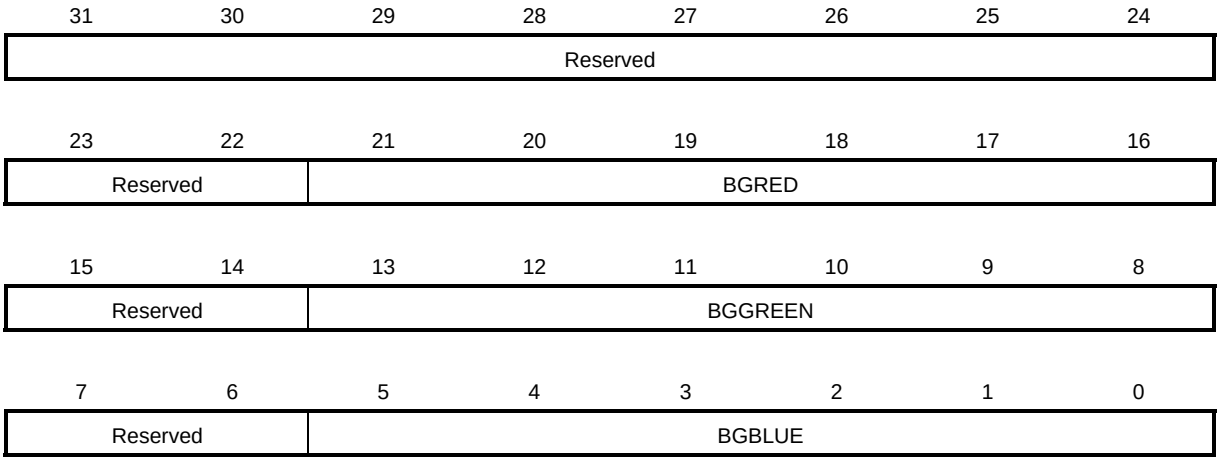
In black back display mode and fixed-value display mode, the LCD controller can operate individually without using the IMC or MEMC, because pixel data is generated in the LCD controller.

3.2.7 Fixed-color output value register

When the fixed-color display mode (BUSSEL = 5) is set in the access bus select register (LCD_BUSSEL), the LCD controller does not read data from a frame buffer but outputs fixed-value data to the LCD panel.

This register (LCD_BACKCOLOR: 4027_001CH) sets the fixed values for this mode.

The set values are captured to the circuit at the beginning of reception of a frame.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:22	0	Reserved. When these bits are read, 0 is returned for each bit.
BGRED	R/W	21:16	0	Sets the value of red output by the LCD controller in fixed-color display mode.
Reserved	R	15:14	0	Reserved. When these bits are read, 0 is returned for each bit.
BGGREEN	R/W	13:8	0	Sets the value of green output by the LCD controller in fixed-color display mode.
Reserved	R	7:6	0	Reserved. When these bits are read, 0 is returned for each bit.
BGBLUE	R/W	5:0	0	Sets the value of blue output by the LCD controller in fixed-color display mode.

When RGB565 is set with the OFORMAT bit of the control register (LCD_CONTROL), the higher 5 bits of the values set to the BGRED and BGBLUE bits are selected and output to the higher 5 bits of the LCD_R and LCD_B pins.

When the BG layer is set to fixed-color display mode (IMC_BG_FORMAT register = 2) in the IMC macro, the RGB values set in this register are used.

When this register is read, the values that become valid at the next frame (first-stage values) are read.

3.2.8 Display area address register

This register (LCD_AREAADR: 4027_0020H) sets the starting address of frame buffer.

The frame buffer set in this register is used in the direct path mode. The setting is also used for the buffer for white back, when the IMC macro is operating in LCD-synchronous mode. This is a frame-synchronous register and its set values take effect upon reception of a frame start signal.

31	30	29	28	27	26	25	24
AREAADR							

23	22	21	20	19	18	17	16
AREAADR							

15	14	13	12	11	10	9	8
AREAADR							

7	6	5	4	3	2	1	0
AREAADR						0	0

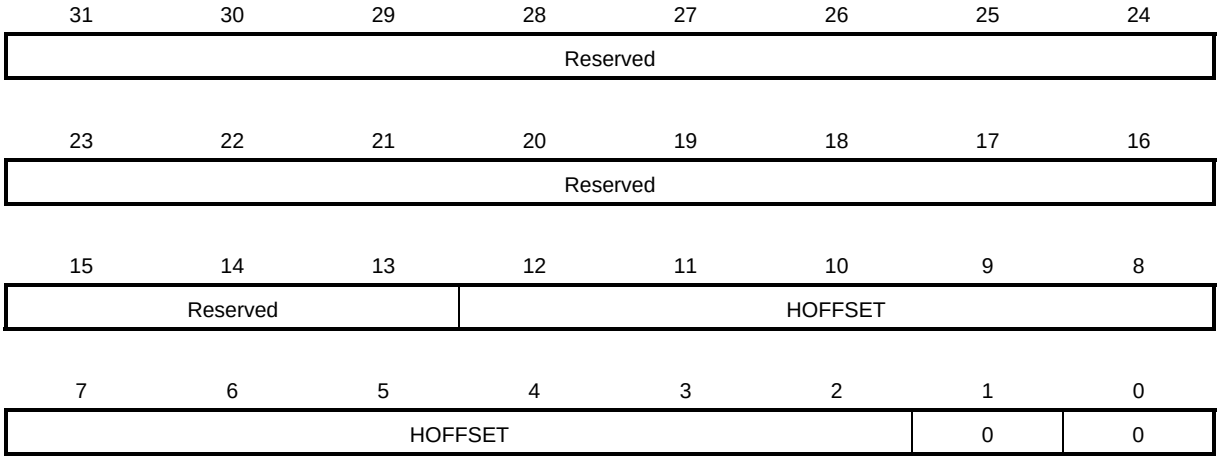
Name	R/W	Bit	After Reset	Function
AREAADR	R/W	31:2	0	Sets the starting address of frame buffer. Set the address using the byte address of 32-bit boundary. For details, see **4.2.1 Frame buffer**.
–	R	1:0	0	Fixed to 0. When these bits are read, 0 is returned for each bit.

When this register is read, the values that become valid at the next frame (first-stage values) are read.

3.2.9 Address addition value register

This register (LCD_HOFFSET: 4027_0024H) sets the total byte count in the horizontal direction in a frame buffer area.

The frame buffer set in this register is used in the direct path mode. The setting is also used for the buffer for white back, when the IMC macro is operating in LCD-synchronous mode. This is a frame-synchronous register and its set values take effect upon reception of a frame start signal.



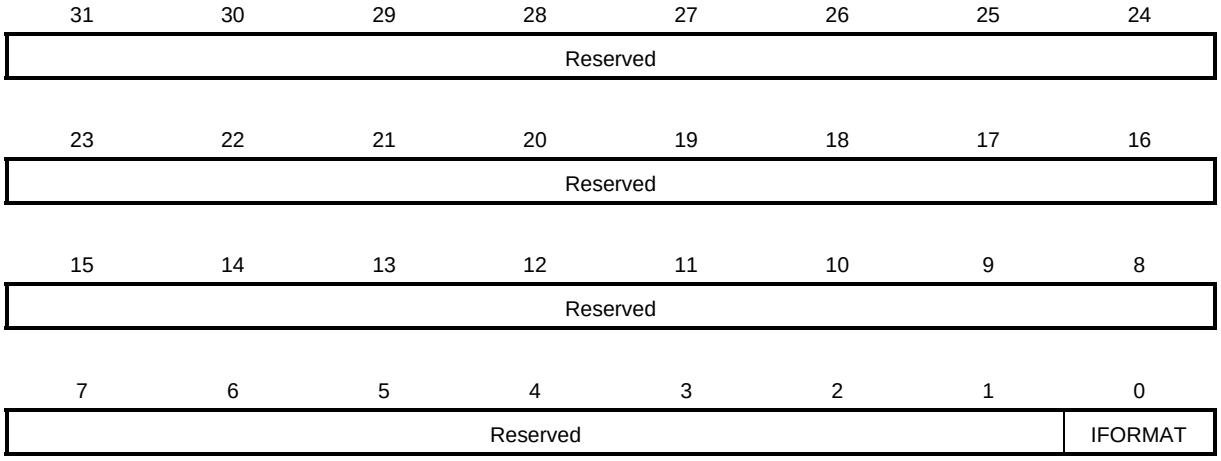
Name	R/W	Bit	After Reset	Function
Reserved	R	31:13	0	Reserved. When these bits are read, 0 is returned for each bit.
HOFFSET	R/W	12:0	0	Sets the total byte count in the horizontal direction in a frame buffer area. (The lower 2 bits are fixed to 0.)

When this register is read, the values that become valid at the next frame (first-stage values) are read.

3.2.10 Input format register

This register (LCD_IFORMAT: 4027_0028H) specifies the image format in a frame buffer area.

The format set in this register is referenced from the IMC macro and used as the output format in the IMC macro. This is a frame-synchronous register and its set values take effect upon reception of a frame start signal.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
IFORMAT	R/W	0	0	Sets the input data format. For details, see **4.1.2 Format conversion**. 0: RGB666 1: RGB565

When this register is read, the values that become valid at the next frame (first-stage values) are read.

When changing the values of this register during operation, the settings related to frame buffers (start address and address addition value) must also be changed.

3.2.11 Simple resize register

This register (LCD_RESIZE: 4027_002CH) is expanded double inside the LCD macro and indicated setting is performed. When the data read from a buffer is output to LCD interface.

Only when reading from Direct Path, it's effective. It's ignored by the time of Local Bus mode through IMC.

The set value is just after start-of-frame timing for a V synchronous register, and this becomes effective.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved							RESIZE

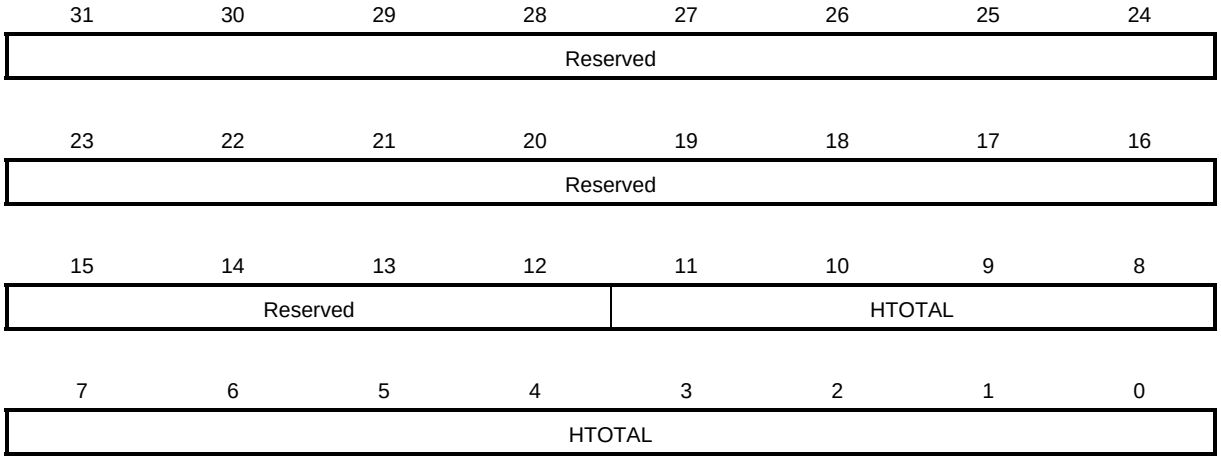
Name	R/W	Bit	After Reset	Function
Reserved	R	31:1	0	Reserved. When these bits are read, 0 is returned for each bit.
RESIZE	R/W	0	0	The simple resizing function is made effective.. 0: Resize invalid 1: Resize effective

When this register is read, the values that become valid at the next frame (first-stage values) are read.

Expansion processing of horizontal direction is performed inside the LCD macro, but 2 lines are to read the same linear data from a frame buffer, and the verticalness direction is achieved. LCD macro will be the read amount of data half as a result.

3.2.12 Horizontal direction total register

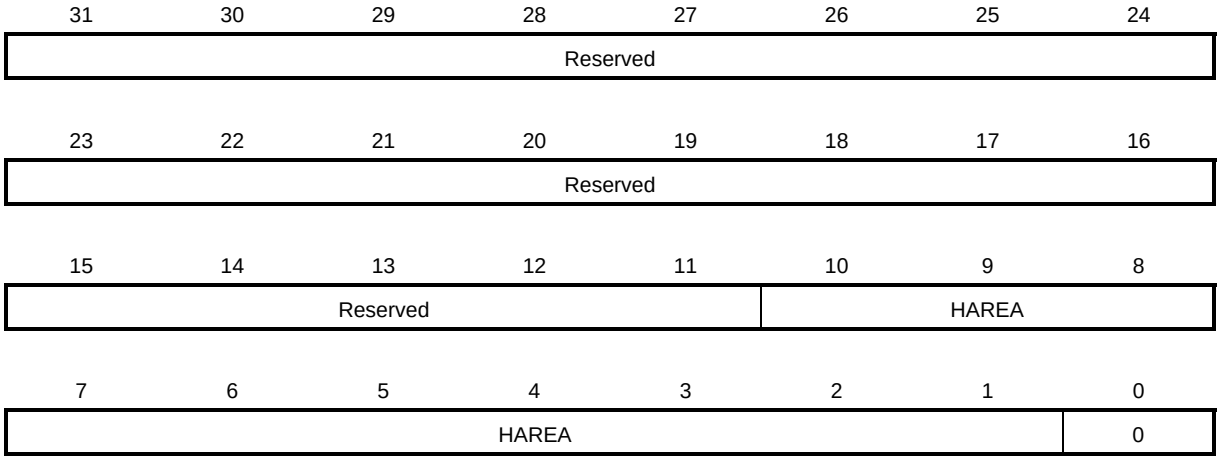
This register (LCD_HTOTAL: 4027_0030H) sets the number of pixel clock cycles (HSYNC cycles) in the horizontal direction.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:12	0	Reserved. When these bits are read, 0 is returned for each bit.
HTOTAL	R/W	11:0	0	Sets the number of pixel clock cycles in the horizontal direction. For details, see **4.1.4 Display area, and horizontal and vertical blanks**.

3.2.13 Horizontal direction display area register

This register (LCD_HAREA: 4027_0034H) sets the number of display pixels in the horizontal direction, in pixel units.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:11	0	Reserved. When these bits are read, 0 is returned for each bit.
HAREA	R/W	10:0	0	Sets the number of display pixels in the horizontal direction. (The lowest bit is fixed to 0 (2-pixel units).) For details, see **4.1.4 Display area, and horizontal and vertical blanks**.

3.2.14 Horizontal synchronization edge 1 register

This register (LCD_HEDGE1: 4027_0038H) sets the position of the first edge of a horizontal synchronization signal by the X coordinate (number of pixel clocks).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved				HEDGE1			

7	6	5	4	3	2	1	0
HEDGE1							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:12	0	Reserved. When these bits are read, 0 is returned for each bit.
HEDGE1	R/W	11:0	0	Sets the position of the first edge of a horizontal synchronization signal by the X coordinate. For details, see **4.1.5 Horizontal synchronization signal**.

3.2.15 Horizontal synchronization edge 2 register

This register (LCD_HEDGE2: 4027_003CH) sets the position of the second edge of a horizontal synchronization signal by the X coordinate (number of pixel clocks).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

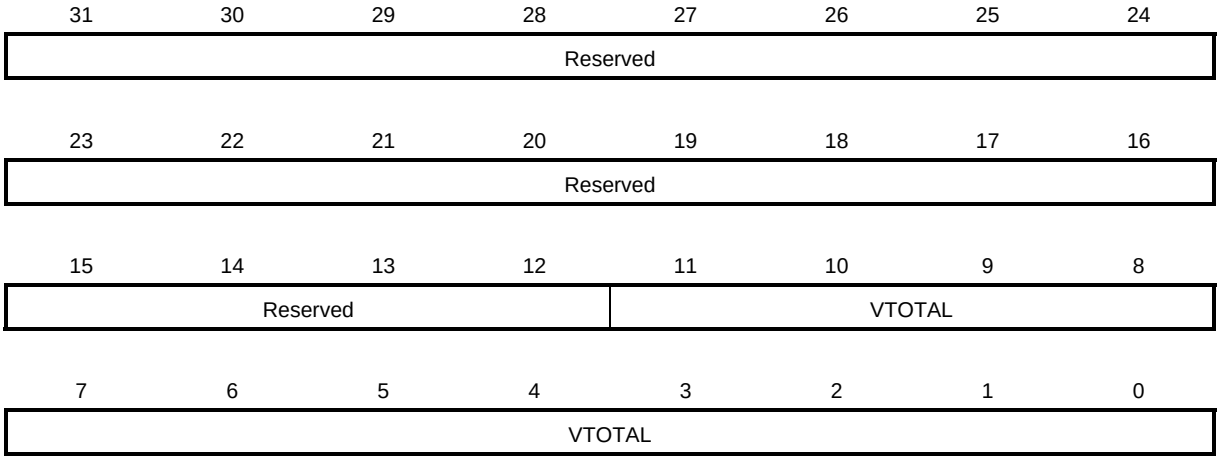
15	14	13	12	11	10	9	8
Reserved				HEDGE2			

7	6	5	4	3	2	1	0
HEDGE2							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:12	0	Reserved. When these bits are read, 0 is returned for each bit.
HEDGE2	R/W	11:0	0	Sets the position of the second edge of a horizontal synchronization signal by the X coordinate. For details, see **4.1.5 Horizontal synchronization signal**.

3.2.16 Vertical direction total register

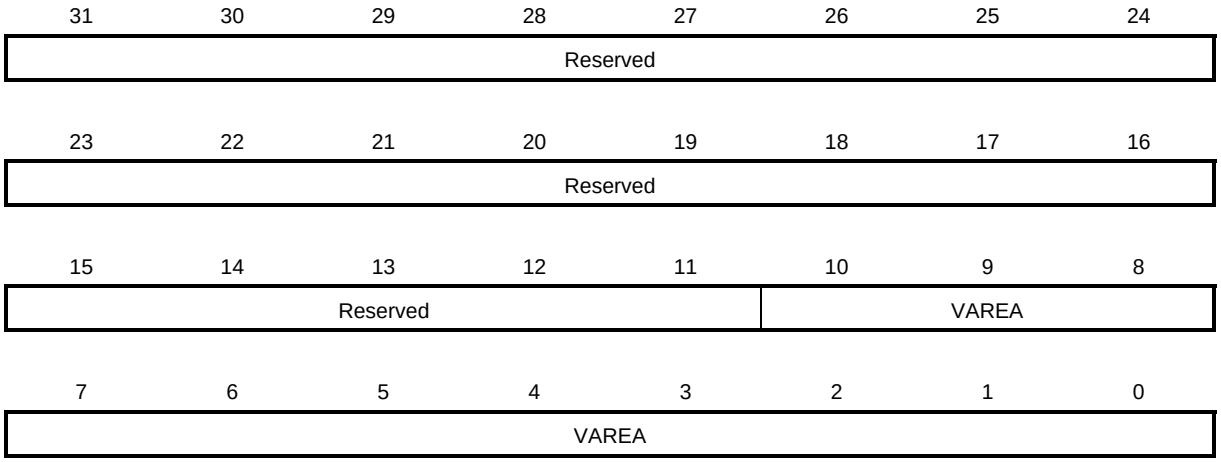
This register (LCD_VTOTAL: 4027_0040H) sets the total number of lines in the vertical direction (VSYNC cycles = HSYNC count).



Name	R/W	Bit	After Reset	Function
Reserved	R	31:12	0	Reserved. When these bits are read, 0 is returned for each bit.
VTOTAL	R/W	11:0	0	Sets the total number of lines in the vertical direction. For details, see **4.1.4 Display area, and horizontal and vertical blanks**.

3.2.17 Vertical direction display area register

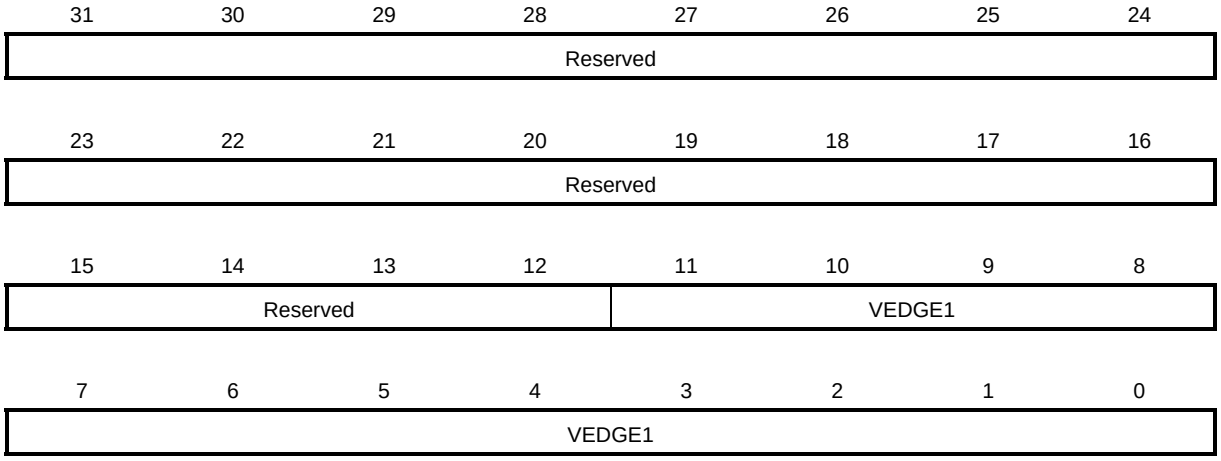
This register (LCD_VAREA: 4027_0044H) sets the number of display lines in the vertical direction.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:11	0	Reserved. When these bits are read, 0 is returned for each bit.
VAREA	R/W	10:0	0	Sets the number of display lines in the vertical direction. For details, see **4.1.4 Display area, and horizontal and vertical blanks**.

3.2.18 Vertical synchronization edge 1 register

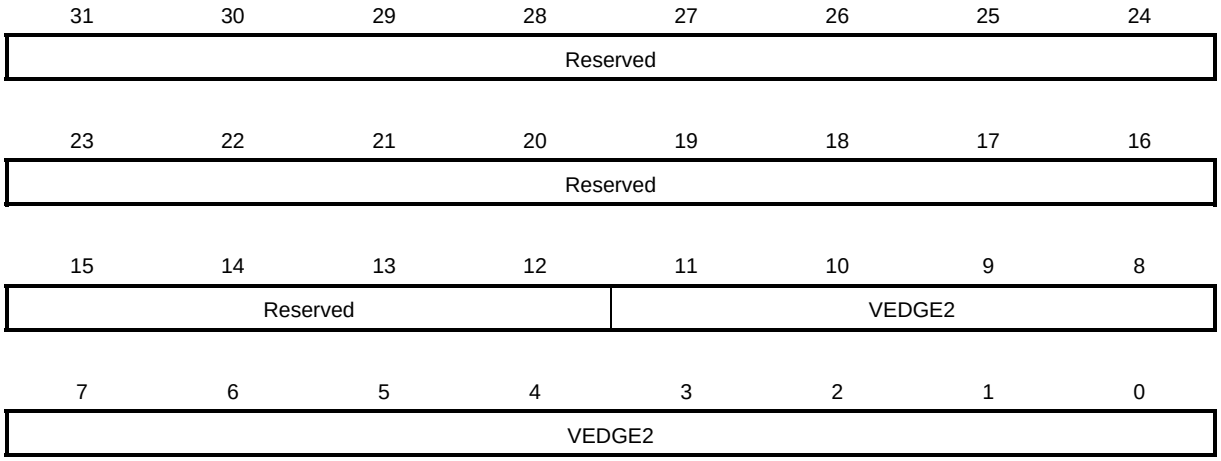
This register (LCD_VEDGE1: 4027_0048H) sets the position of the first edge of a vertical synchronization signal by the Y coordinate (HSYNC count).



Name	R/W	Bit	After Reset	Function
Reserved	R	31:12	0	Reserved. When these bits are read, 0 is returned for each bit.
VEDGE1	R/W	11:0	0	Sets the position of the first edge of a vertical synchronization signal by the Y coordinate. For details, see **4.1.6 Vertical synchronization signal**.

3.2.19 Vertical synchronization edge 2 register

This register (LCD_VEDGE2: 4027_004CH) sets the position of the second edge of a vertical synchronization signal by the Y coordinate.



Name	R/W	Bit	After Reset	Function
Reserved	R	31:12	0	Reserved. When these bits are read, 0 is returned for each bit.
VEDGE2	R/W	11:0	0	Sets the position of the second edge of a vertical synchronization signal by the Y coordinate. For details, see **4.1.6 Vertical synchronization signal**.

3.2.20 Interrupt setting registers

Interrupt setting registers set various interrupt parameters.

(1) Interrupt status register

This register (LCD_INTSTATUS: 4027_0060H) is a read-only register that indicates the statuses of interrupt sources. The statuses of the interrupt sources enabled with the interrupt enable set register can be read.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved			WBTRACE	FRMCOUNT	LCDSTOP	UNDERRUN	LCDVS

Name	R/W	Bit	After Reset	Function
Reserved	R	31:5	0	Reserved. When these bits are read, 0 is returned for each bit.
WBTRACE	R	4	0	Indicates the status of the VGA standby shift end interrupt.
FRMCOUNT	R	3	0	Indicates the status of the frame count interrupt.
LCDSTOP	R	2	0	Indicates the status of the display stop interrupt.
UNDERRUN	R	1	0	Indicates the status of the underrun interrupt.
LCDVS	R	0	0	Indicates the status of the LCD frame interrupt.

Remark 0: No interrupt source, 1: Interrupt source occurred

(2) Interrupt raw status register

This register (LCD_INTRAWSTATUS: 4027_0064H) is a read-only register that indicates the statuses of interrupt sources. An interrupt source is set to the register regardless of the settings of the interrupt enable set register and the interrupt enable clear register.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved			WBTRACE RAW	FRMCOUNT RAW	LCDSTOP RAW	UNDERRUN RAW	LCDVS RAW

Name	R/W	Bit	After Reset	Function
Reserved	R	31:5	0	Reserved. When these bits are read, 0 is returned for each bit.
WBTRACERAW	R	4	0	Indicates the status of the VGA standby shift end interrupt.
FRMCOUNTRAW	R	3	0	Indicates the status of the frame count interrupt.
LCDSTOPRAW	R	2	0	Indicates the status of a display stop interrupt.
UNDERRUNRAW	R	1	0	Indicates the status of an underrun interrupt.
LCDVSRAW	R	0	0	Indicates the status of an LCD frame interrupt.

Remark 0: No interrupt source, 1: Interrupt source occurred

(3) Interrupt enable set register

This register (LCD_INTENSET: 4027_0068H) enables issuance of interrupt requests. Only data of bits to which 1 is written is updated. When the bit corresponding to an interrupt source is set to 1 in this register, the interrupt source is set, the relevant interrupt request is issued and the corresponding bit of the interrupt status register is set to 1. If no bits are set in this register, no interrupt requests are issued even if the interrupt source is set, but the corresponding bit of the interrupt raw status register is set to 1.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved			WBTRACEEN	FRMCOUNTEN	LCDSTOPEN	UNDERRUNEN	LCDVSEN

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31:5	0	Reserved. When these bits are read, 0 is returned for each bit.
WBTRACEEN	R	4	0	Indicates whether issuance of VGA standby shift end interrupt requests is enabled. 0: Not enabled 1: Enabled
	W	4	–	Enables issuance of VGA standby shift end interrupt requests. 1: Cancels interrupt masking.
FRMCOUNTEN	R	3	0	Indicates whether issuance of frame count interrupt requests is enabled. 0: Not enabled 1: Enabled
	W	3	–	Enables issuance of frame count interrupt requests. 1: Cancels interrupt masking.
LCDSTOPEN	R	2	0	Indicates whether issuance of display stop interrupt requests is enabled. 0: Not enabled 1: Enabled
	W	2	–	Enables issuance of display stop interrupt requests. 1: Cancels interrupt masking.

(2/2)

Name	R/W	Bit	After Reset	Function
UNDERRUN	R	1	0	Indicates whether issuance of underrun interrupt requests is enabled. 0: Not enabled 1: Enabled
	W	1	–	Enables issuance of underrun interrupt requests. 1: Cancels interrupt masking.
LCDVSEN	R	0	0	Indicates whether issuance of LCD frame interrupt requests is enabled. 0: Not enabled 1: Enabled
	W	0	–	Enables issuance of LCD frame interrupt requests. 1: Cancels interrupt masking.

(4) Interrupt enable clear register

This register (LCD_INTENCLR: 4027_006CH) is a write-only register that masks issuance of interrupt requests. Only data of bits to which 1 is written is updated. When the bit corresponding to an interrupt source in this register is set to 1, no interrupt requests are issued even if the interrupt source is generated. The status of the corresponding bit in the interrupt status register also remains unchanged. If no bits are set in this register, an interrupt request is issued and the corresponding bit of the interrupt status register is set to 1 when the interrupt source is set.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved			WBTRACEMASK	FRMCOUNTMASK	LCDSTOPMASK	UNDERRUNMASK	LCDVSMASK

Name	R/W	Bit	After Reset	Function
Reserved	–	31:5	0	Reserved. When these bits are read, 0 is returned for each bit.
WBTRACEMASK	W	4	0	Disables issuance of VGA standby shift end interrupt requests. 1: Masks interrupts.
FRMCOUNTMASK	W	3	0	Disables issuance of frame count interrupt requests. 1: Masks interrupts
LCDSTOPMASK	W	2	0	Disables issuance of display stop interrupt requests. 1: Masks interrupts
UNDERRUNMASK	W	1	0	Disables issuance of underrun interrupt requests. 1: Masks interrupts
LCDVSMASK	W	0	0	Disables issuance of LCD frame interrupt requests. 1: Masks interrupts

(5) Interrupt source clear register

This register (LCD_INTFFCLR: 4027_0070H) is a write-only register that requests clearing of an interrupt source. Only data of bits to which 1 is written is updated. Setting the bit corresponding to an interrupt source to 1 clears the interrupt source.

If setting and clearing of an interrupt source are performed at the same time, setting takes precedence.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved			WBTRACE CLR	FRMCOUNT CLR	LCDSTOP CLR	UNDERRUN CLR	LCDVSCLR

Name	R/W	Bit	After Reset	Function
Reserved	–	31:5	0	Reserved. When these bits are read, 0 is returned for each bit.
WBTRACECLR	W	4	0	Requests clearing of a VGA standby shift end interrupt source. 1: Clearing an interrupt source.
FRMCOUNTCLR	W	3	0	Requests clearing of a frame count interrupt source. 1: Clearing an interrupt source.
LCDSTOPCLR	W	2	0	Requests clearing of a display stop interrupt source. 1: Clearing an interrupt source.
UNDERRUNCLR	W	1	0	Requests clearing of an underrun interrupt source. 1: Clearing an interrupt source.
LCDVSCLR	W	0	0	Requests clearing of an LCD frame interrupt source. 1: Clearing an interrupt source.

(6) Frame count interrupt setting register

This register (LCD_FRAMECOUNT: 4027_0074H) is used to perform various settings related to the frame count interrupt.

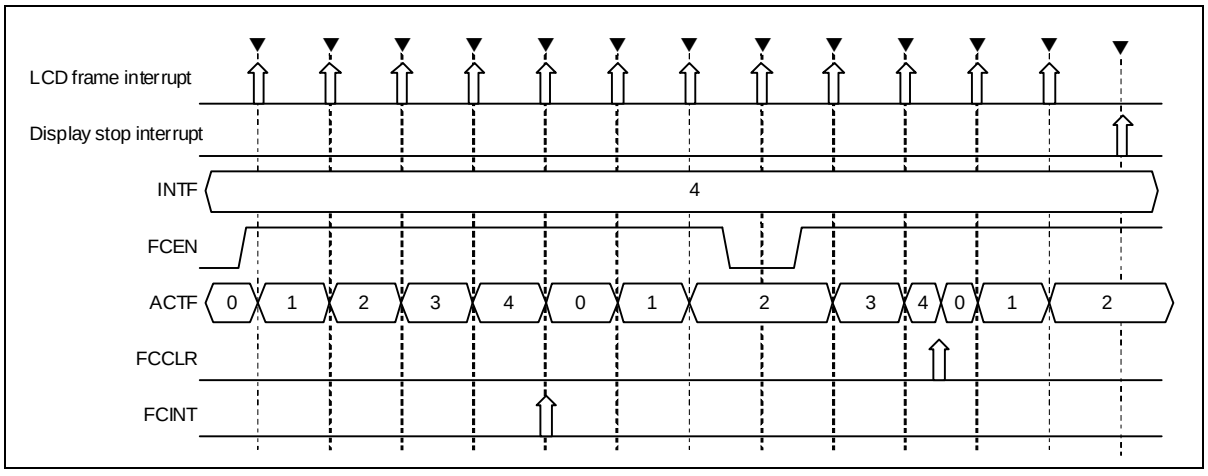
31	30	29	28	27	26	25	24
	Reserved						FCCLR

23	22	21	20	19	18	17	16
	Reserved						FCEN

15	14	13	12	11	10	9	8
ACTF							

7	6	5	4	3	2	1	0
INTF							

Name	R/W	Bit	After Reset	Function
Reserved	–	31:25	0	Reserved. When these bits are read, 0 is returned for each bit.
FCCLR	W	24	0	Clears the frame counter value. 0: Does not affect the setting. When this bit is read, 0 is returned. 1: Initializes the ACTF bit setting.
Reserved	–	23:17	0	Reserved. When these bits are read, 0 is returned for each bit.
FCEN	R/W	16	0	Sets the operation of the frame count function. 0: Stops 1: Starts operation
ACTF	R	15:8	0	Indicates the number of current frames being counted.
INTF	R/W	7:0	0	Sets the timer count threshold by which a frame count interrupt is issued.



When an LCD frame interrupt is issued while the FCEN bit is set to 1, the ACTF bit value is incremented. It is not incremented when a display stop interrupt is issued. If an LCD frame interrupt is issued when the values of the ACTF and INTF bits are the same, a frame count interrupt is issued and the ACTF bit is cleared to 0. The ACTF bit is also cleared to 0 when the FCCLR bit is set to 1.

CHAPTER 4 DESCRIPTION OF FUNCTIONS

4.1 LCD Panel Interface

4.1.1 Image data

The LCD controller supports an LCD panel in 16 bpp mode (65,536 colors) and 18 bpp mode (260,000 colors). RGB666 and RGB565 are switched by setting the OFORMAT bit of the control register (LCD_CONTROL).

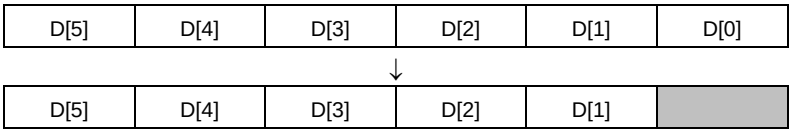
4.1.2 Format conversion

In the LCD controller, the format of data input (from the IMC) and output to an LCD panel can be set individually. Since the output data format is mainly determined in accordance with the LCD panel connected, setting of the output data format is assigned to the control register (LCD_CONTROL) (an immediately-reflected register, which is defined in the chapter of the IMC). Setting of the input data format is assigned to individual registers so as to enable switching in frame units.

If a different format is specified to input and output, the components of R and B are converted according to the following rules.

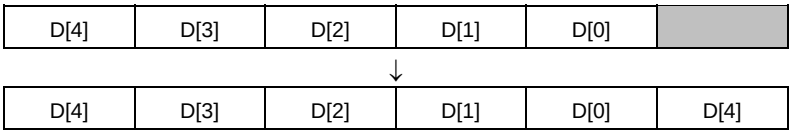
- **When the input format is RGB666 and output format is RGB565**

The LSB of R and B is discarded and scaled to be 5 bits.



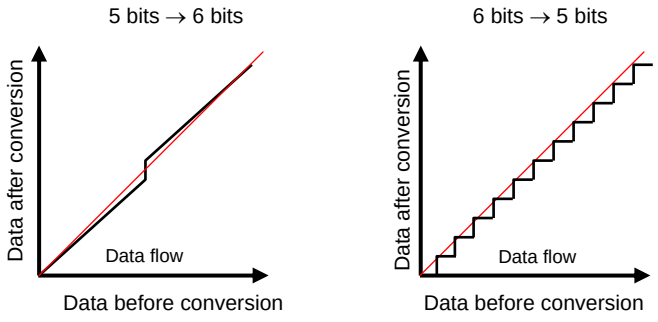
- **When the input format is RGB565 and output format is RGB666**

The MSB of R and B is added and scaled to be 6 bits.



The next figure shows format conversion processing. It just shows a conceptual diagram because the gradation varies between input and output.

Figure 4-1. Format Conversion Operation

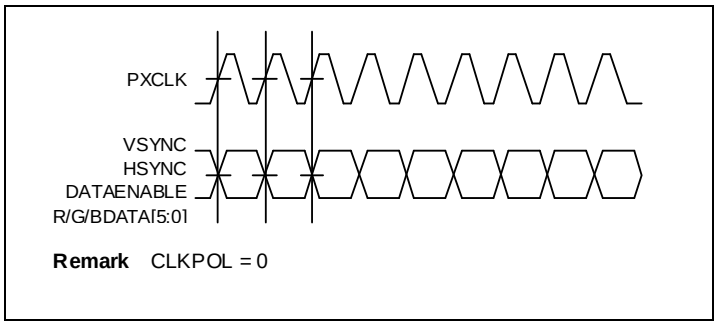


4.1.3 LCD clock

The phases of the output clock (PXCLK) and LCD panel interface signal lines (VSYNC, HSYNC, DATAENABLE or R/G/BDATA) can be selected. Use the CLKPOL bit of the control register for setting (0: LCD clock rising edge synchronization, 1: LCD clock falling edge synchronization).

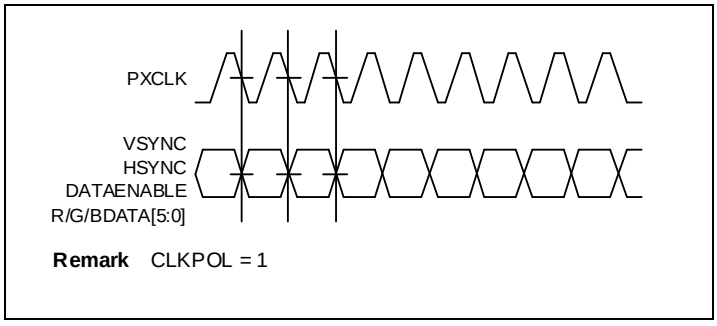
When the setting is changed, glitch noise may be applied to PXCLK, because all the function block internal circuits operate in synchronization with the rising edge and the setting of the CLKPOL bit and PXCLK are Ex-ORed and used as pin output. To switch the setting safely, first stop supplying LCD_LCLK in the ASMU macro and then change the CLKPOL bit setting in the LCD controller.

Figure 4-2. LCD Clock Rising Edge Synchronization



Remark CLKPOL = 0

Figure 4-3. LCD Clock Falling Edge Synchronization



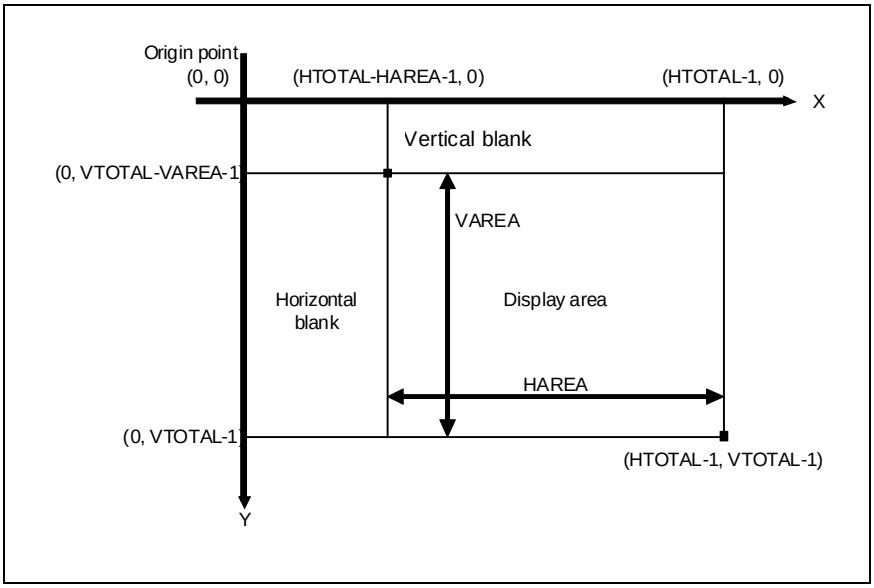
Remark CLKPOL = 1

4.1.4 Display area, and horizontal and vertical blanks

The LCD display areas and horizontal/vertical blanks are defined by using the lower right coordinate system, in pixel clock units. The value of the X coordinate increases as it moves to the right, and the value of the Y coordinate increases as it moves down. The origin point is the higher left (0, 0).

To set the square size in an LCD panel, use the HAREA and VAREA bits of the horizontal/vertical direction display area registers. The HTOTAL and VTOTAL bits of the horizontal/vertical direction total registers define the lower right corner of the square, including horizontal and vertical blanks (non-display area).

Figure 4-4. Display Area and Horizontal/Vertical Blanks



Define the parameters by setting the following bits of the relevant LCD controller registers.

Table 4-1. Parameters Related to Display Size

Register	Setting Bits
Horizontal direction total register	HTOTAL[11:0]
Horizontal direction display area register	HAREA[10:0]
Vertical direction total register	VTOTAL[11:0]
Vertical direction display area register	VAREA[10:0]

Caution Set the parameters so as to satisfy the following expressions.

1. HTOTAL > HAREA+4

2. VTOTAL > VAREA

Data is read from a frame buffer, starting from the origin point (0, 0) as the frame display start position. Pixel data is output to an LCD panel starting from the position of (HTOTAL – HAREA – 1, VTOTAL – VAREA – 1).

A buffer underrun is likely to occur if the period between these two points is too short. Keep the vertical blanking interval as long as possible.

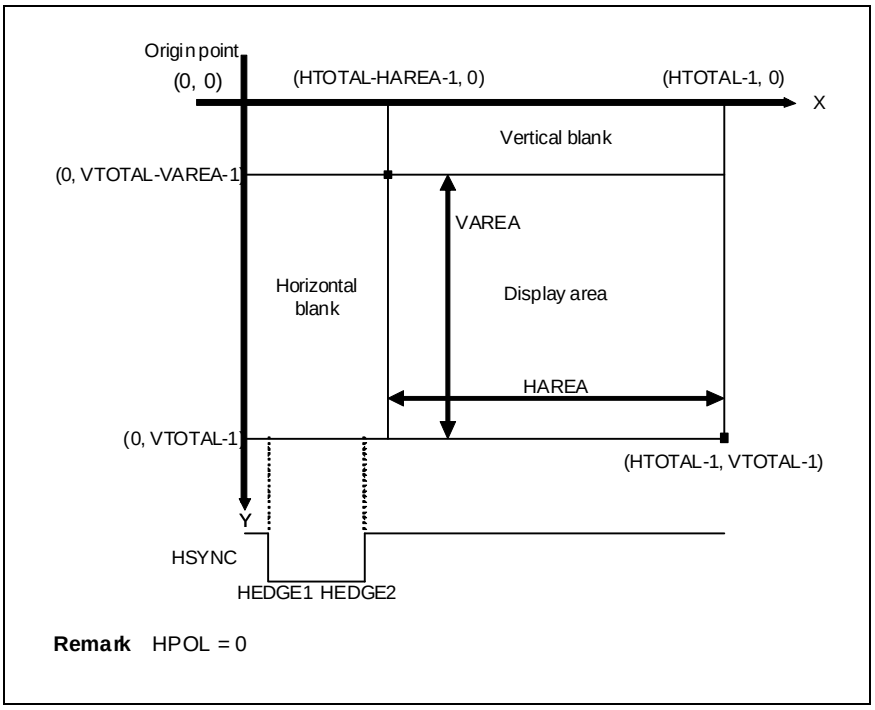
4.1.5 Horizontal synchronization signal

The horizontal synchronization signal is defined by using the lower right coordinate system, in LCD clock units. A pulse is generated by each line in the square specified with the origin point (0, 0) and (HTOTAL − 1, VTOTAL − 1).

The first edge of a horizontal synchronization signal is set by the HEDGE1 bit of the horizontal synchronization edge 1 register, and the second edge is set by the HEDGE2 bit of the horizontal synchronization edge 2 register.

To control the polarity of a horizontal synchronization signal, use the HPOL bit of the control register (LCD_CONTROL) (0: a signal level changes from high to low at the first edge, and changes from low to high at the second edge, 1: opposite setting to 0).

Figure 4-5. Horizontal Synchronizing Signal



Define the parameters by setting the following bits of the relevant LCD controller registers.

Table 4-2. Parameters Related to Horizontal Synchronization

Register	Setting Bits
Horizontal synchronization edge 1 register	HEDGE1[11:0]
Horizontal synchronization edge 2 register	HEDGE2[11:0]

Caution Set the parameters so as to satisfy the following expression.
HTOTAL > HEDGE2 > HEDGE1 ≥ 0

4.1.6 Vertical synchronization signal

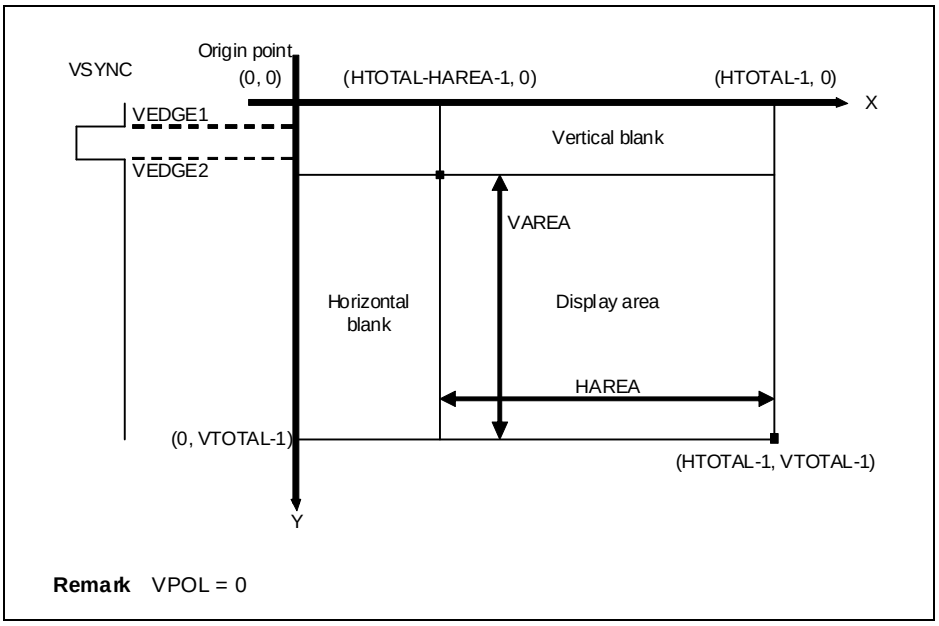
The vertical synchronization signal is defined by using the lower right coordinate system, in LCD clock units. A pulse is generated in the square.

The first edge of a vertical synchronization signal is set by the VEDGE1 bit of the vertical synchronization edge 1 register, and the second edge is set by the VEDGE2 bit of the vertical synchronization edge 2 register.

To control the polarity of a vertical synchronization signal, use the VPOL bit of the control register (LCD_CONTROL) (0: a signal level changes from high to low at the first edge, and changes from low to high at the second edge, 1: reverse of setting to 1).

The VSYNC level changes at the horizontal coordinate 0 in the following figure, regardless of the EDGE setting for HSYNC. When HEDGE is set to a value other than 0, therefore, note that VSYNC and HSYNC do not change at the same time.

Figure 4-6. Vertical Synchronization Signal



Remark VPOL = 0

Define the parameters by setting the following bits of the relevant LCD controller registers.

Table 4-3. Parameters Related to Vertical Synchronization

Register	Setting Bits
Vertical synchronization edge 1 register	VEDGE1[11:0]
Vertical synchronization edge 2 register	VEDGE2[11:0]

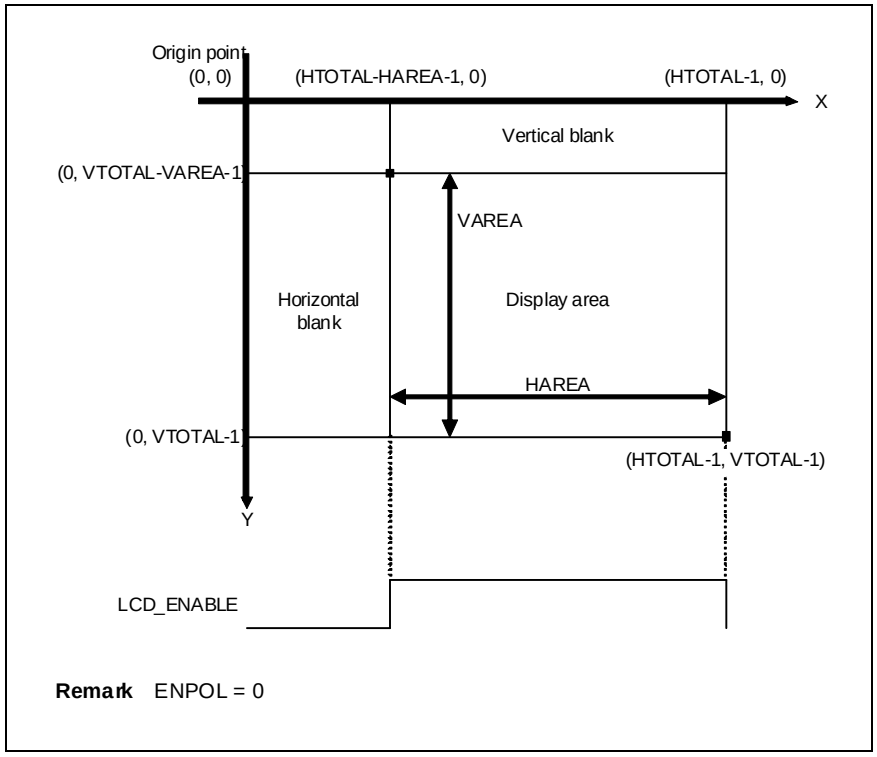
Caution Set the parameters so as to satisfy the following expression.

VTOTAL > VEDGE2 > VEDGE1 ≥ 0

4.1.7 Enable signal

An enable signal is set by the HAREA and VAREA bits of the horizontal/vertical direction display area registers, and goes into the active level in the display area. The active level can be controlled by the ENPOL bit of the control register (LCD_CONTROL) (0: active level of enable signal = high, 1: active level of enable signal = low).

Figure 4-7. Enable Signal



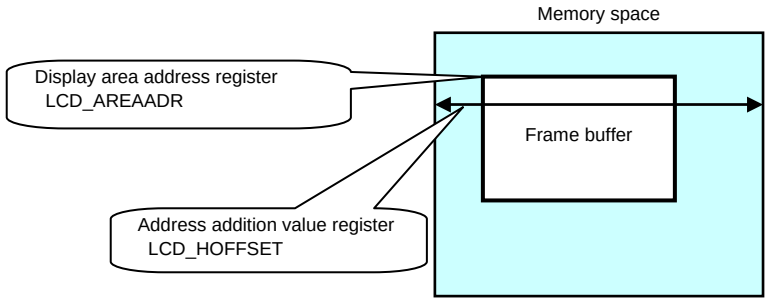
Remark ENPOL = 0

4.2 Frame Buffer and Data Buffer

4.2.1 Frame buffer

Buffer that stores a screen of image data is collectively called frame buffer. The LCD controller can set one screen. The display area address register is used to set the start address of the frame buffer, by any address. In addition, the horizontal direction size of the frame buffer area can be specified by the address addition value register (word boundary). Using this, the rectangle area cropped from the frame buffer mapped larger than the displayed image size can be output to an LCD panel.

Figure 4-8. Frame Buffer



The number of horizontal pixels of image data to be stored in the frame buffer can be set with the HAREA bit.
The volume of image data varies depending on the data format.

- When the input format is RGB565: 32 bytes with 16 pixels (8 words)
- When the input format is RGB666: 36 bytes with 16 pixels (9 words)

Therefore, set a value that satisfies the following conditions in the address addition value register.

- When the input format is RGB565: LCD_HOFFSET ≥ HAREA / 16 * 32
- When the input format is RGB666: LCD_HOFFSET ≥ HAREA / 16 * 36

Caution In the LCD controller in EM1, the value that can be specified as the number of horizontal pixels is defined as a multiple of 2. Consequently, the condition for setting the HOFFSET value changes as follows.

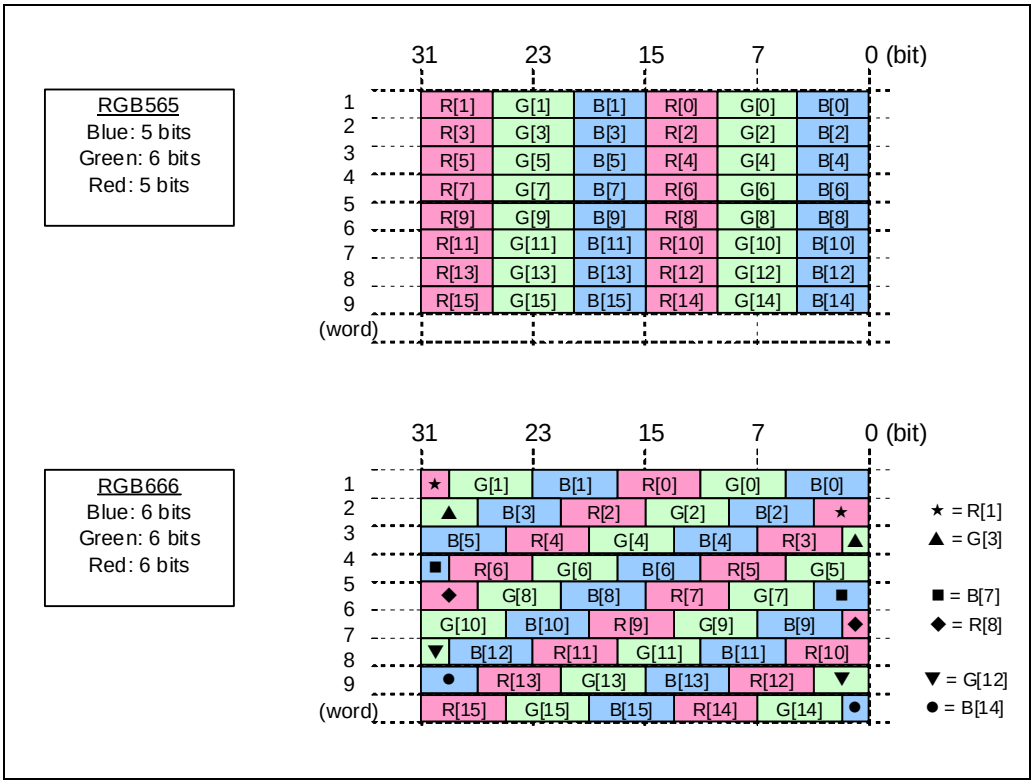
When the input format is RGB565: LCD_HOFFSET ≥HAREA / 2 * 4

In the case of RGB666, one pixel is composed of 18 bits. That is, data amount in one line is HAREA * 18 (bits). Divide the data amount in word units (32 bits), round up the fractional part, and set to HOFFSET a value of the obtained result or larger.

4.2.2 Frame buffer storage format

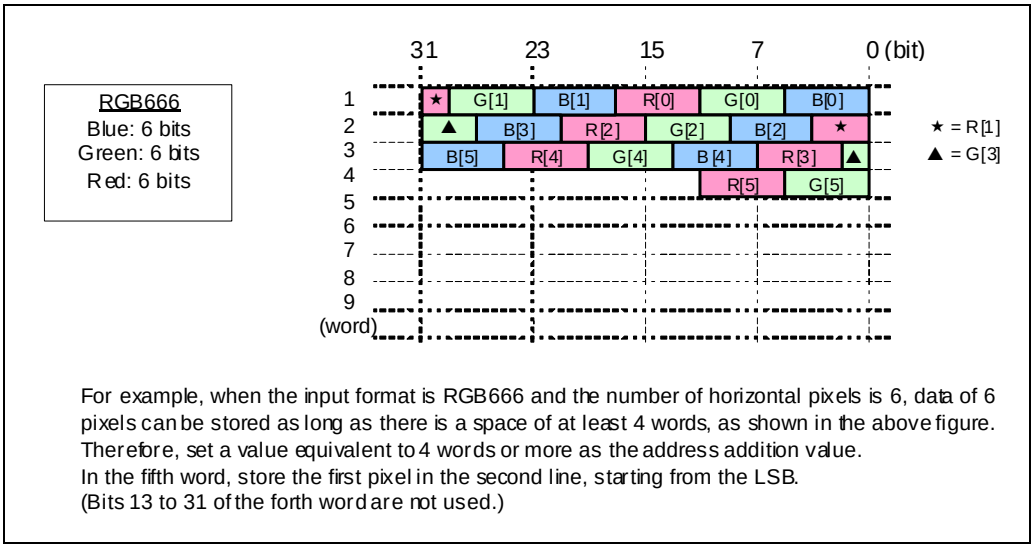
When storing image data in the frame buffer, fill the last word of the line thoroughly. Store RGB666 data in 36 bytes, and store RGB565 data in 32 bytes, in 16-pixel units.

Figure 4-9. Frame Buffer Storage Format



The following shows an example of memory storage when the number of horizontal pixels is not a multiple of 16.

Figure 4-10. When Number of Horizontal Pixels Is Not a Multiple of 16



4.2.3 Frame buffer access

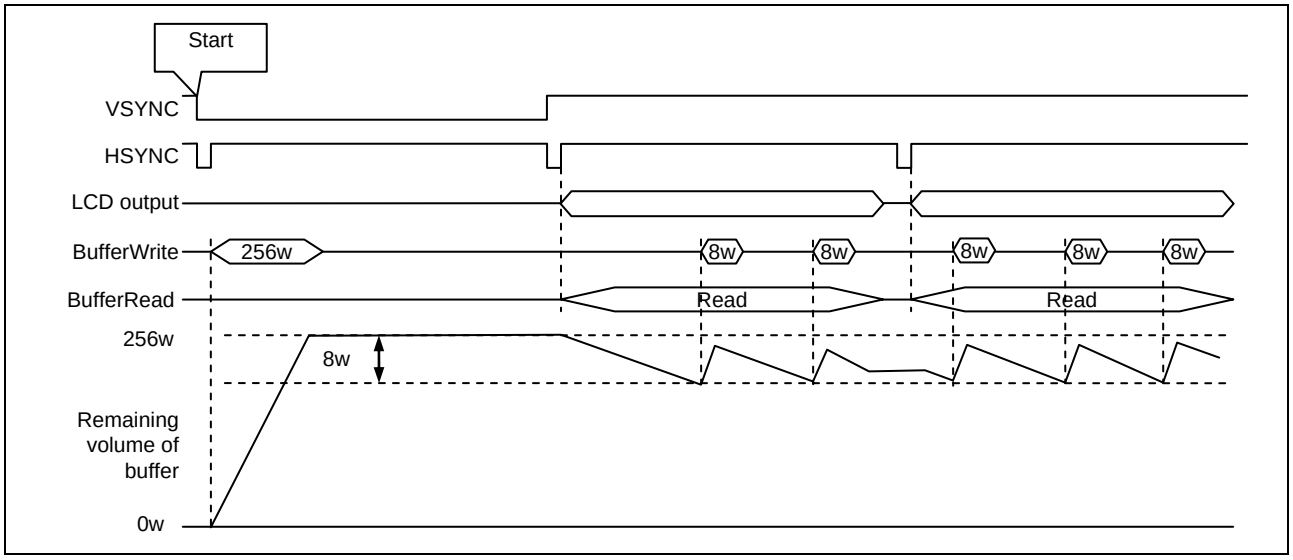
The BUSSEL bit setting is used to select the frame buffer access mode for accessing the local bus between the IMC and LCD and the direct path between the MEMC and LCD.

4.2.4 Data buffer

The data buffer is incorporated in the LCD controller and captures the image data read from the frame buffer. The data buffer consists of two ports (one read port and one write port) of 32 bits × 128 words and is used as a FIFO. When there is an available space of 8 words in the data buffer (when DATAREQ bit = 0 (initial value)), data is written to the write port of the data buffer via the frame buffer interface. The read port is used for reading out (LCD displaying) data from the LCD interface.

Figure 4-11 shows accessing the data buffer. First, image data is written to the data buffer via the frame buffer interface. Next, the LCD interface reads the image data from the area to which data was written via the frame buffer interface, and performs LCD display. After that, image data is written to the data buffer via the frame buffer interface when the data buffer has an available space of 8 words (when DATAREQ bit = 0 (initial value)). If the data buffer read speed via the LCD interface is faster than the buffer write speed, an underrun interrupt is generated.

Figure 4-11. Data Buffer Access



Caution If the data transfer rate is not fast enough in comparison with the LCD panel image refresh rate, the image data amount is insufficient, which results in a fatal image deterioration.
To avoid this, determine the clock cycle so that the following expression is sufficiently met.
1. Pixel clock frequency <<< Main clock frequency
(EM1 specification: PIXCLK = 6 to 50 MHz, LCD_CLK = 166 MHz)

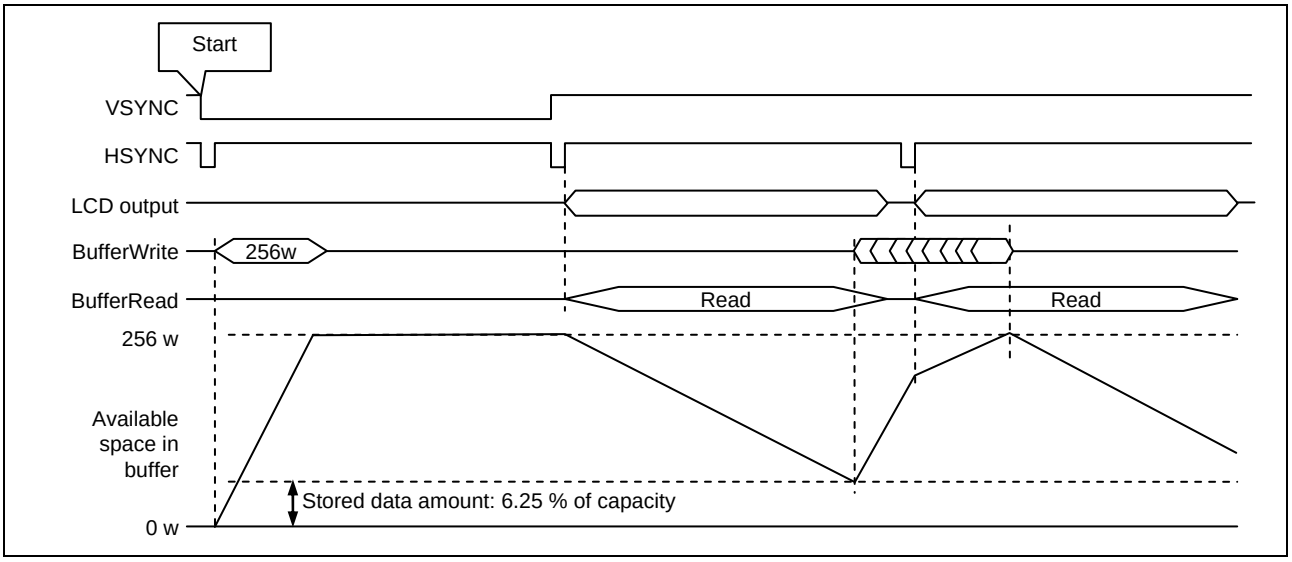
4.2.5 Data request cycle setting

When the frame buffer is mapped on SDRAM, usually data is written to the data buffer if there is an available space of 8 words. Due to this, SDRAM is frequently accessed and thus effective power management is disturbed. The data request cycle register (LCD_DATAREQ) can be used to concentrate issuance of SDRAM access requests in a specific period.

For example, when 6.25% is set in the LCD_DATAREQ register and the data stored in the data buffer decreases to 6.25% or less, data is continuously read from the frame buffer until the data buffer becomes full. Refer to the following figure for the operation. Note that a buffer underrun is more likely to occur if reading of data is stalled due to a certain cause.

Caution The following figure just shows a concept of operation and values in the figure does not necessarily match those of the actual operation.

Figure 4-12. Access When 6.25% Is Set in Data Request Cycle Setting Register

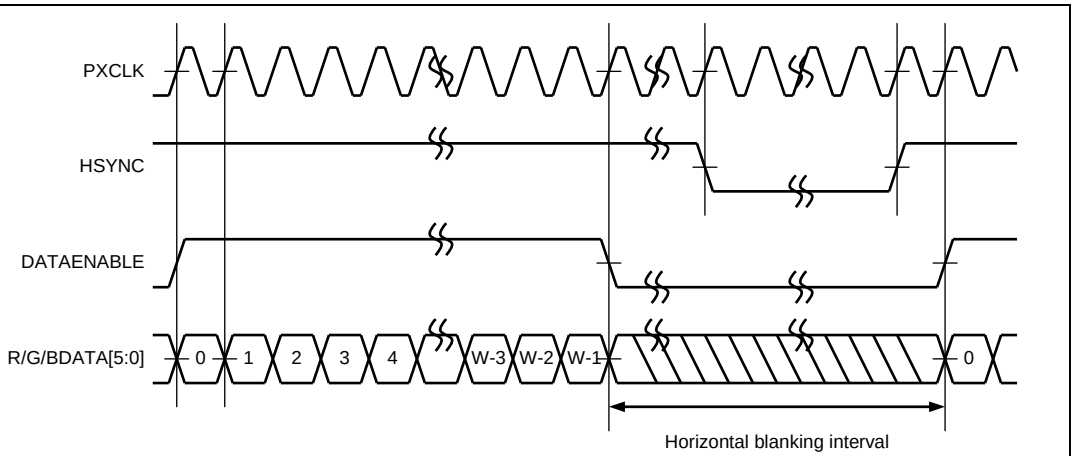


4.3 Operation Timing

4.3.1 LCD interface

Operation timing of the LCD interface is shown below.

Figure 4-13. LCD Panel (Horizontal Direction)

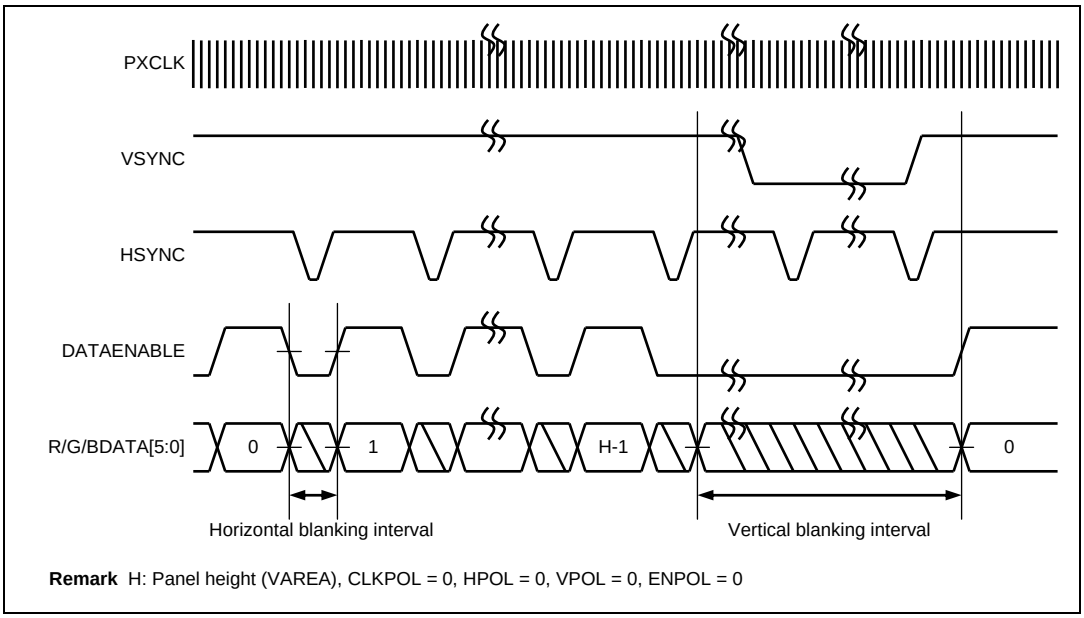


Remark W: Panel width (HAREA), CLKPOL = 0, HPOL = 0, ENPOL = 0

To set the detection edge (rising/falling) of an LCD clock, the polarity (positive/negative logic) of a horizontal synchronization signal and the active level (high/low) of an enable signal, use the CLKPOL, HPOL and ENPOL bits of the control register (LCD_CONTROL), respectively.

During the period in which the LCD_ENABLE signal is inactive (vertical/horizontal blanking interval), zeros are output as RGB data values.

Figure 4-14. LCD Panel (Vertical Direction)



Remark H: Panel height (VAREA), CLKPOL = 0, HPOL = 0, VPOL = 0, ENPOL = 0

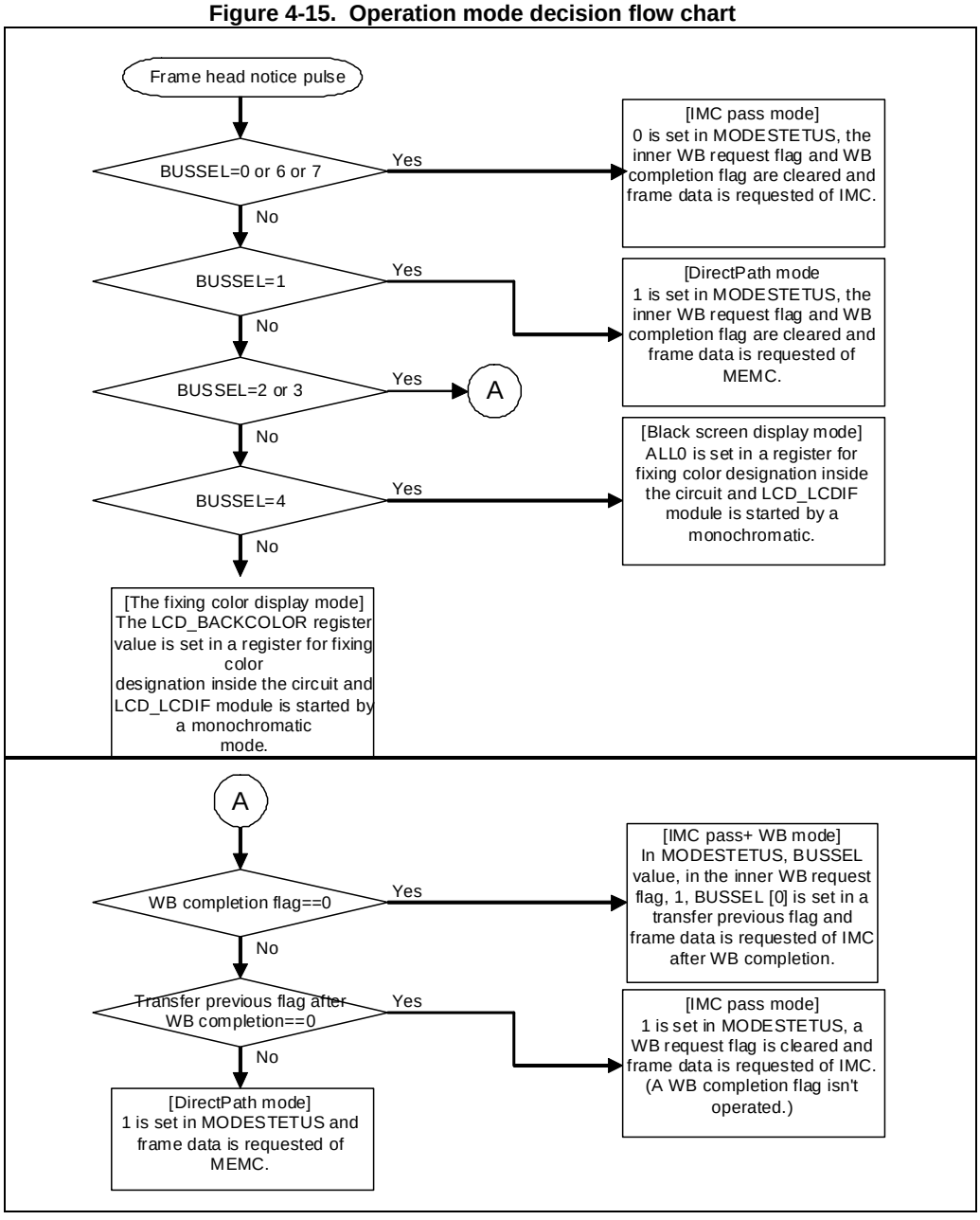
To set the detection edge (rising/falling) of an LCD clock, the polarity (positive logic/negative logic) of a horizontal synchronization signal, the polarity (positive logic/negative logic) of a vertical synchronization signal, and the active level (active high/active low) of an enable signal, use the CLKPOL, HPOL and ENPOL bits of the control register (LCD_CONTROL), respectively.

4.3.2 State transition every frame

LCD macro is the head of the frame LCD_CONTROL module generates (frame interrupt genesis timing), and LCD_FIFO_CONT module moves while choosing an operation mode from the LCD_BUSSEL register set value and the internal state as of it.

An operation mode decision flow chart is indicated below.

Figure 4-15. Operation mode decision flow chart



※ There is a possibility that the shifting between terminal modes which isn't intended occurs because a finite difference can't be recognized inside the circuit when switching BUSSEL from 2 to 3 as a careful point. The automatic transfer which is just as it is by some circumstances is canceled after Write Back request, once again, Write Back, please go through a frame of case and mode which is besides 2/3 once.

4.4 Clock and Reset

The LCD controller has three clock input lines: LCD_CLK (LCD_CCLK), LCD_PCLK, and LCD_LCLK. The LCD_LCLK frequency is 6 to 50 MHz, the LCD_PCLK frequency is 83 MHz, and the LCD_CLK frequency is 166 MHz. LCD_PCLK and LCD_CLK are synchronous, while LCD_LCLK is asynchronous. The source of LCD_CCLK and LCD_CLK is the same, but these clocks can be controlled individually via the LCD controller to save power.

4.5 Interrupt Sources

The LCD controller issues five types of interrupts. Control of each interrupt is assigned to each bit of the interrupt setting register. For details, refer to **Table 4-4**.

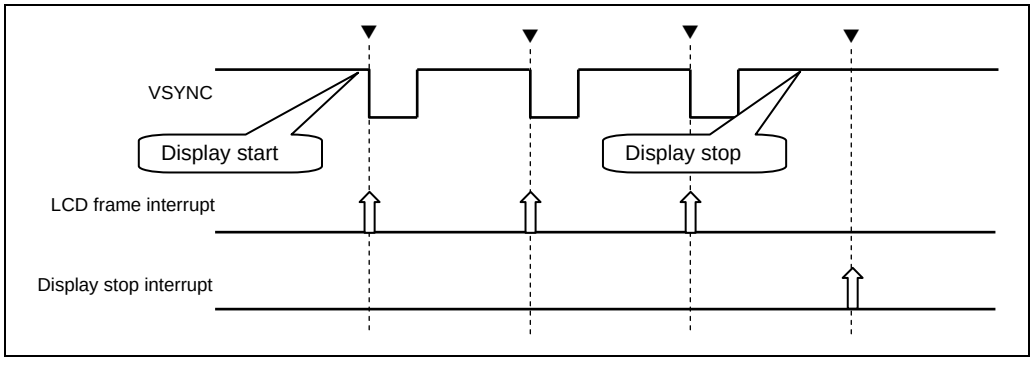
Table 4-4. Interrupts

Interrupt Name	Source	Bit Assignment
VGA standby shift end interrupt	This interrupt is issued to report the state that power to the L1 domain can be shut down after WB completion, when BUSSEL is set to 3.	4
Frame count interrupt	This interrupt is issued for each of the specified number of frames.	3
Display stop interrupt	This interrupt is issued if the display register value is 0 when frame display ends.	2
Underrun interrupt	This interrupt is issued when an underrun occurs in the LCD internal buffer.	1
LCD frame interrupt	This interrupt is issued when a frame display starts.	0

An LCD frame interrupt is issued when a frame display start signal is detected. Therefore, if the register setting is changed immediately after an LCD frame interrupt is issued, the change takes effect at the next frame.

An underrun interrupt is issued when a buffer underrun occurs and capturing of data currently being transferred is stopped. Ordinary operation is resumed when the next frame transfer starts, according to various settings.

Figure 4-16. Issuance Timing of Frame Interrupt and Display Stop Interrupt



CHAPTER 5 USAGE PROCEDURES

The following shows general procedures for using the LCD controller.

5.1 Starting LCD Display

An example of the setting procedure to start LCD display is described below.

<1> Set the control register (LCD_CONTROL) according to the specifications of the LCD panel connected.

<2> In the same manner, set the parameters related to SYNC and effective pixels, using the following registers.

Horizontal direction total register (LCD_HTOTAL)

Horizontal direction display area register (LCD_HAREA)

Horizontal synchronization edge 1 register (LCD_HEDGE1)

Horizontal synchronization edge 2 register (LCD_HEDGE2)

Vertical direction total register (LCD_VTOTAL)

Vertical direction display area register (LCD_VAREA)

Vertical synchronization edge 1 register (LCD_VEDGE1)

Vertical synchronization edge 2 register (LCD_VEDGE2)

<3> Perform settings related to frame buffers according to the usage rule of internal memory.

Display area address register (LCD_AREAADR)

Address addition value register (LCD_HOFFSET)

Input format register (LCD_IFORMAT)

Simple resize register (LCD_RESIZE)

<4> Set the access bus select register (LCD_BUSSEL).

When accessing the local bus via the IMC is set, separately set parameters for the IMC.

<5> Set “1” in the display register (LCD_LCDOUT) to start LCD display.

Remark The setting of <1> to <4> is not in particular order.

Only the settings of <3> and <4> can be changed during operation in frame units.

Change of settings of <1> and <2> during operation is not supported, so be sure to stop operating before change the settings.

5.2 Stopping LCD Display

When the LCDOUT bit of the display register (LCD_LCDOUT) is set to “0”, the LCD controller stops operation after transfer of the frame currently being output to display is completed.

Whether the LCD display has stopped can be checked by detecting a display stop interrupt or by polling the STATUS bit of the status register (LCD_STATUS).

5.3 Mode Change During Operation (BUSSEL)

Local bus access via the IMC and fixed-value output mode can be switched by setting the access bus select register (LCD_BUSSEL). The setting change takes effect after an LCD frame interrupt occurs after the register values are rewritten. The actual operating mode can be checked by reading the status register immediately after occurrence of an LCD frame interrupt.

5.4 VGA Standby Mode Use Procedure

5.4.1 When data to be displayed has not been stored in frame cache memory

If the LCDOUT bit of the display register (LCD_LCDOUT) is set to 1 while the BUSSEL bit of the access bus select register (LCD_BUSSEL) is set to 2 or 3, the LCD controller operates in the ordinary image synthesis display mode by using the local bus between the IMC and LCD controller and requests WB to the IMC macro. Completion of WB can be checked by detecting a WB end interrupt issued by the IMC macro.

When BUSSEL = 010, the LCD controller automatically enters the ordinary image synthesis display mode after completion of WB. In this case, manually switch to the cache display (BUSSEL = 1).

In either automatic transition, the transition status can be checked by reading the MODESTATUS bit of the status register (LCD_STATUS) immediately after a vertical synchronization interrupt occurs.

Revision History

Date	Revision	Comments
February 10, 2009	1.0	–
April 27, 2009	2.0	Incremental update from comments to the 1.0..
June 16, 2009	3.0	Incremental update from comments to the 2.0..

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