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User’s Manual

Multimedia Processor for Mobile Applications

SPI

EMMA Mobile^{TM}1

Document No. S19261EJ3V0UM00 (3rd edition)
Date Published September 2009

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M8E0904E

PREFACE

Readers

This manual is intended for hardware/software application system designers who wish to understand and use the SPI interface functions of EMMA Mobile1 (EM1), a multimedia processor for mobile applications.

Purpose

This manual is intended to explain to users the hardware and software functions of the SPI interface of EM1, and be used as a reference material for developing hardware and software for systems that use EM1.

Organization

This manual consists of the following chapters.

- Chapter 1 Overview
- Chapter 2 Pin functions
- Chapter 3 Registers
- Chapter 4 Description of functions
- Chapter 5 Usage

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electricity, logic circuits, and microcontrollers.

To understand the functions of the SPI interface of EM1 in detail
→ Read this manual according to the **CONTENTS**.

To understand the other functions of EM1
→ Refer to the user's manual of the respective module.

To understand the electrical specifications of EM1
→ Refer to the Data Sheet.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxB Decimal ... xxxx Hexadecimal ... xxxxH
Data type:	Word … 32 bits Halfword … 16 bits Byte … 8 bits

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name		Document No.
MC-10118A Data sheet		S19657E
μPD77630A Data sheet		S19686E
User's manual	Audio/Voice and PWM Interfaces	S19253E
	DDR SDRAM Interface	S19254E
	DMA Controller	S19255E
	I^{2}C Interface	S19256E
	ITU-R BT.656 Interface	S19257E
	LCD Controller	S19258E
	MICROWIRE	S19259E
	NAND Flash Interface	S19260E
	SPI	This manual
	UART Interface	S19262E
	Image Composer	S19263E
	Image Processor Unit	S19264E
	System Control/General-Purpose I/O Interface	S19265E
	Timer	S19266E
	Terrestrial Digital TV Interface	S19267E
	Camera Interface	S19285E
	USB Interface	S19359E
	SD Memory Card Interface	S19361E
	PDMA	S19373E
	One Chip (MC-10118A)	S19598E
	One Chip (μPD77630A)	S19687E

Caution The related documents listed above are subject to change without notice. Be sure to use the latest version of each document when designing.

CONTENTS

LIST OF FIGURES

CHAPTER 1 OVERVIEW

EM1 incorporates three SPI (serial peripheral interface: a 4-wire serial interface) channels which can be used in either master mode or slave mode.

1.1 Features

The main features of the SPI are as follows.

○ Transfer modes

Master mode and slave mode

CPU mode and DMA mode

CPU mode: Mode in which transfer ends when transmission, reception, or transmission/reception of one frame ends.

DMA mode: Mode in which transfer is executed continuously by using 32-word FIFOs for transmission and reception. This mode is classified into two modes: normal mode, in which transfer is executed until it is stopped by the ACPU, and fixed-length mode, in which transfer automatically stops in accordance with the FIFO status.

○ The SCLK polarity (normal/inverted) and a delay (half of SCLK) can be specified for individual CS signals.

○ The transfer bit length can be specified (8 to 32 bits).

○ Automatic transfer stop function (fixed-length DMA mode)

SPI transmission is stopped when the transmit buffer becomes empty during master transmission.

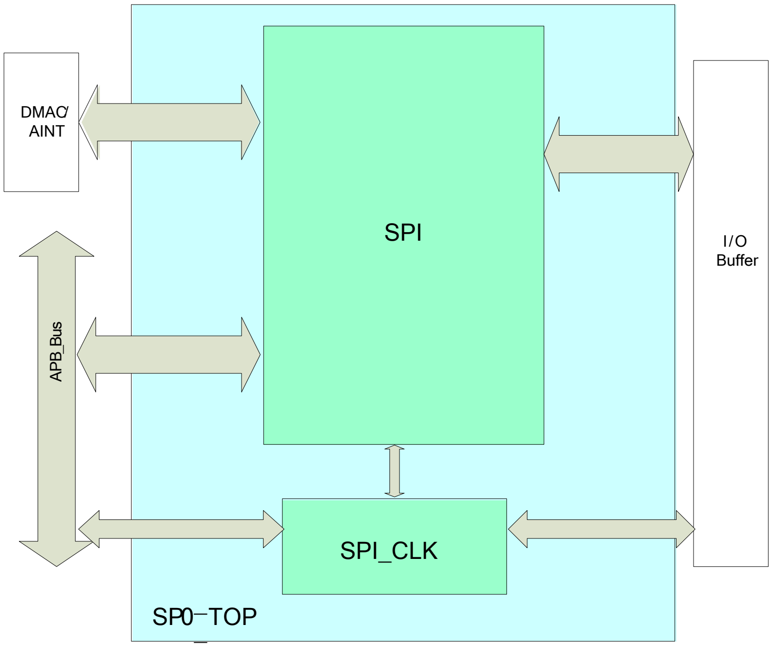
SPI reception is stopped when the amount of data stored in the receive buffer reaches the threshold specified by using a register, during master reception.

○ The CS signal levels can be fixed by setting a register.

○ The I/O phase of SPx_SI and SPx_SO can be switched.

1.2 Block Diagram

Figure 1-1. SPI Module Block Diagram



CHAPTER 2 PIN FUNCTIONS

2.1 SPI Interface Pins

Pin Name	I/O	After Reset	Function	Alternate Pin Function
SP0_CLK	I/O	0	SPI0 clock output	MWI_SK
SP0_SI	Input	–	SPI0 data	MWI_SI
SP0_SO	Output	0	SPI0 data	MWI_SO
SP0_CS0	I/O	0	SPI0 chip select	MWI_CS
SP0_CS[2:1]	Output	0	SPI0 chip select	GIO_P[49:48]
SP1_CLK	I/O	0	SPI1 clock input	GIO_P73 NTS_VS
SP1_SI	Input	–	SPI1 data	GIO_P74 NTS_HS
SP1_SO	Output	0	SPI1 data	GIO_P75 NTS_DATA0 CAM_YUV0
SP1_CS5	Output	0	SPI1 chip select	GIO_P81 NTS_DATA6 PM1_SI
SP1_CS4	Output	0	SPI1 chip select	GIO_P80 NTS_DATA5 PM1_SEN
SP1_CS[3:1]	Output	0	SPI1 chip select	GIO_P[79:77] NTS_DATA[4:2] CAM_YUV[4:2]
SP1_CS0	I/O	0	SPI1 chip select	GIO_P76 NTS_DATA1 CAM_YUV1
SP2_CLK	I/O	0	SPI2 clock input	DTV_BCLK
SP2_SI	Input	–	SPI2 data	DTV_DATA
SP2_SO	Output	0	SPI2 data	DTV_PSYNC
SP2_CS0	I/O	0	SPI2 chip select	DTV_VLD

3.1 Registers

The SPI interface registers can only be accessed in word units.
Do not access reserved registers.
Any value written to reserved bits in each register is ignored.

The register configuration of SP0, SP1 and SP2 is the same.

Base address:	SP0_TOP	C012_0000H
	SP1_TOP	C013_0000H
	SP2_TOP	4013_0000H

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Mode register	SPx_MODE	R/W	0000_0002H
0004H	SPI polarity register	SPx_POL	R/W	0000_7000H
0008H	Control register	SPx_CONTROL	R/W	0000_8040H
000CH	Reserved	–	–	–
0010H	Transmit data register	SPx_TX_DATA	W	0000_0000H
0014H	Receive data register	SPx_RX_DATA	R	0000_00xxH
0018H	Interrupt status register	SPx_STATUS	R	0000_0000H
001CH	Interrupt raw status register	SPx_RAW_STATUS	R	0000_0000H
0020H	Interrupt enable set register	SPx_ENSET	R/W	0000_0000H
0024H	Interrupt enable clear register	SPx_ENCLR	W	0000_0000H
0028H	Interrupt source clear register	SPx_FFCLR	W	0000_0000H
002CH- 0030H	Reserved	–	–	–
0034H	Control register 2	SPx_CONTROL2	R/W	0000_0000H
0038H	CS fix register	SPx_TIECS	R/W	0000_0000H
003CH- FFFFH	Reserved	–	–	–

Remark SPx: x = 0 to 2

3.2 Register Functions

3.2.1 Mode register

This register (SPx_MODE: 0000H) specifies the operation mode of the SPx module.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved		CK_PHASE	NB_A[4:0]				

7	6	5	4	3	2	1	0
Reserved	CS_SELA[2:0]			Reserved		M_S	DMA

Name	R/W	Bit	After Reset	Function
Reserved	R	31:14	0	Reserved. When these bits are read, 0 is returned for each bit.
CK_PHASE	R/W	13	0	0: Normal mode 1: Phase change mode (changing to using a common phase of SCLK for transmission and reception.)
NB_A[4:0]	R/W	12:8	00	Specifies the number of transferred bits[Note]. “NB_A value + 1” bits are transferred. Settable value: 7 to 31
Reserved	R	7	0	Reserved. When this bit is read, 0 is returned.
CS_SELA[2:0]	R/W	6:4	0	Selects the chip select signal used for transfer. 000: CS0 001: CS1 010: CS2 011: CS3 100: CS4 101: CS5 110: Unselectable 111: Unselectable
Reserved	R	3:2	0	Reserved. When these bits are read, 0 is returned for each bit.
M_S	R/W	1	1	Specifies the operating mode. 0: Master mode 1: Slave mode
DMA	R/W	0	0	Specifies the operating mode. 0: CPU mode 1: DMA mode

Note Set the NB_A bit to a value of 7 or more. If a value of less than 7 is specified, data is transferred in the same way as when 7 is specified. The mode cannot be changed during operation.

3.2.2 SPI polarity register

This register (SPx_POL: 0004H) selects the polarity of SCLK and CS (chip select) signals and specifies the SPx_CS inactive period for contiguous transfer (CSW), using the number of SPx_SCLK clock cycles.

This register is used to change the CS output when the CS output is fixed (set to 1) in the CS fix register.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved		CK5_DLY	CK5_POL	CS5_POL	CK4_DLY	CK4_POL	CS4_POL

15	14	13	12	11	10	9	8
CSW[3:0]				CK3_DLY	CK3_POL	CS3_POL	CK2_DLY

7	6	5	4	3	2	1	0
CK2_POL	CS2_POL	CK1_DLY	CK1_POL	CS1_POL	CK0_DLY	CK0_POL	CS0_POL

Name	R/W	Bit	After Reset	Function
Reserved	R	31:22	0	Reserved. When these bits are read, 0 is returned for each bit.
CK5_DLY	R/W	21	0	0: No delay clock is specified. 1: A delay clock is specified.
CK5_POL	R/W	20	0	0: Positive 1: Negative
CS5_POL	R/W	19	0	0: Positive 1: Negative
CK4_DLY	R/W	18	0	0: No delay clock is specified. 1: A delay clock is specified.
CK4_POL	R/W	17	0	0: Positive 1: Negative
CS4_POL	R/W	16	0	0: Positive 1: Negative
CSW[3:0]	R/W	15:12	7	Specifies the width of the SPx_CS inactive period during master transfer. 1 to 16 SPx_SCLK clocks[Note] Interrupts such as END occur after the CSW cycles.
CK3_DLY	R/W	11	0	0: No delay clock is specified. 1: A delay clock is specified.
CK3_POL	R/W	10	0	0: Positive 1: Negative
CS3_POL	R/W	9	0	0: Positive 1: Negative
CK2_DLY	R/W	8	0	0: No delay clock is specified. 1: A delay clock is specified.
CK2_POL	R/W	7	0	0: Positive 1: Negative
CS2_POL	R/W	6	0	0: Positive 1: Negative
CK1_DLY	R/W	5	0	0: No delay clock is specified. 1: A delay clock is specified.
CK1_POL	R/W	4	0	0: Positive 1: Negative
CS1_POL	R/W	3	0	0: Positive 1: Negative
CK0_DLY	R/W	2	0	0: No delay clock is specified. 1: A delay clock is specified.
CK0_POL	R/W	1	0	0: Positive 1: Negative
CS0_POL	R/W	0	0	0: Positive 1: Negative

Note The CSW width is set to a value equivalent to “specified value + 1” SPx_SCLK cycles.

3.2.3 Control register

This register (SPx_CONTROL: 0008H) controls the SPx module.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
TX_EMP	RX_FULL	Reserved					RST

7	6	5	4	3	2	1	0
TX_FULL	RX_EMP	Reserved		WRT	RD	STOP	START

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31:16	0	Reserved. When these bits are read, 0 is returned for each bit.
TX_EMP	R	15	1	0: One or more valid data items exist in the transmit FIFO. 1: The transmit FIFO is empty.
RX_FULL	R	14	0	0: One or more writable areas exist in the receive FIFO. 1: 32-word data is stored in the receive FIFO.
Reserved	R	13:9	0	Reserved. When these bits are read, 0 is returned for each bit.
RST	R/W	8	0	1: Resets the SPx module. Some register settings are not reset. 0: Cancels the reset.
TX_FULL	R	7	0	0: There are writable areas in the transmit FIFO. 1: 32-word data is stored in the transmit FIFO.
RX_EMP	R	6	1	0: Data exists in the receive FIFO. 1: The receive FIFO is empty.
Reserved	R	5:4	0	Reserved. When this bit is read, 0 is returned.
WRT	R/W	3	0	0: Disables transmission. “0” is always output to SPx_SO. 1: Enables transmission. In CPU mode: Data stored in TX_DATA is output to SPx_SO. In DMA mode: TX_DMAREQ is issued if there is available space in the transmit FIFO.
RD	R/W	2	0	0: Disables reception. No data is written to the receive FIFO. 1: Enables reception. In CPU mode: Generates an RDV interrupt each time a frame is received. In DMA mode: RX_DMAREQ is issued if there is valid data in the receive FIFO.

(2/2)

Name	R/W	Bit	After Reset	Function
STOP	W	1	0	0: Ignored 1: Stops DMA transfer forcibly. When this bit is read, 0 is returned. Setting is prohibited when DMA transfer is not performed.
START	W	0	0	0: Ignored 1: Starts transfer. (Ignored during slave operation.)
	R			0: Transfer has been stopped. 1: Transfer is in progress. (Ignored during slave operation.)

Cautions 1. Writing 1 to the RST bit executes a software reset, and writing 0 cancels the software reset.

To execute a synchronous reset during the software reset period, the SPx module requests SPx_PCLK and SPx_SCLK. After the software reset, wait for at least four SPx_SCLK cycles and then cancel the software reset.

The following registers are reset by setting the RST bit.

- **SPx_CONTROL (except for the RST bit)**
- **SPx_STATUS**
- **SPx_RAW_STATUS**

If a software reset is executed during SPI transmission/reception, the current transfer is aborted. At this time, frames being transferred are not guaranteed.

2. The STOP bit can be set only in DMA mode. Setting the STOP bit to 1 is prohibited in a mode other than DMA mode.

If the STOP bit is set to 1 while transfer is stopped, DMA transfer is stopped immediately. If the STOP bit is set to 1 while transfer is being executed, DMA transfer will be stopped after the current transfer ends. When setting the STOP bit to 1, do not change the settings of the WRT and RD bits that were specified when transfer started.

Example To stop transfer that was started by setting the SPx_CONTROL register to 0D in the DMA transmit/receive mode, set the SPx_CONTROL register to 0E.

3. When restarting transfer after setting the STOP bit to 1, make sure that START is set to 0 (transfer has been stopped).

4. Changing the setting of the RD or WRT bit is prohibited during transfer.

5. Reset cancellation (RST = 0) and transfer start (START = 1) must not be set at the same time.

6. Transfer must not be started (START = 1) while the WRT and RD bits are set to 0.

3.2.4 Transmit data register

This register (SPx_TX_DATA: 0010H) stores the transmit data to be written to the transmit FIFO. When this register is read, 0 is returned for each bit. Store data in LSB order. If the NB_A bit of the SPx_MODE register is set to 7, store transmit data to the TX_DATA[7:0] bits.

31	30	29	28	27	26	25	24
TX_DATA[31:24]							

23	22	21	20	19	18	17	16
TX_DATA[23:16]							

15	14	13	12	11	10	9	8
TX_DATA[15:8]							

7	6	5	4	3	2	1	0
TX_DATA[7:0]							

Name	R/W	Bit	After Reset	Function
TX_DATA[31:0]	W	31:0	0	Transmit data register

Caution Do not write data to the transmit FIFO while it is full, because the written data will be lost.

3.2.5 Receive data register

This register (SPx_RX_DATA: 0014H) stores the receive data read from the receive FIFO. Writing to this register is ignored. Receive data is stored in LSB order. If the NB_A bit of the SPx_MODE register is set to 7, data is stored in the RX_DATA[7:0] bits.

31	30	29	28	27	26	25	24
RX_DATA[31:24]							

23	22	21	20	19	18	17	16
RX_DATA[23:16]							

15	14	13	12	11	10	9	8
RX_DATA[15:8]							

7	6	5	4	3	2	1	0
RX_DATA[7:0]							

Name	R/W	Bit	After Reset	Function
RX_DATA[31:0]	R	31:0	0000_00XX	Receive data register

Caution Do not read the receive FIFO while it is empty, because invalid data will be read.

3.2.6 Interrupt status register

This read-only register (SPx_STATUS: 0018H) is used to read the status of the interrupt sources enabled by the interrupt enable set register (SPx_ENSET).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved	TX_STOP	RX_STOP	TERR	RDV	END	TX_UDR	RX_OVR

Name	R/W	Bit	After Reset	Function
Reserved	R	31:7	0	Reserved. When these bits are read, 0 is returned for each bit.
TX_STOP	R	6	0	Indicates that data is no longer stored in the transmit FIFO after transmission starts. This flag is valid only in DMA master mode.
RX_STOP	R	5	0	Indicates that the amount of received data has reached the value set to the RX_FIFO_FULL bit of the SPx_CONTROL2 register. This flag is valid only in DMA master mode.
TERR	R	4	0	Indicates that the number of SPx_SCLK_I cycles does not match the value set to the NB_A bit of the SPx_MODE register. This flag is not set if the number of SPx_SCLK_I cycles is a multiple of the value set to the NB_A bit.
RDV	R	3	0	Indicates that reception of 1 frame is complete in CPU mode.
END	R	2	0	Indicates that transmission and reception of one frame is complete in CPU mode.
TX_UDR	R	1	0	Indicates that an underrun has occurred in the transmit FIFO.
RX_OVR	R	0	0	Indicates that an overrun has occurred in the receive FIFO.

Cautions 1. The interrupts TERR, TX_UDR, RX_OVR, END, and RDV occur in CPU mode.

2. The interrupts TERR, TX_UDR, RX_OVR, RX_STOP, and TX_STOP occur in DMA mode.

3. The interrupts TERR, TX_UDR, and RX_OVR occur only in slave mode.

3.2.7 Interrupt raw status register

This read-only register (SPx_RAW_STATUS: 001CH) is used read the status of interrupt sources regardless of the setting of the interrupt enable set register (SPx_ENSET).

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved	TX_STOP_RAW	RX_STOP_RAW	TERR_RAW	RDV_RAW	END_RAW	TX_UDR_RAW	RX_OVR_RAW

Name	R/W	Bit	After Reset	Function
Reserved	R	31:7	0	Reserved. When these bits are read, 0 is returned for each bit.
TX_STOP_RAW	R	6	0	Indicates that data is no longer stored in the transmit FIFO after transmission starts. This flag is valid only in DMA master mode.
RX_STOP_RAW	R	5	0	Indicates that the amount of received data has reached the value set to the RX_FIFO_FULL bit of the SPx_CONTROL2 register. This flag is valid only in DMA master mode.
TERR_RAW	R	4	0	Indicates that the number of SPx_SCLK_I cycles does not match the value set to the NB_A bit of the SPx_MODE register. This flag is not set if the number of SPx_SCLK_I cycles is a multiple of the value set to the NB_A bit.
RDV_RAW	R	3	0	Indicates that reception of 1 frame is complete in CPU mode.
END_RAW	R	2	0	Indicates that transmission and reception of one frame is complete in CPU mode.
TX_UDR_RAW	R	1	0	Indicates that an underrun has occurred in the transmit FIFO.
RX_OVR_RAW	R	0	0	Indicates that an overrun has occurred in the receive FIFO.

Cautions 1. The interrupts TERR_RAW, TX_UDR_RAW, RX_OVR_RAW, END_RAW, and RDV_RAW occur in CPU mode.

2. The interrupts TERR_RAW, TX_UDR_RAW, RX_OVR_RAW, RX_STOP_RAW, and TX_STOP_RAW occur in DMA mode.

3. The interrupts TERR_RAW, TX_UDR_RAW, and RX_OVR_RAW occur only in slave mode.

3.2.8 Interrupt enable set register

This register (SPx_ENSET: 0020H) enables the issuance of interrupt requests. When the bit corresponding to an interrupt source is set to 1 in this register, the interrupt source is set, an interrupt request is issued, and the corresponding bit in the interrupt status register (SPx_STATUS) is set to 1. Writing 0 to this register does not affect the setting. The interrupt request issuance enable status can be checked by reading this register.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved	TX_STOP_EN	RX_STOP_EN	TERR_EN	RDV_EN	END_EN	TX_UDR_EN	RX_OVR_EN

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	31:7	0	Reserved. When these bits are read, 0 is returned for each bit.
TX_STOP_EN	R	6	0	Indicates whether issuance of the TX_STOP interrupt request is enabled. 0: Not enabled. 1: Enabled.
	W			Enables issuance of the TX_STOP interrupt. 0: Ignored. 1: Cancels masking of the interrupt.
RX_STOP_EN	R	5	0	Indicates whether issuance of the RX_STOP interrupt request is enabled. 0: Not enabled. 1: Enabled.
	W			Enables issuance of the RX_STOP interrupt. 0: Ignored. 1: Cancels masking of the interrupt.
TERR_EN	R	4	0	Indicates whether issuance of the TERR interrupt request is enabled. 0: Not enabled. 1: Enabled.
	W			Enables issuance of the TERR interrupt. 0: Ignored. 1: Cancels masking of the interrupt.
RDV_EN	R	3	0	Indicates whether issuance of the RDV interrupt request is enabled. 0: Not enabled. 1: Enabled.
	W			Enables issuance of the RDV interrupt. 0: Ignored. 1: Cancels masking of the interrupt.
END_EN	R	2	0	Indicates whether issuance of the END interrupt request is enabled. 0: Not enabled. 1: Enabled.
	W			Enables issuance of the END interrupt. 0: Ignored. 1: Cancels masking of the interrupt.

(2/2)

Name	R/W	Bit	After Reset	Function
TX_UDR_EN	R	1	0	Indicates whether issuance of the TX_UDR interrupt request is enabled. 0: Not enabled. 1: Enabled.
	W			Enables issuance of the TX_UDR interrupt. 0: Ignored. 1: Cancels masking of the interrupt.
RX_OVR_EN	R	0	0	Indicates whether issuance of the RX_OVR interrupt request is enabled. 0: Not enabled. 1: Enabled.
	W			Enables issuance of the RX_OVR interrupt. 0: Ignored. 1: Cancels masking of the interrupt.

3.2.9 Interrupt enable clear register

This register (SPx_ENCLR: 0024H) disables the issuance of interrupt requests. When the bit corresponding to an interrupt source is set to 1 in the register, an interrupt request is not issued even if the interrupt source occurs. The status of the bit corresponding to the interrupt status register (SPx_STATUS) also does not change. Writing 0 to this register does not affect the setting.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved	TX_STOP_ MASK	RX_STOP_ MASK	TERR_MASK	RDV_MASK	END_MASK	TX_UDR_ MASK	RX_OVR_ MASK

Name	R/W	Bit	After Reset	Function
Reserved	R	31:7	0	Reserved. When these bits are read, 0 is returned for each bit.
TX_STOP_MASK	W	6	0	0: Ignored. 1: Disables issuance of a request for the TX_STOP interrupt.
RX_STOP_MASK	W	5	0	0: Ignored. 1: Disables issuance of a request for the RX_STOP interrupt.
TERR_MASK	W	4	0	0: Ignored. 1: Disables issuance of a request for the TERR interrupt.
RDV_MASK	W	3	0	0: Ignored. 1: Disables issuance of a request for the RDV interrupt.
END_MASK	W	2	0	0: Ignored. 1: Disables issuance of a request for the END interrupt.
TX_UDR_MASK	W	1	0	0: Ignored. 1: Disables issuance of a request for the TX_UDR interrupt.
RX_OVR_MASK	W	0	0	0: Ignored. 1: Disables issuance of a request for the RX_OVR interrupt.

3.2.10 Interrupt source clear register

This write-only register (SPx_FFCLR: 0028H) clears interrupt sources. When the bit corresponding to an interrupt source is set to 1 in the register, the interrupt source is cleared. Writing 0 to this register does not affect the setting.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved	TX_STOP_CLR	RX_STOP_CLR	TERR_CLR	RDV_CLR	END_CLR	TX_UDR_CLR	RX_OVR_CLR

Name	R/W	Bit	After Reset	Function
Reserved	R	31:7	0	Reserved. When these bits are read, 0 is returned for each bit.
TX_STOP_CLR	W	6	0	0: Ignored. 1: Clears the interrupt source of TX_STOP.
RX_STOP_CLR	W	5	0	0: Ignored. 1: Clears the interrupt source of RX_STOP.
TERR_CLR	W	4	0	0: Ignored. 1: Clears the interrupt source of TERR.
RDV_CLR	W	3	0	0: Ignored. 1: Clears the interrupt source of RDV.
END_CLR	W	2	0	0: Ignored. 1: Clears the interrupt source of END.
TX_UDR_CLR	W	1	0	0: Ignored. 1: Clears the interrupt source of TX_UDR.
RX_OVR_CLR	W	0	0	0: Ignored. 1: Clears the interrupt source of RX_OVR.

3.2.11 Control register 2

This register (SPx_CONTROL2: 0034H) controls fixed-length transfer in DMA master mode.

The settings of fixed-length transfer are invalid in a mode other than the DMA master mode.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
RX_FIFO_FULL[15:8]							

15	14	13	12	11	10	9	8
Reserved						TX_STOP_MODE	RX_STOP_MODE

7	6	5	4	3	2	1	0
RX_FIFO_FULL[7:0]							

Name	R/W	Bit	After Reset	Function
Reserved	R	31:24	0	Reserved. When these bits are read, 0 is returned for each bit.
RX_FIFO_FULL[15:8]	R/W	23:16	0	The higher 8 bits of RX_FIFO_FULL
Reserved	R	15:10	0	Reserved. When these bits are read, 0 is returned for each bit.
TX_STOP_MODE	R/W	9	0	Specifies whether to stop SPI transmission/reception when the transmit FIFO becomes empty during DMA master transmission. 0: Does not stop transfer. 1: Stops transfer.
RX_STOP_MODE	R/W	8	0	Specifies whether to stop SPI transmission/reception when the number of received words reaches the value set to the RX_FIFO_FULL bits during DMA master reception. 0: Does not stop transfer. 1: Stops transfer.
RX_FIFO_FULL[7:0]	R/W	7:0	0	The lower 8 bits of RX_FIFO_FULL Specifies the threshold of the number of words to be received. An RX_STOP interrupt occurs if the number of received words reaches the specified value. Specify this together with the higher 8 bits. 0000h: An RX_STOP interrupt occurs when 1 word is received. 0001h: An RX_STOP interrupt occurs when 2 words are received. : FFFEh: An RX_STOP interrupt occurs when 65,535 words are received. FFFFh: An RX_STOP interrupt occurs when 65,536 words are received.

Caution The threshold specified by the RX_FIFO_FULL bits is valid for reception in DMA mode (receive mode, transmit/receive mode).

An RX_STOP interrupt is output regardless of the RX_STOP_MODE setting. When transmission and reception are enabled (WRT and RD = 1 in SPx_CONTROL register), set the TX_STOP_MODE and RX_STOP_MODE bits to 1. Setting fixed-length transfer for one side only is prohibited in this mode.

3.2.12 CS fix register

This register (SPx_TIECS: 0038H) fixes the output of SPx_CS0 to SPx_CS5.

The level is fixed according to the value set to the SPI polarity register (SPx_POL).

If the CS3_POL bit of the SPx_POL register is set to 0 (positive), for example, setting the R_CS3 bit of this register to 1 fixes the CS3 output level to 0.

31	30	29	28	27	26	25	24
Reserved							

23	22	21	20	19	18	17	16
Reserved							

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved		R_CS5	R_CS4	R_CS3	R_CS2	R_CS1	R_CS0

Name	R/W	Bit	After Reset	Function
Reserved	R	31:6	0	Reserved. When these bits are read, 0 is returned for each bit.
R_CS5	R/W	5	0	Specifies the value output from the SPx_CS5 pin. 0: Normal operation 1: SPx_CS5 is fixed to the value set to CS5_POL.
R_CS4	R/W	4	0	Specifies the value output from the SPx_CS4 pin. 0: Normal operation 1: SPx_CS4 is fixed to the value set to CS4_POL.
R_CS3	R/W	3	0	Specifies the value output from the SPx_CS3 pin. 0: Normal operation 1: SPx_CS3 is fixed to the value set to CS3_POL.
R_CS2	R/W	2	0	Specifies the value output from the SPx_CS2 pin. 0: Normal operation 1: SPx_CS2 is fixed to the value set to CS2_POL.
R_CS1	R/W	1	0	Specifies the value output from the SPx_CS1 pin. 0: Normal operation 1: SPx_CS1 is fixed to the value set to CS1_POL.
R_CS0	R/W	0	0	Specifies the value output from the SPx_CS0 pin. 0: Normal operation 1: SPx_CS0 is fixed to the value set to CS0_POL.

CHAPTER 4 DESCRIPTION OF FUNCTIONS

4.1 Automatic Transfer Stop Function (in Fixed-Length DMA Master Mode)

SPI transmission is stopped when the transmit FIFO becomes empty during master transmission in DMA mode.

SPI reception is stopped when the amount of data stored in the receive FIFO reaches the value set to the RX_FIFO_FULL bits of the SPx_CONTROL2 register during master reception in DMA mode.

4.2 Interrupt Generation

Interrupt signals (SPx_INT) can be generated by the following sources.

○ Interrupt signals (SPx_INT) are generated:

- When the transmit FIFO becomes empty during master transfer in DMA mode. (TX_STOP)
- When the amount of received data reaches the value set to the RX_FIFO_FULL[15:0] bits of the SPx_CONTROL2 register during master transfer in DMA mode. (RX_STOP)
- When the number of SPx_SCLK_I clock cycles is not a multiple of the value set to the NB_A bits of the SPx_MODE register during slave transfer. (TERR)
  When a TERR interrupt occurs, an END interrupt does not occur upon the completion of transfer. A software reset is required to resume transfer.
- When reception of one frame is completed in CPU mode. (RDV)
- When transmission or reception of one frame is completed in CPU mode. (END)
- When the transmit FIFO underruns during slave transfer. (TX_UDR)
  At that time, the data being transmitted is not guaranteed. A software reset is required to resume transfer.
- When the receive FIFO overruns during slave transfer. (RX_OVR)
  At that time, the data being received is not guaranteed. A software reset is required to resume transfer.
  Once the receive FIFO becomes full, an RX_OVR interrupt occurs when the next data is received, even if data in the receive FIFO is read to release it from the full state.
- When SCLK or CS is input before transmit data is set to the transmit FIFO for slave transfer in DMA mode when transmission and reception is set (WRT and RD = 1). (TX_UDR)

4.3 Clocks

Each SPI clock can be controlled (constant supply, automatic control and stop) by setting a clock setting register in the ASMU.

When automatic APB clock control is enabled, it is assumed that the APB clock (PCLK) takes one cycle before PSEL, two cycles during PSEL, and three cycles after PSEL to access registers.

PCLK is requested by the SPI by pulling PCLKREQ and SCLKREQ high.

○ SPx_SCLKREQ

- The SPI sets the SPx_SCLKREQ pin to 1 to request the clock supplier (ASMU) to output SPx_SCLK.
- Once SPx_SCLKREQ is set to 1, the SPI continues to request SPx_SCLK during master transfer (START bit of SPx_CONTROL register = 1).

○ SPx_PCLKREQ

- The SPI sets the SPx_PCLKREQ pin to 1 to request the clock supplier (ASMU) to output SPx_PCLK.
- Once SPx_PCLKREQ is set to 1, the SPI requests SPx_PCLK when controlling a pointer.

4.4 Fixing CS by Setting a Register

The SPx_CS0 to SPx_CS5 signals can be fixed to a certain level (high or low) by setting the SPx_TIECS register. The level to which the signals are to be fixed is specified using the SPx_POL register.

The CS level can only be fixed by the SPx_TIECS register; it is not affected by the SPI internal operation.

4.5 Switching the I/O Phases of SPx_SI and SPx_SO (at the Rising/Falling Edge of SCLK)

Using the CK_PHASE bit of the SPx_MODE register, the reverse phase of SPx_SI/SPx_SO input/output (default) can be changed to a common phase. The F/F phase of the reception side is changed during master operation, and the F/F phase of the transmission side is changed during slave operation.

4.6 Reset Control

○ The SPI registers use a synchronous reset.

○ Because all registers are reset at power-on, SPx_PCLK and SPx_SCLK must be supplied from the ASMU during the power-on reset period.

○ Software reset control

The SPI module is in the software reset state in the period from when the RST bit of the SPx_CONTROL register is set to 1 until it is set to 0.

The following registers are reset by a software reset.

- SPx_CONTROL (except for the RST bit)
- SPx_STATUS
- SPx_RAW_STATUS

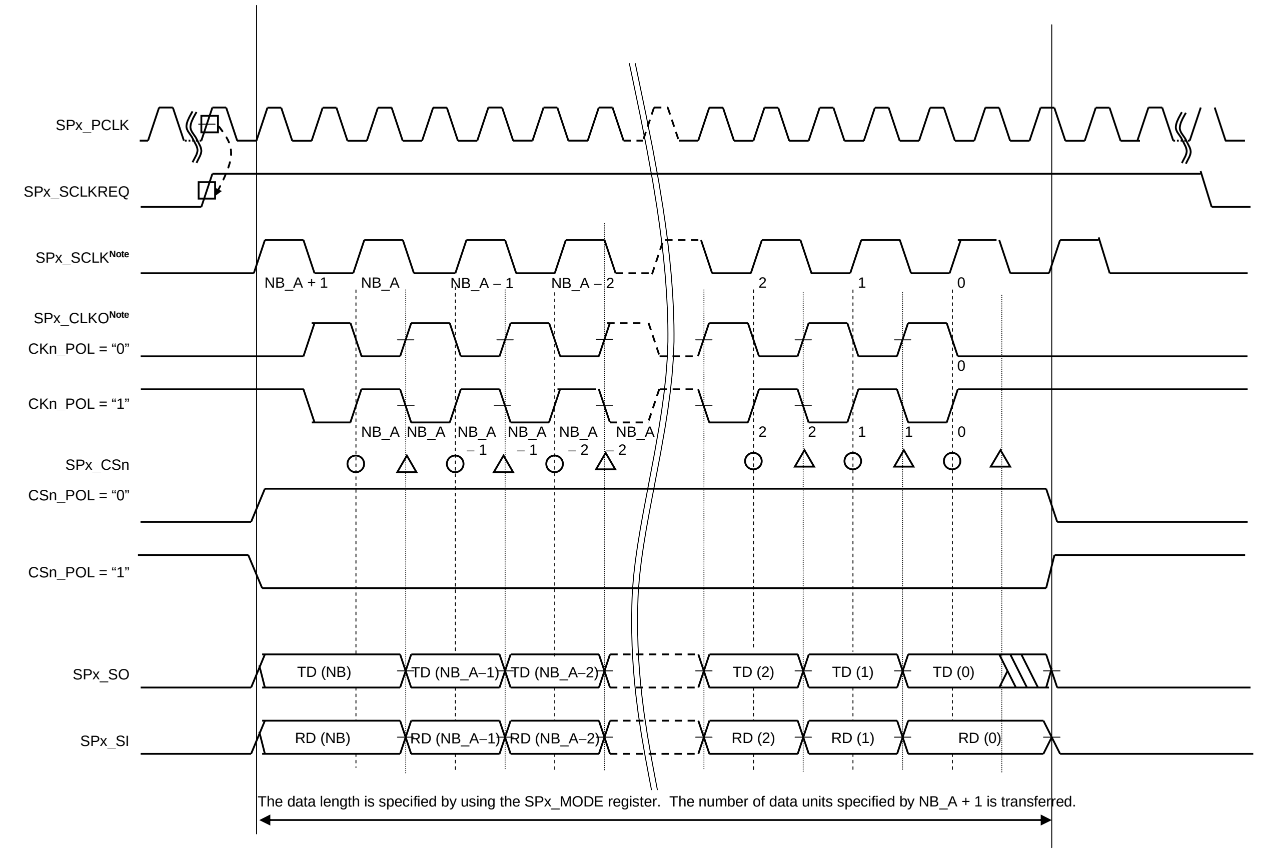
Caution Transfer is stopped if a software reset is executed during transfer. (The data being transferred is not guaranteed.)

4.7 Detailed Timing

4.7.1 SPI interface timing 1 (CKn_DLY = 0 in master mode)

Figure 4-1 shows SPI interface timing 1.

Figure 4-1. SPI Interface Timing 1



The data length is specified by using the SPx_MODE register. The number of data units specified by NB_A + 1 is transferred.

○ Timing at which data is loaded into SPI with CK_PHASE = 0

△ Timing at which data is loaded into SPI with CK_PHASE = 1

Note SPx_SCLK: Serial clock input from ASMU
SPx_CLKO: Serial clock output to the SPI interface

SPI interface timing 1 shows the timing of the SPI in master mode with the CKn_DLY bit[Note] of the SPx_POL register set to 0.

A serial clock is output from SPx_CLKO, and a CS signal is output from SPx_CSn[Note] to an external device.

In master mode, SPx_SCLKREQ is set to 1 in synchronization with SPx_PCLK in cycle in which communication started, and this SPx_SCLKREQ triggers supply of SPx_SCLK from the ASMU. Transmit/receive data is output in synchronization with SPx_SCLK when SPx_CSn is active[Note], and the receive data is fetched by the SPI module in synchronization with SPx_SCLK.

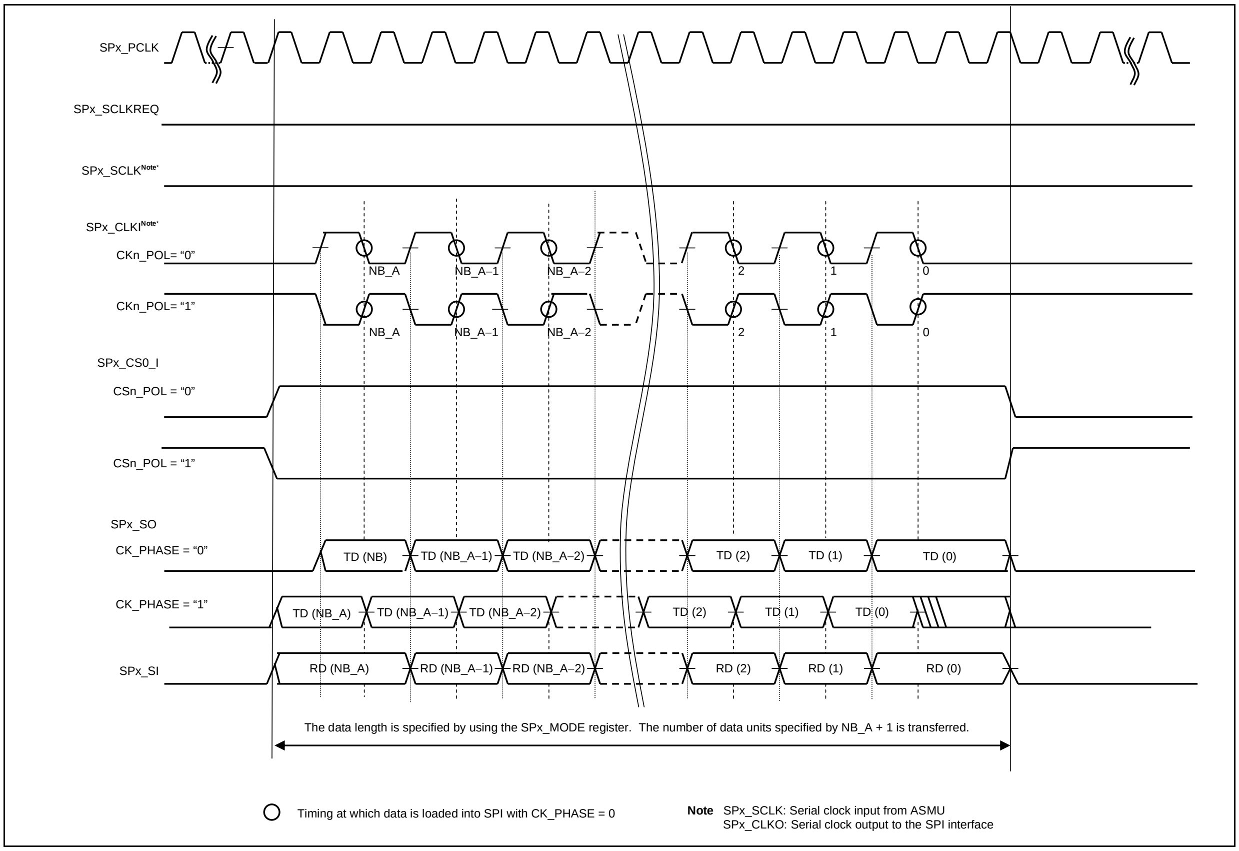
In master mode, the timing at which the receive data is fetched varies depending on the setting of CK_PHASE.

Note CSn_POL, CKn_POL, and CKn_DLY show the polarity or delay setting of CSn specified by the CS_SELA bits of the mode register (n = 0 to 5). Data is output to the selected CS during master operation, regardless of whether the mode is CPU mode or DMA mode. The CSn_POL bit is used to determine the active level of SPx_CSn (0: high, 1: low).

4.7.2 SPI interface timing 2 (CK0_DLY = 0 in slave mode)

Figure 4-2 shows SPI interface timing 2.

Figure 4-2. SPI Interface Timing 2



The data length is specified by using the SPx_MODE register. The number of data units specified by NB_A + 1 is transferred.

○ Timing at which data is loaded into SPI with CK_PHASE = 0

Note SPx_SCLK: Serial clock input from ASMU
SPx_CLKO: Serial clock output to the SPI interface

SPI interface timing 2 shows the timing of the SPI in slave mode with the CK0_DLY bit**Note** of the SPx_POL register set to 0.

A serial clock is input from SPx_CLKI, and a CS signal is input to SPx_CSn_I from an external device.

In slave mode, SPx_SCLKREQ is not set to 1, and therefore a request for supply of SPx_SCLK is not issued.

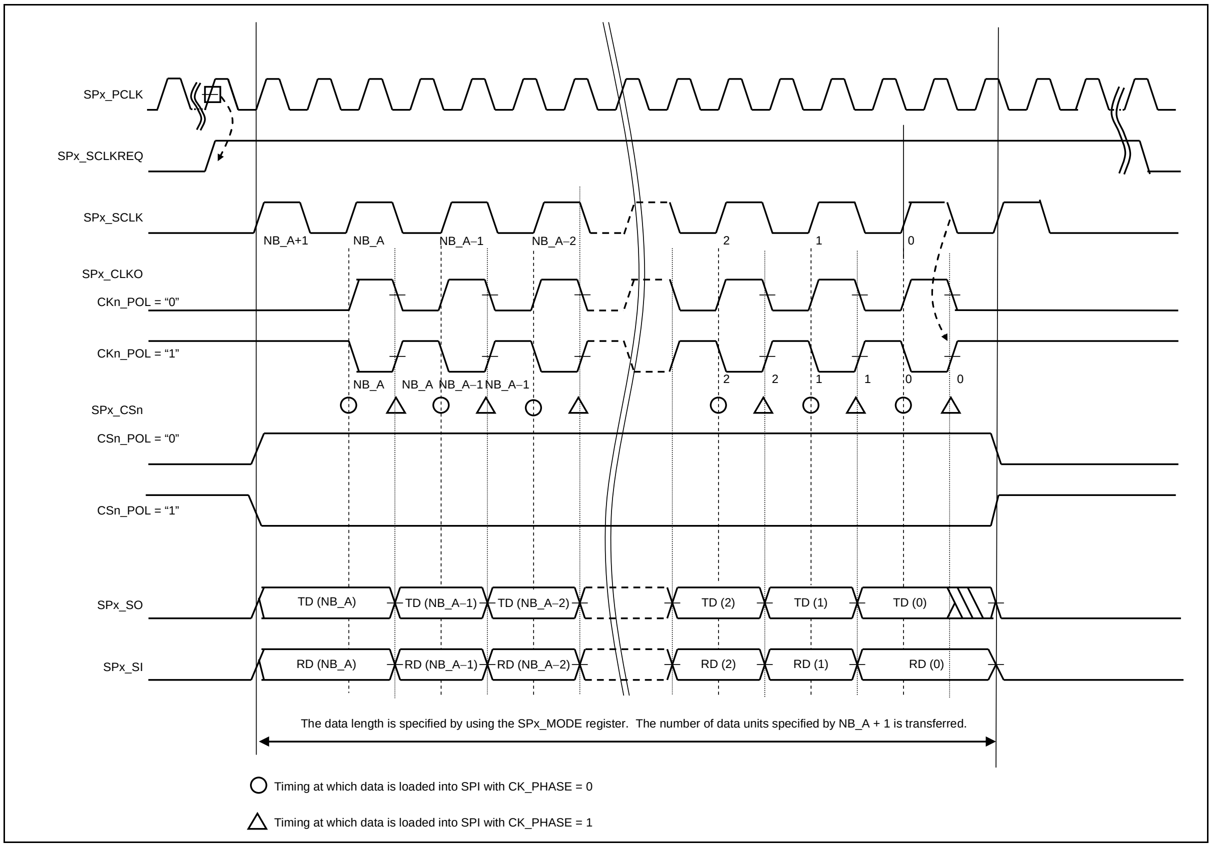
Transmit/receive data is output in synchronization with SCLK (SPx_CLKI) when SPx_CS0_I is active**Note**, and the receive data is fetched by the SPI module in synchronization with SCLK (SPx_CLKI).

In slave mode, the timing at which the transmit data is output varies depending on the setting of CK_PHASE.

4.7.3 SPI interface timing 3 (CKn_DLY = 1 in master mode)

Figure 4-3 shows SPI interface timing 3.

Figure 4-3. SPI Interface Timing 3



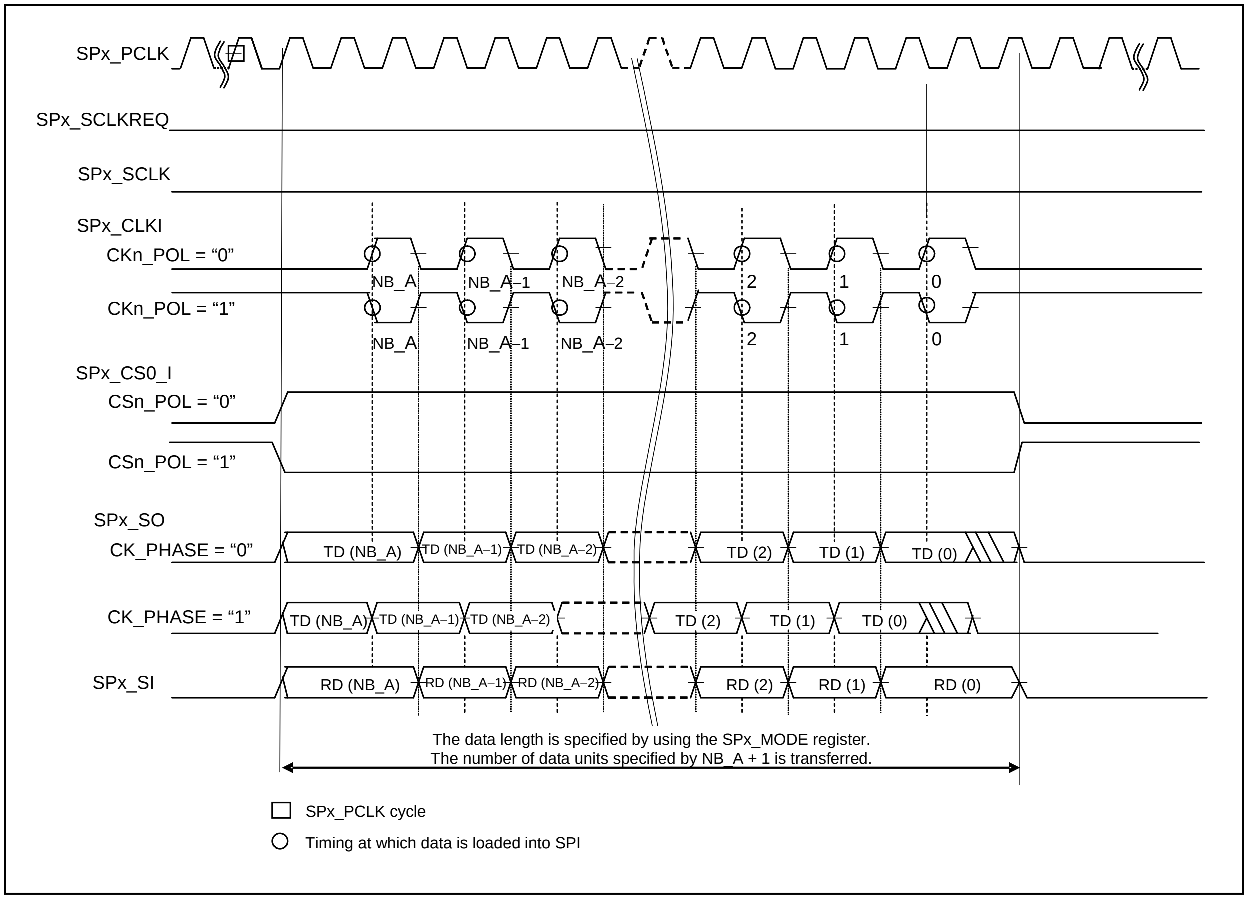
SPI interface timing 3 shows the timing of the SPI in master mode with the CKn_DLY bit$^{\text{Note}}$ of the SPx_POL register set to 1, and when SPx_CLKO is output half a clock later than the output timing in SPI interface timing 1.

In master mode, the timing at which the receive data is fetched varies depending on the setting of CK_PHASE.

4.7.4 SPI interface timing 4 (CK0_DLY = 1 in slave mode)

Figure 4-4 shows SPI interface timing 4.

Figure 4-4. SPI Interface Timing 4



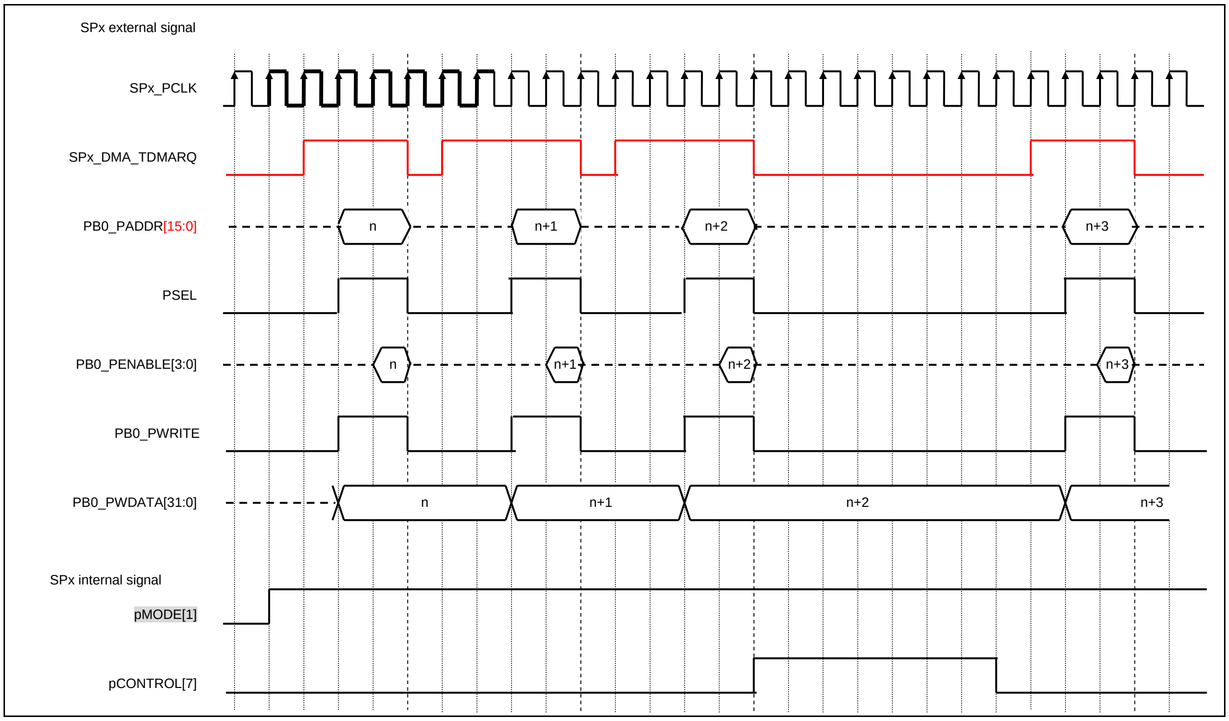
SPI interface timing 4 shows the timing of the SPI in slave mode with the CK0_DLY bit[Note] of the SPx_POL register set to 1, and when SPx_CLKI is output half a clock later than the output timing in SPI interface timing 2.

In slave mode, the timing at which the transmit data is output varies depending on the setting of CK_PHASE.

4.7.5 DMA transmission timing

Figure 4-5 shows the timing of DMA transmission.

Figure 4-5. DMA Transmission Timing



When the DMA bit of the mode register (SPx_MODE) is set to 1, DMA mode is set. Setting the WRT bit of the control register (SPx_CONTROL) to 1 enables issuance of requests for DMA transmission.

If the transmit FIFO is not full while the DMA bit is set to 1, SPx_DMA_TDMARQ is set to 1 to request transmit data. Whether the transmit FIFO is full can be checked by reading the TX_FULL bit of the SPx_CONTROL register.

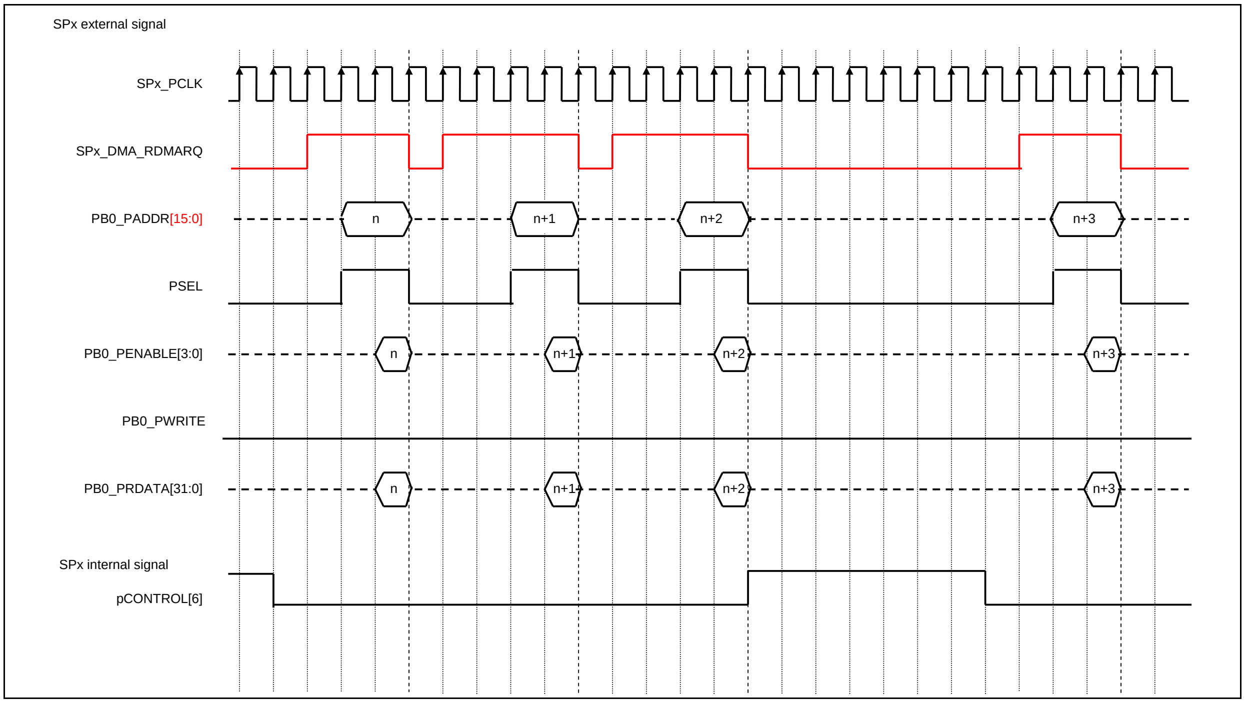
To request transmission repeatedly, set SPx_DMA_TDMARQ to 0 for one SPx_PCLK cycle; the next access is then performed.

To stop transfer which is activated by setting the START bit of the control register (SPx_CONTROL) to 1, set the STOP bit of the SPx_CONTROL register to 1.

4.7.6 DMA reception timing

Figure 4-6 shows the timing of DMA reception.

Figure 4-6. DMA Reception Timing



When the DMA bit of the mode register (SPx_MODE) is set to 1, DMA mode is set. Setting the RD bit of the control register (SPx_CONTROL) to 1 enables issuance of requests for DMA reception.

If the receive FIFO is not empty while the DMA bit is set to 1, SPx_DMA_RDMARQ is set to 1 to request receive data.

Whether the receive FIFO is empty can be checked by reading the RX_EMP bit of the SPx_CONTROL register.

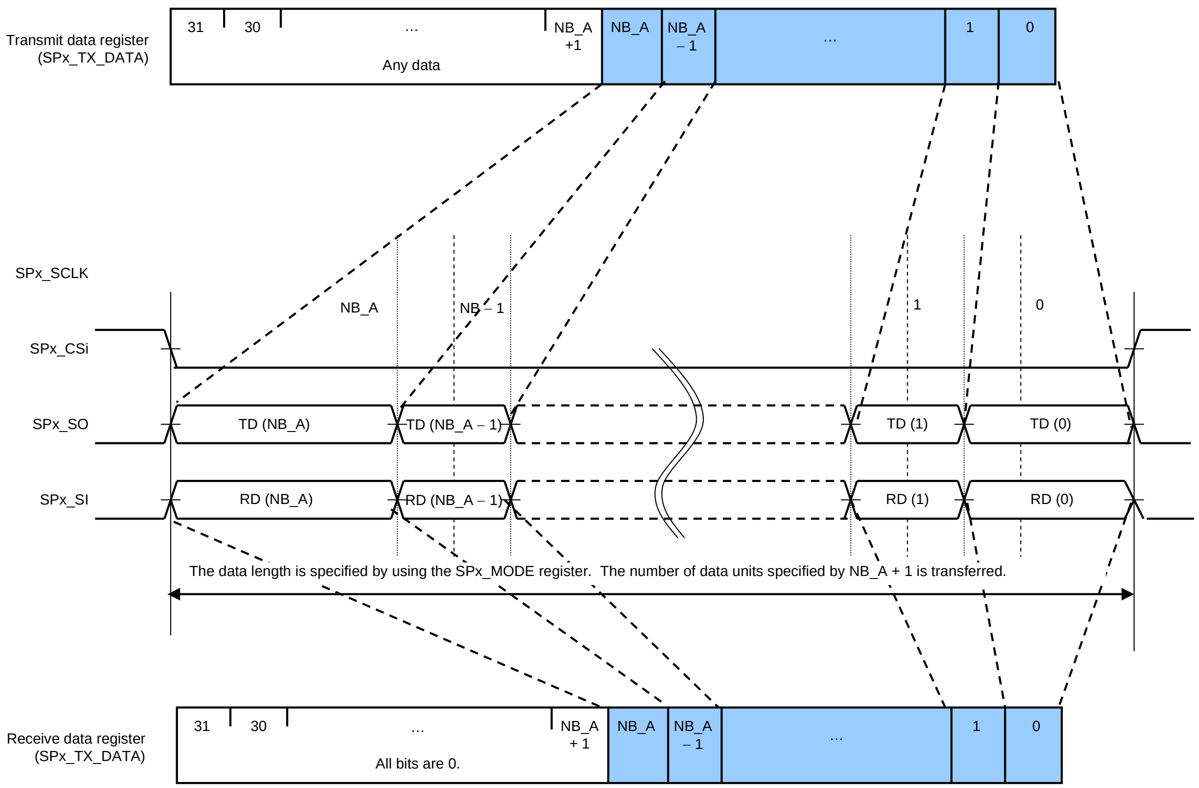
To request reception repeatedly, set SPx_DMA_RDMARQ to 0 for one SPx_PCLK cycle; the next access is then performed.

To stop transfer which is activated by setting the START bit of the control register (SPx_CONTROL) to 1, set the STOP bit of the SPx_CONTROL register to 1.

4.7.7 Correspondence between transmit data register, receive data register, and serial transfer data

Figure 4-7 shows the correspondence between the transmit data register, the receive data register, and the serial transfer data.

Figure 4-7. Bit Correspondence



Serial data in the transmit data register is transferred via SPx_SO starting from the MSB of the data specified by the NB_A bits of the SPx_MODE register.

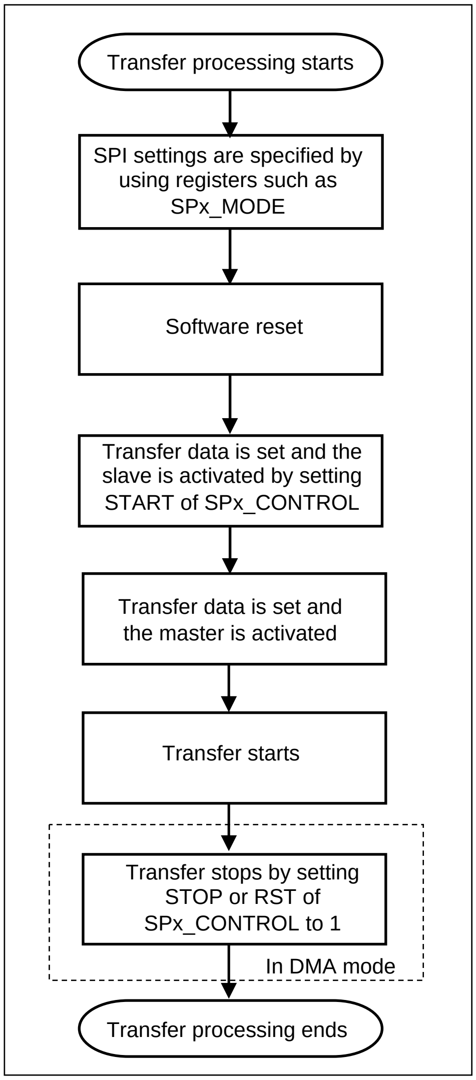
Serial data received via SPx_SI is stored in the receive data register, starting from the MSB. The LSB of the receive data is stored in the LSB of the receive data register. Bits higher than the ones specified by the NB_A bits are filled with 0.

CHAPTER 5 USAGE

5.1 SPI Transfer Procedure

Figure 5-1 shows the SPI transfer procedure.

Figure 5-1. SPI Transfer Procedure


Transfer processing starts
SPI settings are specified by using registers such as SPx_MODE
Software reset
Transfer data is set and the slave is activated by setting START of SPx_CONTROL
Transfer data is set and the master is activated
Transfer starts
Transfer stops by setting STOP or RST of SPx_CONTROL to 1
In DMA mode
Transfer processing ends

Caution If this procedure is not observed, data that differs from the data set in the SPx_TX_DATA register might be output from the SPIx_SO pin. If transfer started by setting the START bit of the SPx_CONTROL register to 1 and frame transfer occur at the same time in slave mode, the data of the overlapped frame might not be transmitted or received correctly. In DMA mode, transfer is stopped by setting the STOP or RST bit of the SPx_CONTROL register to 1.

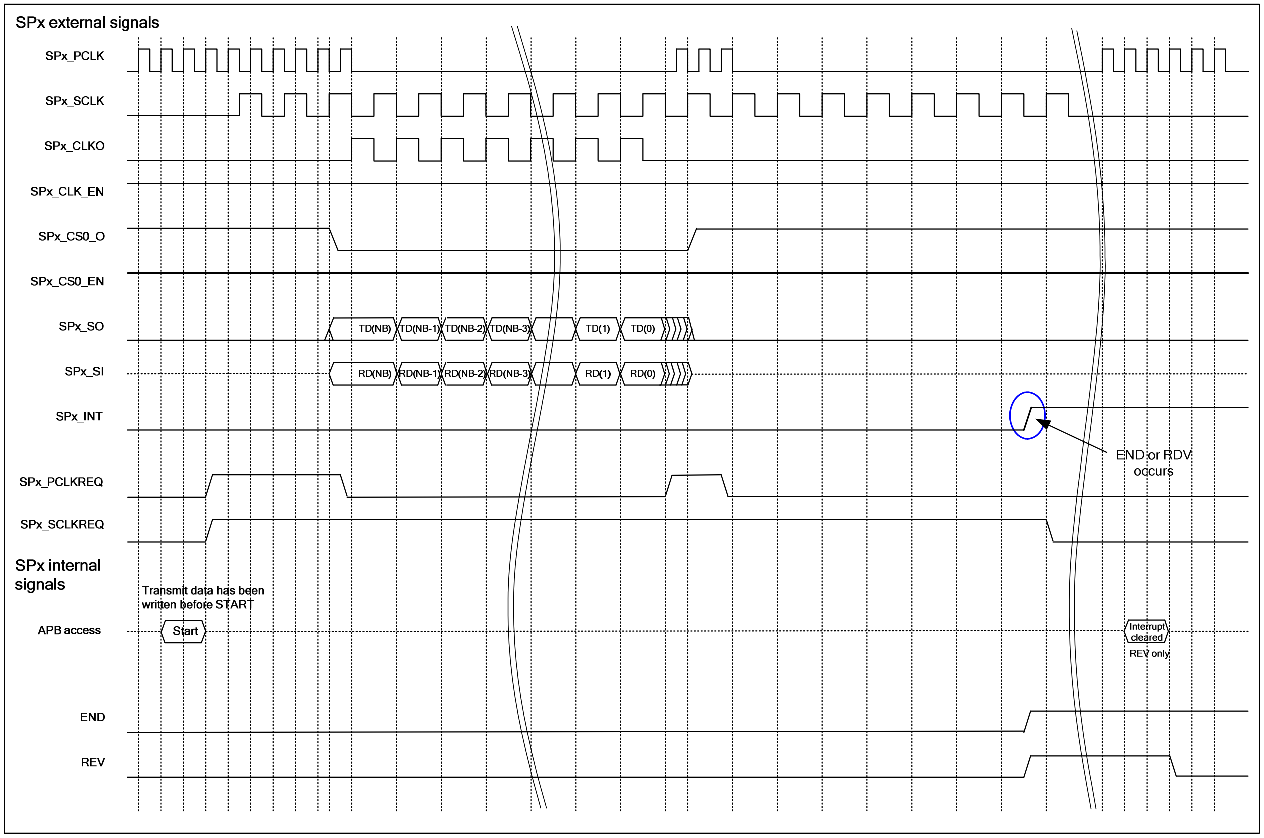
Remarks 1. When changing the register values, supply the internal SCLK clock by setting the GCLKCTRL1 register in the ASMU (in master and slave mode).

2. Disable automatic SCLK control by using the CLKCTRLx register in the ASMU. It is recommended to also disable automatic PCLK control by using the APBCLKCTRLx register.

5.1.1 Master transfer in CPU mode

Figure 5-2 shows the timing of master transfer in CPU mode.

Figure 5-2. Master Transfer Timing in CPU Mode (CKn_DLY = 0)



Master transfer in CPU mode is enabled by setting the DMA bit to 0 and M_S bit to 0 in the mode register (SPx_MODE). In master mode, the SPI interface is controlled by SPx_CLKO and SCx_CSn_O output from the SPI module.

When the RD bit of the control register (SPx_CONTROL) is set to 1, data is received serially starting from the MSB. When the WRT bit of the SPx_CONTROL register is set to 1, data stored in the transmit data register (SPx_TX_DATA) is transmitted serially, starting from the MSB. The amount of data to be transferred is the value of the NB_A bits specified in the SPx_MODE register + 1. SPx_SCLK is output for more cycles than the amount of data specified by NB_A, but SPx_CLKO is controlled by the SPI module and output to the SPI interface for number of cycles equivalent to the amount of data specified by NB_A + 1.

If the START bit of the SPx_CONTROL register is set to 1 while there is no data stored in the transmit FIFO, transmission is held pending until transmit data is written to the transmit FIFO. Data is not received while the receive FIFO is full.

The END flag of the SPx_STATUS register is set to 1 when frame transmission ends. For reception, the RDV flag is also set to 1. A TERR interrupt does not occur during master transfer in CPU mode.

For transmission/reception, data is transferred according to the conditions for transmission.

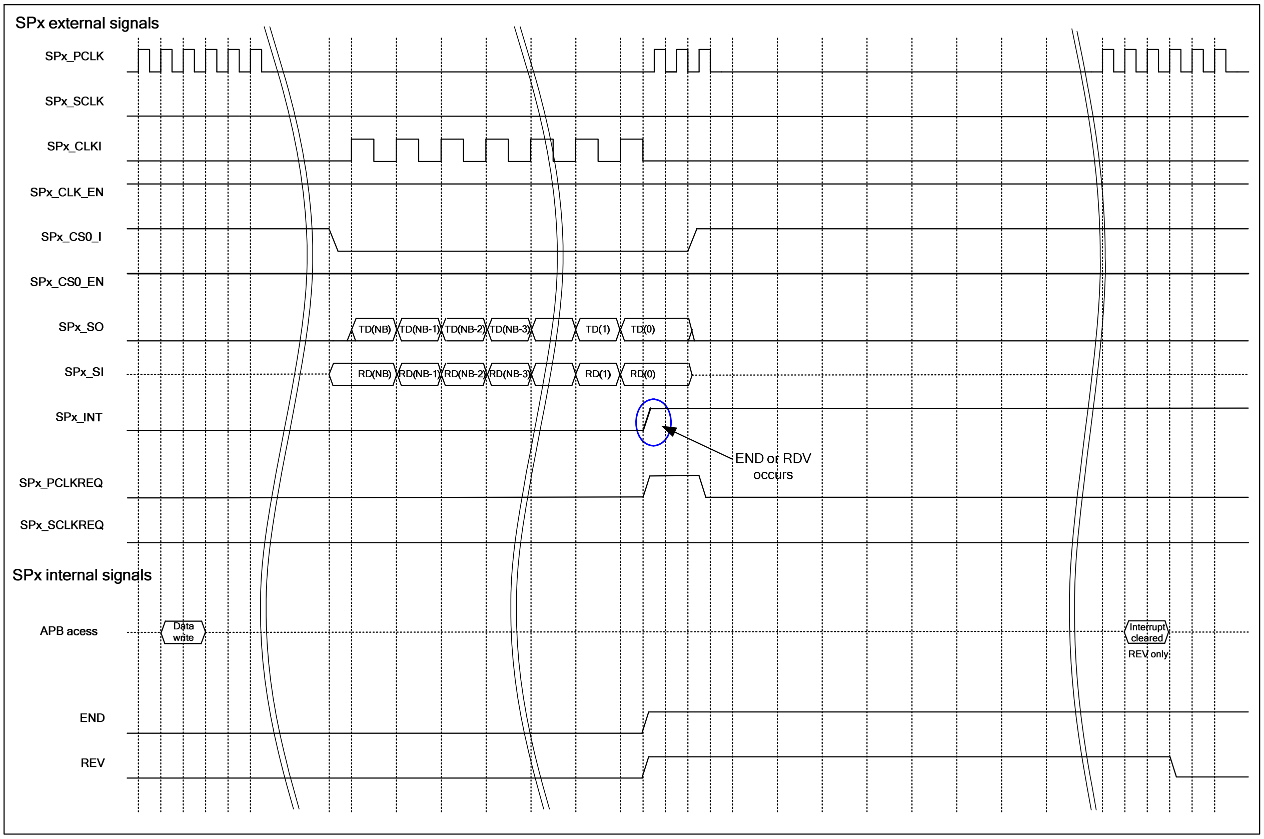
While the WRT bit is set to 0, SPx_SO outputs “0”. In the same manner, if transmission is triggered by setting the WRT bit to 1 while the RD bit is set to 0, data sent via SPx_SI is ignored. At this time, an RDV interrupt request is not output. The START bit is reset to 0 in synchronization with SPx_PCLK when transfer of the frame for which transfer was started ends.

The RST bit of the SPx_CONTROL register resets the controller (registers) other than the SPx_MODE register and interrupts.

5.1.2 Slave transfer in CPU mode

Figure 5-3 shows the timing of slave transfer in CPU mode.

Figure 5-3. Slave Transfer Timing in CPU Mode (CKn_DLY = 0)



Slave transfer in CPU mode is enabled by setting the DMA bit to 0 and M_S bit to 1 in the mode register. In slave mode, the SPI is controlled by SPx_CLKI and SCx_CS0_I input from the SPI module.

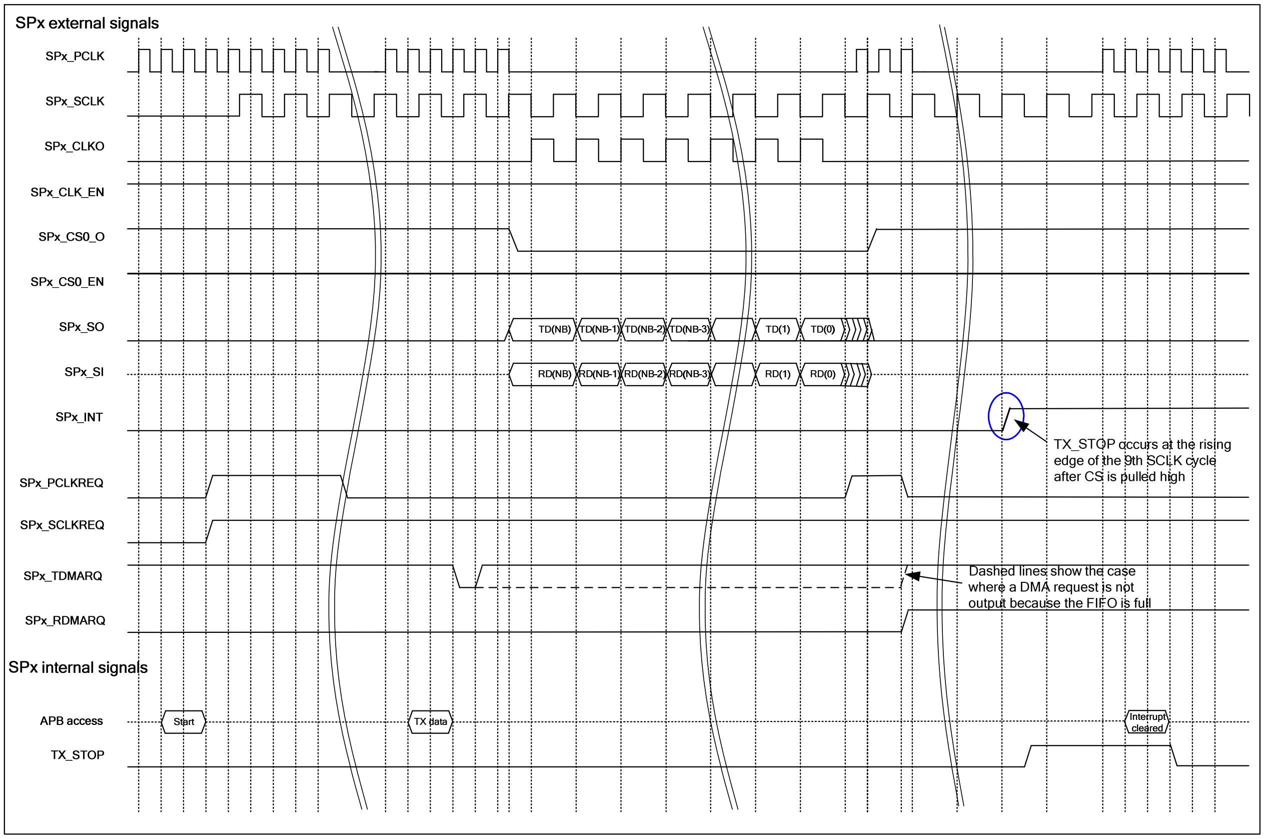
The internal operation is the same as that of master transfer in CPU mode. However, a TERR interrupt occurs at the end of frame transmission.

Caution Set the RST bit when frame transfer is not being executed.

5.1.3 Master transfer in DMA mode (normal transfer)

Figure 5-4 shows the timing of normal master transfer in DMA mode.

Figure 5-4. Master Transfer Timing in DMA Mode (Normal Transfer) (CKn_DLY = 0)



Master transfer in DMA mode is enabled by setting the DMA bit to 1 and M_S bit to 0 in the mode register. The SPI interface operation is the same as that of master transfer in CPU mode.

Transmission starts as soon as data is written to the transmit FIFO via DMA.

Reception starts as soon as the RD and START bits are set to 1 in the SPx_CONTROL register. Data is not received if the receive FIFO is full.

For transmission/reception, data is transferred according to the conditions for transmission.

When a serial transfer transaction ends, transfer of the next frame starts if the next transmit data is stored in the transmit FIFO and the receive FIFO is not full. The interval for the next transfer can be specified from 1 to 16 SPx_SCLK cycles by using the CSW bits of the SPI polarity register.

The RDV, END, or TERR interrupt does not occur during master transfer in DMA mode, but the TX_STOP and RX_STOP interrupts do occur.

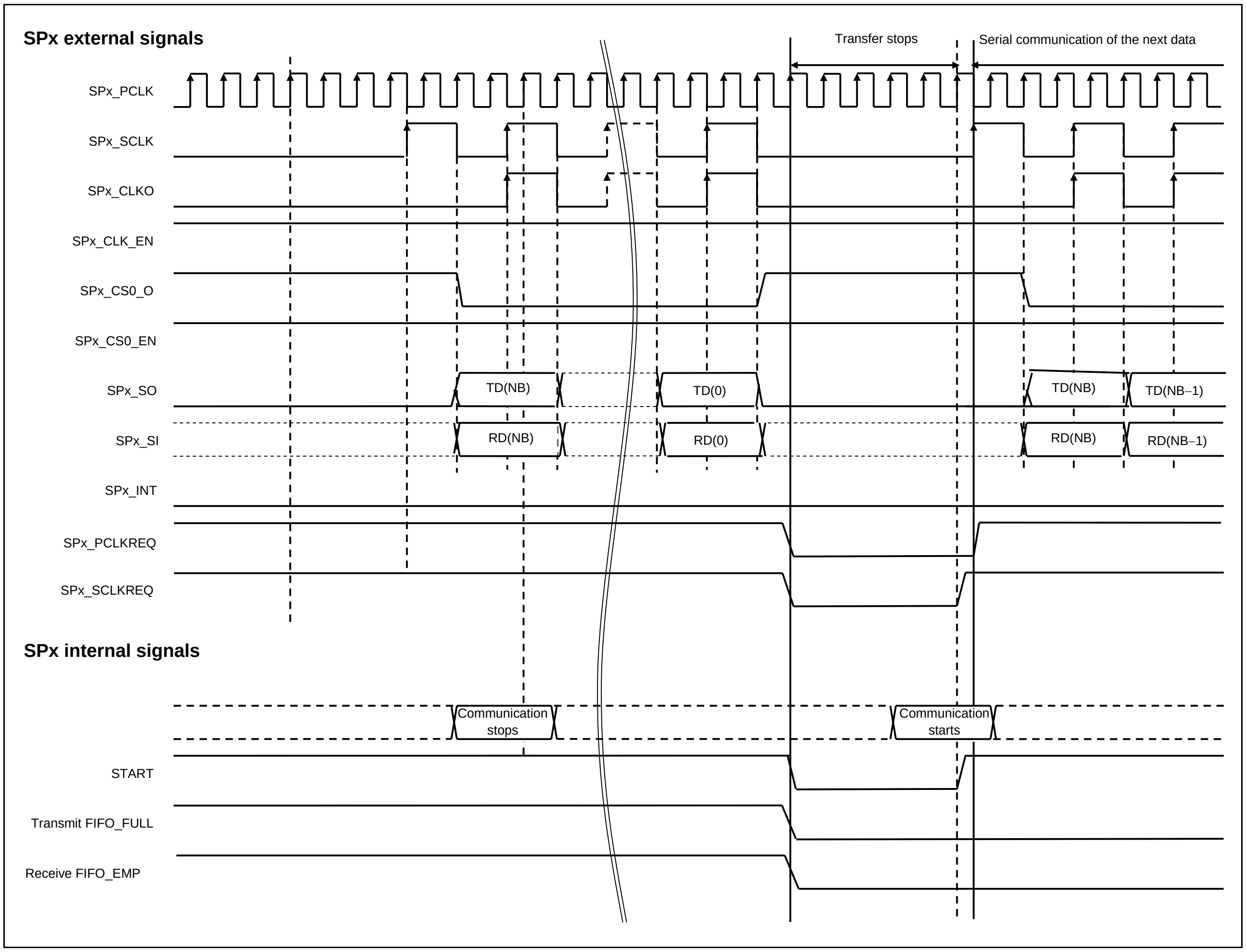
A TX_UDR interrupt occurs upon transmission of a frame that sends null data if the transaction started while the transmit FIFO was empty.

An RX_OVR interrupt occurs upon reception of a frame if the transaction started while the receive FIFO was full.

5.1.4 Master transfer in DMA mode (STOP to START)

Figure 5-5 shows the timing of STOP to START master transfer in DMA mode.

Figure 5-5. Master Transfer Timing in DMA Mode (STOP to START)



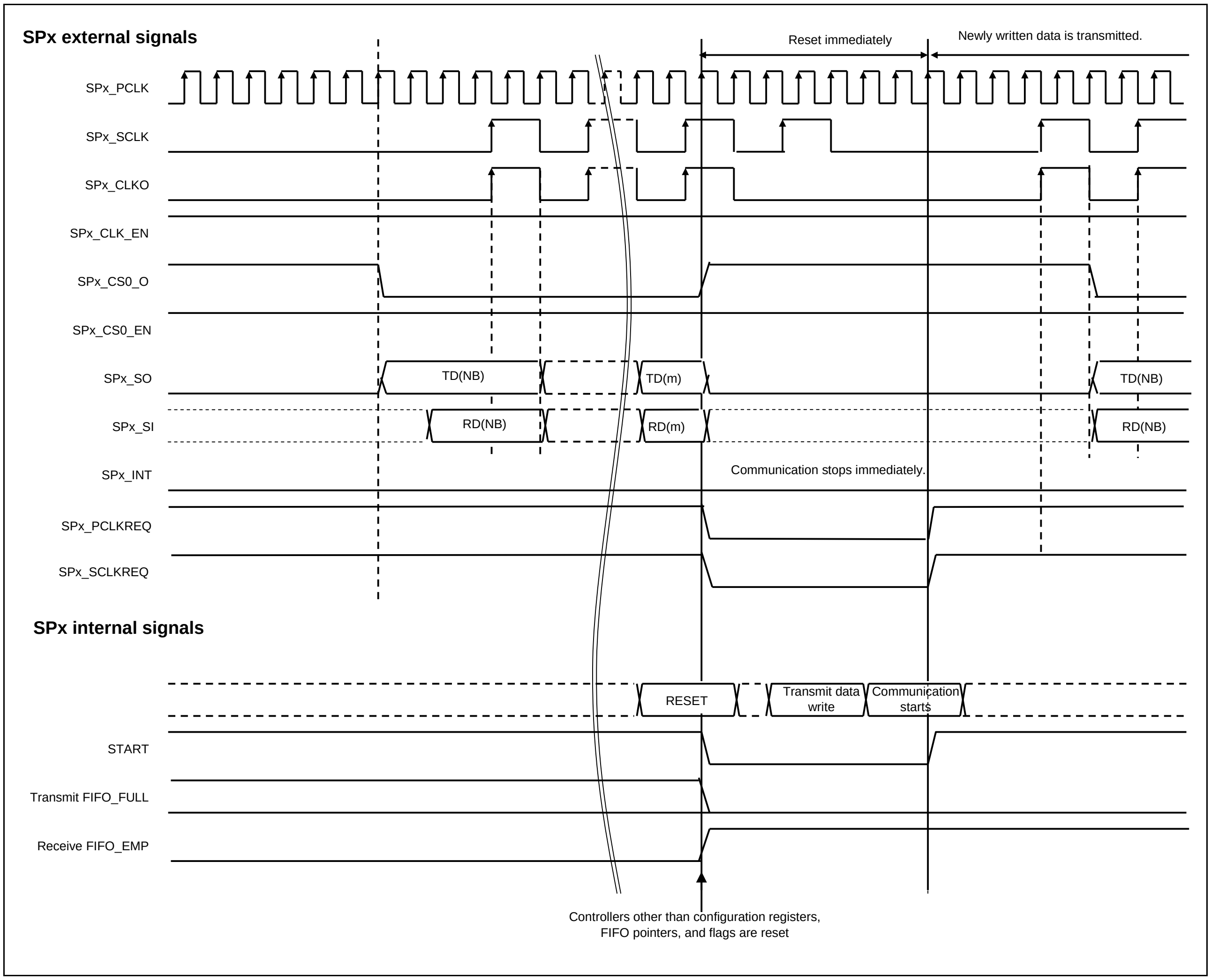
If the STOP bit of the SPx_CONTROL register is set to 1 while SPI transfer is being executed, transfer ends when transfer of the current frame is complete. The received data is stored in the receive FIFO.

If the START bit of the SPx_CONTROL register is set to 1 immediately after the STOP bit was set to 1, transfer starts from the pointer to the position next to the position where the previous transfer was stopped.

5.1.5 Master transfer in DMA mode (RESET to START)

Figure 5-6 shows the timing of RESET to START master transfer in DMA mode.

Figure 5-6. Master Transfer Timing in DMA Mode (RESET to START)

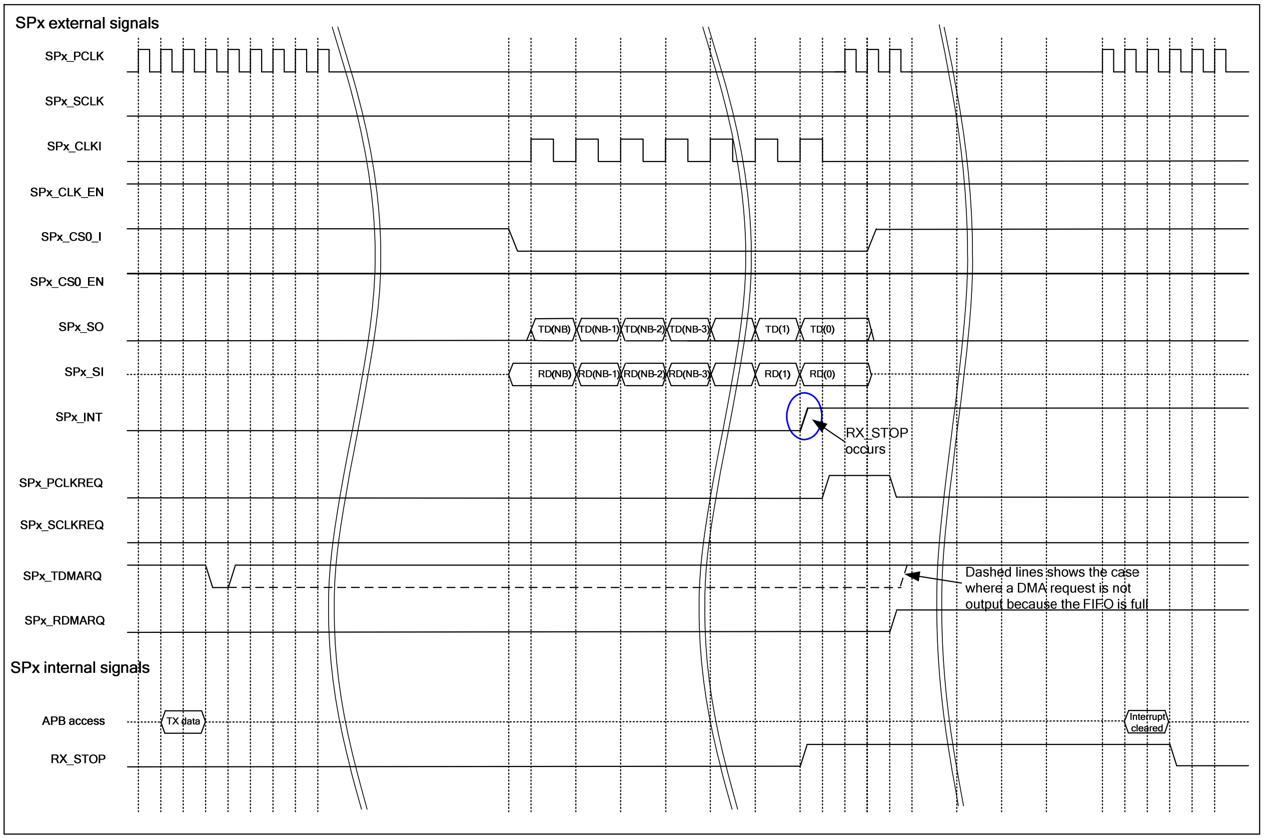


If the RST bit of the SPx_CONTROL register is set to 1 while SPI transfer is being executed, transfer ends immediately. At the same time, all the controllers (registers) other than configuration registers are reset.

5.1.6 Slave transfer in DMA mode (normal transfer)

Figure 5-7 shows the timing of normal slave transfer in DMA mode.

Figure 5-7. Slave Transfer Timing in DMA Mode (Normal Transfer) (CKn_DLY = 0)



Slave transfer in DMA mode is enabled by setting the DMA bit to 1 and M_S bit to 1 in the mode register. In slave mode, the SPI is controlled by SPx_CLKI and SCx_CS0_I input from the SPI module. The operation of the SPI interface is the same as that of master transfer in DMA mode.

The RDV and END interrupts do not occur during slave transfer in DMA mode, but the TX_UDR, RX_OVR, and TERR interrupts occur.

5.1.7 Fixed-length transmission in DMA (master) mode

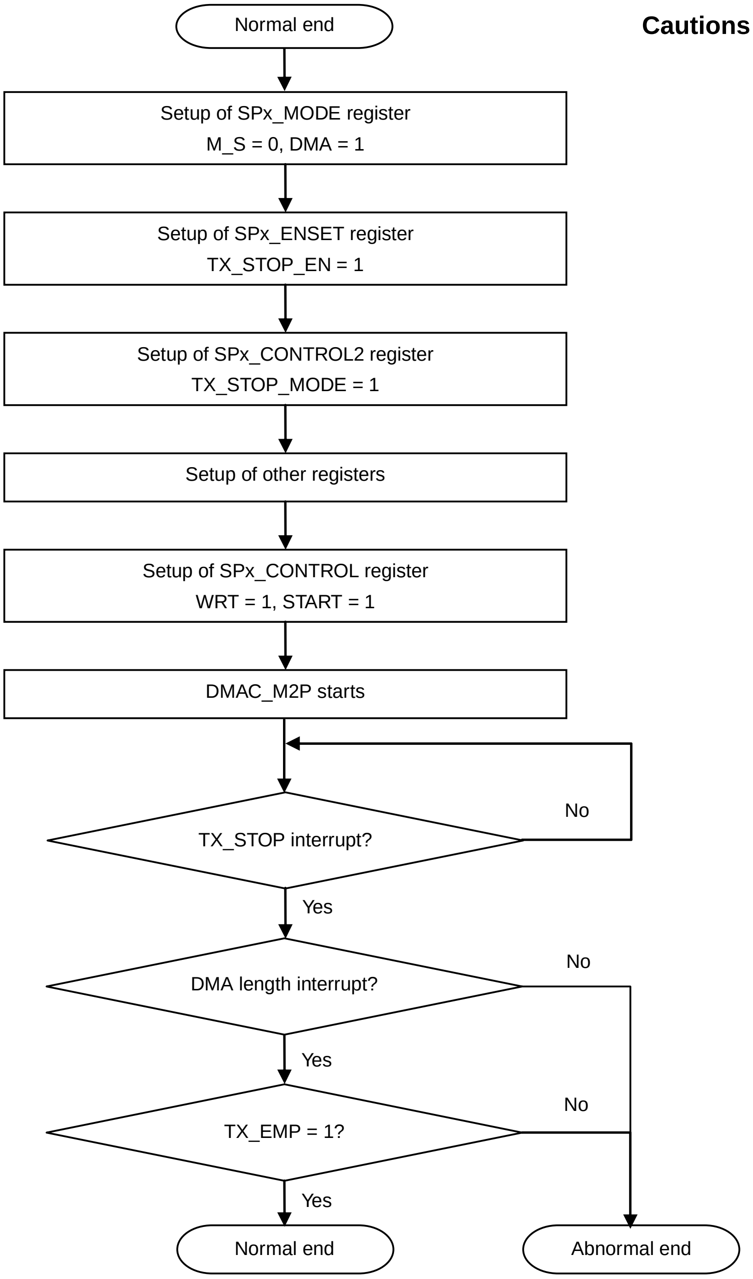
In this mode, the total number of transfer data items (data length) in the DMA controller can be matched with the number of SPI transmission frames.

This mode can be used by setting the registers as shown below.

In this mode, transmission is stopped upon reception of frame_end of a frame that indicates the last frame stored in the transmit FIFO, and therefore the transmit FIFO is judged to be empty.

When SPI transmission is stopped in this way, a TX_EMP interrupt occurs.

The following shows the flow for processing fixed-length transmission in DMA (master) mode.



Cautions 1. Make sure that the transmit FIFO does not become empty before transfer of the data length set to the DMA controller is completed. If the transmit FIFO becomes empty before the DMA controller finishes transferring the specified data length, SPI transmission is aborted and fixed-length transmission is not performed.

2. Since SPI transmission is stopped when the transmit FIFO becomes empty, the transfer request (TX_DAMREQ) is output once more than the transmit data count.

3. If the transmit FIFO becomes empty and thus SPI transmission stops at the same time as data is written to the transmit FIFO via DMA, the SPI stops even though the transmit FIFO is no longer empty. To recognize this state, check if the TX_EMP bit of the SPI_CONTROL register is set to 1 after a TX_STOP interrupt occurs. If the TX_EMP bit shows 0, it means that data exists in the transmit FIFO, and the above conflict has occurred.

5.1.8 Fixed-length reception in DMA (master) mode

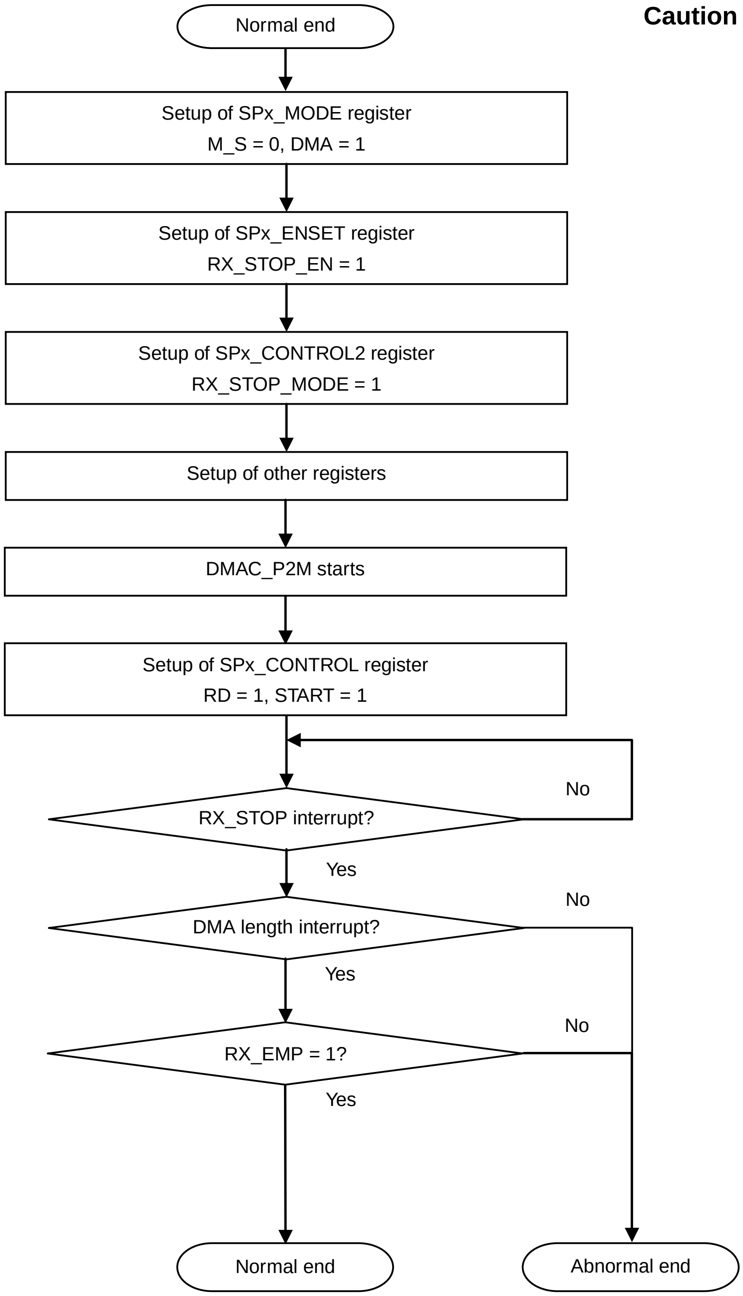
In this mode, the total number of transfer data items (data length) in the DMA controller can be matched with the number of SPI reception frames.

This mode can be used by setting the registers as shown below.

In this mode, reception is stopped upon reception of the number of frames specified in the RX_FIFO_FULL register. When SPI reception is stopped in this way, an RX_STOP interrupt occurs.

Even if reception is stopped because the receive FIFO becomes full, a DMA request continues to be output until the receive FIFO becomes empty, so the ACPU does not need to receive the data.

The number of receive frames can be specified from 1 to 65,536 words by setting the RX_FIFO_FULL register. The following shows the flow for processing fixed-length reception in DMA (master) mode.



Caution **Make sure that the receive FIFO does not become full before transfer of the data length set to the DMA controller is completed. If the receive FIFO becomes full before the DMA controller finishes transferring the specified data length, SPI reception is aborted and fixed-length reception is not performed.**

5.1.9 Continuous CPU transmission via fixed-length transmission in DMA (master) mode

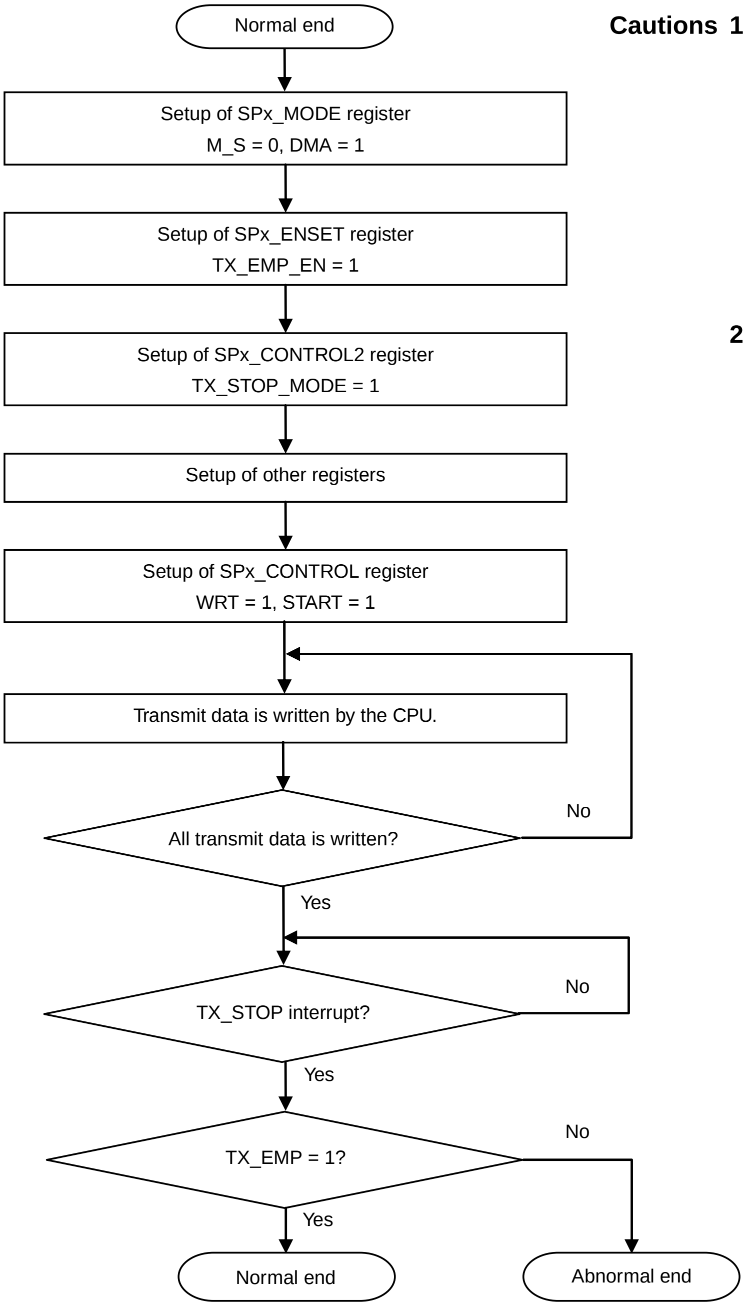
In this mode, data can be continuously transmitted via fixed-length transmission by being written by the CPU.

This mode can be used by setting the registers as shown below.

In this mode, transmission is stopped upon reception of frame_end of a frame that indicates the last frame stored in the transmit FIFO, and therefore the transmit FIFO is judged to be empty.

When SPI transmission is stopped in this way, a TX_STOP interrupt occurs.

The following shows the flow for processing continuous CPU transmission via fixed-length transmission in DMA (master) mode.


Normal end
Setup of SPx_MODE register
M_S = 0, DMA = 1
Setup of SPx_ENSET register
TX_EMP_EN = 1
Setup of SPx_CONTROL2 register
TX_STOP_MODE = 1
Setup of other registers
Setup of SPx_CONTROL register
WRT = 1, START = 1
Transmit data is written by the CPU.
All transmit data is written?
No
Yes
TX_STOP interrupt?
No
Yes
TX_EMP = 1?
No
Yes
Normal end
Abnormal end

Cautions 1. Make sure that the transmit FIFO does not become empty before the CPU finishes writing data to the transmit FIFO. If the transmit FIFO becomes empty before the CPU finishes writing data to the transmit FIFO, SPI transmission is aborted and fixed-length transmission is not performed

2. If the transmit FIFO becomes empty and thus SPI transmission stops at the same time as data is written to the transmit FIFO via the CPU, SPI stops even though the transmit FIFO is no longer empty. To recognize this state, check if the TX_EMP bit of the SPI_CONTROL register is set to 1 after a TX_STOP interrupt occurs. If the TX_EMP bit shows 0, it means that data exists in the transmit FIFO, and the above conflict has occurred.

Revision History

Date	Revision	Comments
February 10, 2009	1.0	−
April 27, 2009	2.0	Incremental update from comments to the 1.0..
September 30, 2009	3.0	Incremental update from comments to the 2.0..

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