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RENESAS

User's Manual

Multimedia Processor for Mobile Applications

UART Interface

EMMA Mobile™1

Document No. S19262EJ3V0UM00 (3rd edition)
Date Published September 2009

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Printed in Japan

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M8E0904E

PREFACE

Readers

This manual is intended for hardware/software application system designers who wish to understand and use the UART interface functions of EMMA Mobile1 (EM1), a multimedia processor for mobile applications.

Purpose

This manual is intended to explain to users the hardware and software functions of the UART interface of EM1, and be used as a reference material for developing hardware and software for systems that use EM1.

Organization

This manual consists of the following chapters.

- Chapter 1 Overview
- Chapter 2 Pin functions
- Chapter 3 Registers
- Chapter 4 Description of functions
- Chapter 5 Usage

How to Read This Manual

It is assumed that the readers of this manual have general knowledge of electricity, logic circuits, and microcontrollers.

To understand the functions of the UART interface of EM1 in detail

→ Read this manual according to the **CONTENTS**.

To understand the other functions of EM1

→ Refer to the user's manual of the respective module.

To understand the electrical specifications of EM1

→ Refer to the Data Sheet.

Conventions

Data significance:	Higher digits on the left and lower digits on the right
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring particular attention
Remark:	Supplementary information
Numeric representation:	Binary ... xxxx or xxxxb
	Decimal ... xxxx
	Hexadecimal ... xxxxH
Data type:	Word … 32 bits
	Halfword … 16 bits
	Byte … 8 bits

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name		Document No.
MC-10118A Data sheet		S19657E
μPD77630A Data sheet		S19686E
User's manual	Audio/Voice and PWM Interfaces	S19253E
	DDR SDRAM Interface	S19254E
	DMA Controller	S19255E
	I^2C Interface	S19256E
	ITU-R BT.656 Interface	S19257E
	LCD Controller	S19258E
	MICROWIRE	S19259E
	NAND Flash Interface	S19260E
	SPI	S19261E
	UART Interface	This manual
	Image Composer	S19263E
	Image Processor Unit	S19264E
	System Control/General-Purpose I/O Interface	S19265E
	Timer	S19266E
	Terrestrial Digital TV Interface	S19267E
	Camera Interface	S19285E
	USB Interface	S19359E
	SD Memory Card Interface	S19361E
	PDMA	S19373E
	One Chip (MC-10118A)	S19598E
	One Chip (μPD77630A)	S19687E

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CHAPTER 1 OVERVIEW

This chapter describes the Universal Asynchronous Receiver/Transmitter (UART) for EM1.

1.1 Function Overview

The UART block incorporated in EM1 has two 64-byte FIFO buffers, one for transmission and one for reception, and is compatible with TL16C750, a general-purpose UART chip.

The IrDA SIR encoder/decoder is provided for the serial interface, which enables transmission and reception by using the RZI (Return-to-Zero-Inverted) signal.

1.2 Features

- Three UART blocks: UART0, UART1, and UART2
- Two 64-byte FIFO buffers, one for transmission and one for reception
  The following operating modes are available:
  - Non-FIFO mode (16450 mode)
  - 16-byte FIFO mode (16550 mode)
  - 64-byte FIFO mode
- Programmable auto-RTS and auto-CTS
- Standard asynchronous communication control bits (start, stop, and parity bits) can be added to or deleted from transmitted and received serial data. The following items can be specified:
  - Character length: 5, 6, 7 or 8 bits
  - Parity bit: Even parity, odd parity, or no parity bit
  - Stop bit: 1 or 2 bits
  - Baud rate: Reference clock frequency division ratio selectable from 1 to $(2^{16} - 1)$
- Modem control interface (CTS, RTS, DSR, DTR, RI, DCD)
- IrDA SIR encoder/decoder (2.4 to 115.2 kbps)

1.3 I/O Signals

The following signals are used for UART communication.

- UARTx_SIN: UARTx data input (external pins)
- UARTx_SOUT: UARTx data output (external pins)
- UARTx_CTSB: UARTx transmission enable input (low active) (external pins)
- UARTx_RTSB: UARTx transmission request output (low active) (external pins)
- XIN: Operating clock input from ASMU (U7x_SCLK) (internal clock input)
- MR: Master reset input from ASMU (U7x_RSTZ) (internal reset input)

Remark x = 0 to 2

2.1 UART Interface Pins

Pin Name	I/O	After Reset	Function	Alternate Pin Function
URT0_SRIN	Input	–	Serial data	–
URT0_SOUT	Output	0	Serial data	–
URT0_CTSB	Input	–	Prepared to transmit or receive connected device data	GIO_P85 URT1_SRIN
URT0_RTSB	Output	0	Prepared to transmit or receive data	GIO_P86 URT1_SOUT
URT1_SRIN	Input	–	Serial data	GIO_P85 URT0_CTSB
URT1_RTSB	Output	0	Serial data	GIO_P86 URT0_RTSB
URT2_SRIN	Input	–	Serial data	GIO_P108 NAND_ALE
URT2_SOUT	Output	0	Serial data	GIO_P109 NAND_CLE
URT2_CTSB	Input	–	Prepared to transmit or receive connected device data	GIO_P110 NAND_D0
URT2_RTSB	Output	0	Prepared to transmit or receive data	GIO_P111 NAND_D1

CHAPTER 3 REGISTERS

UART register addresses use half-word boundaries.

3.1 Registers

The offset addresses 0000H to 0034H are assigned to UART registers, and 0040H to 0050H are assigned to IR encoder/decoder registers.

Do not access reserved registers. The value 0000_0000H is returned for a read access.

Do not write any value other than 0 to the reserved bits in each register.

Base addresses: 5000_0000H (UART0), 5001_0000H (UART1), 5002_0000H (UART2)

Address	Register Name	Register Symbol	R/W	After Reset
0000H	Receive buffer register	RBR	R	Undefined
	Transmit hold register	THR	W	
0004H	Interrupt enable register	IER	R/W	0000H
0008H	Interrupt identification register	IIR	R	0001H
000CH	FIFO control register	FCR	R/W	0000H
0010H	Line control register	LCR	R/W	0000H
0014H	Modem control register	MCR	R/W	0000H
0018H	Line status register	LSR	R	0060H
001CH	Modem status register	MSR	R	00xxH[Note 1]
0020H	Scratch register	SCR	R/W	0000H
0024H	Divisor latch LS byte register	DLL	R/W[Note 2]	0000H
0028H	Divisor latch MS byte register	DLM	R/W[Note 2]	0000H
002CH	Hardware control register	HCR0	R/W	0000H
0030H	Hardware status register 2	HCR2	R	0000H
0034H	Hardware status register 3	HCR3	R	0000H
0038H	Reserved	–	–	–
003CH	Reserved	–	–	–
0040H	IR control register 0	IRCR0	R/W	0000H
0044H	IR control register 1	IRCR1	R/W	0002H
0048H	IR control register 2	IRCR2	R/W	0000H
004CH	IR control register 3	IRCR3	R/W	0000H
0050H	IR control register 4	IRCR4	R/W	0000H

Notes 1. Differs depending on the condition of the connected device.

2. Bit 7 (DLAB) of the LCR register must be set to 1 before setting up the DLL and DLM registers. The DLAB bit must be set to 0 after writing to the DLL and DLM registers. For details, see **3.2.5 Line control register**.

3.2 UART Registers

3.2.1 Receive buffer/transmit hold register

This register (RBR/THR: 5000_0000H (UART0), 5001_0000H (UART1), 5002_0000H (UART2)) is used to read received data and write data to transmit.

This register functions as the receive buffer register (RBR) when read, or as the transmit hold register (THR) when written. In FIFO mode (bit 0 of FCR register = 1), the FIFO buffers are accessed.

15	14	13	12	11	10	9	8
0/D7	0/D6	0/D5	0/D4	0/D3	0/D2	0/D1	0/D0

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Name	R/W	Bit	After Reset	Function
0/D[7:0]	R	15:8	Undefined	Reads received data in 2-byte units. These bits are not used for 1-byte access. Zeroes are returned.
	W			Writes data to transmit in 2-byte units. These bits are not used for 1-byte access. Writing is ignored.
D[7:0]	R	7:0	Undefined	Reads received data.
	W			Stores data to transmit.

○ Operation in non-FIFO mode (bit 0 of FCR register = 0)

Received data is read out by reading this register, and data written to this register is stored as data to transmit. Data of the lowest bit (D0) is transmitted or received first.

Only the lower bytes (D[7:0]) are used. This register can be accessed in byte units via the host bus interface. If this register is accessed in 2-byte units in non-FIFO mode, the higher bytes (0/D[7:0]) become invalid (all zeros returned when read, ignored when written) and only the lower bytes are used.

○ Operation in FIFO mode (bit 0 of FCR register = 1)

Received data is read out from the receive FIFO by reading this register, and data written to this register is stored into the transmit FIFO as data to transmit. This register can be accessed in 1- or 2-byte units via the host bus interface. Data of the lowest bit (D0) is transmitted or received first.

If this register is read in byte units, all zeros are returned from the higher bytes (0/D[7:0]) and data in the lower bytes (D[7:0]) becomes valid. If this register is written, the higher bytes become invalid and only the lower bytes are used.

The FIFO capacity is selected by using bit 5 of the FCR register.

The 16-byte FIFO mode is selected (16550 mode) by setting bit 5 of the FCR register to 0, and the 64-byte FIFO mode is selected by setting bit 5 of the FCR register to 1.

Cautions 1. If data is written to the transmit FIFO when it is full or if 2-byte data is written to the transmit FIFO when only 1 byte of space is available, an overrun error occurs and no data is written to the transmit FIFO. When an overrun error occurs, bit 7 of the HCR3 register is set to 1.

2. When data is read from the empty receive FIFO or if the reading of 2-byte data from the receive FIFO is attempted when only 1 byte of data is stored, an underrun error occurs and data is not read from the receive FIFO. (All zeros are output to the host bus interface.) When an underrun error occurs, bit 7 of the HCR2 register is set to 1.

3. If the number of transmitted or received data bits is 5 to 7 bits, data in the lower bits is transmitted or received and bits exceeding the specified transfer bit count are discarded.

Example When the transfer bit count is set to 5 (bits 1 and 0 (WLS) of LCR register = 00b):
On the transmission side, data of bits 7 to 5 is discarded and data of bits 4 to 0 is transmitted.
On the reception side, “0” is written to bits 7 to 5 and valid data is written to bits 4 to 0.

3.2.2 Interrupt enable register

This register (IER: 5000_0004H (UART0), 5001_0004H (UART1), 5002_0004H (UART2)) enables the issuance of interrupt requests. Each interrupt can be set up individually for each interrupt source.

The interrupt sources corresponding to bits to which 1 is written are enabled.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				EDSSI	ELSI	ETBEI	ERBI

Name	R/W	Bit	After Reset	Function
Reserved	R	15:8	0	Reserved. When these bits are read, 0 is returned for each bit.
Reserved	R/W	7:4	0	Reserved. Written data is ignored.
EDSSI	R/W	3	0	Specifies whether to enable the modem status interrupt. 0: Disables the modem status interrupt. 1: Enables the modem status interrupt.
ELSI	R/W	2	0	Specifies whether to enable the reception error (receiver line status) interrupt. 0: Disables the reception error interrupt. 1: Enables the reception error interrupt.
ETBEI	R/W	1	0	Specifies whether to enable the transmit buffer empty (transmit hold register (THR) empty) interrupt. 0: Disables the transmit buffer empty interrupt. 1: Enables the transmit buffer empty interrupt.
ERBI	R/W	0	0	Specifies whether to enable the reception completion (received data available) and timeout interrupts. 0: Disables the reception completion and timeout interrupts. 1: Enables the reception completion and timeout interrupts.

Caution By setting bit 0 to "0", reception completion and timeouts can be excluded from the interrupt sources. However, when bit 4 of the HCR0 register is set to 1 (receiver timeout DMA REQ disable), a timeout error is added to the interrupt sources, regardless of the setting of bit 0.

Remark A timeout error is detected when either of the following conditions is satisfied while the FIFO stores at least one character:

<1> The most recent serial character is received before at least the four continuous character times.

<2> The host read the FIFO most recently before four continuous character times.

Four continuous character times is equivalent to four characters of a 12-bit received character (start: 1 bit, data: 8 bits, parity: 1 bit, stop: 2 bits), that is, 768 cycles (for a 16× clock) (12 × 4 × 16 = 768 cycles (for a 16× clock)).

3.2.3 Interrupt identification register

This register (IIR: 5000_0008H (UART0), 5001_0008H (UART1), 5002_0008H (UART2)) is used to identify interrupt sources.

The FIFO operating mode and interrupt sources can be checked by reading this register.

When multiple interrupts sources are generated, the interrupt source that has the highest priority is output to this register.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
FIFOs Enabled[1:0]		64 Byte FIFO Enabled	Reserved	Interrupt ID[3:0]			

Name	R/W	Bit	After Reset	Function
Reserved	R	15:8	0	Reserved. When these bits are read, 0 is returned for each bit.
FIFOs Enabled[1:0]	R	7:6	00b	Indicates the FIFO operating mode. 00b: Non-FIFO mode (16450 mode) 11b: 16-byte/64-byte FIFO mode (See bit 5.)
64 Byte FIFO Enabled	R	5	0	Indicates the FIFO operating mode. This bit is enabled when bits 7 and 6 are set to 11b. 0: 16-byte FIFO mode (16550 mode) 1: 64-byte FIFO mode
Reserved	R	4	0	Reserved. When this bit is read, 0 is returned.
Interrupt ID[3:0]	R	3:0	0001b	Among the interrupts that have occurred, these bits indicate the ID of the interrupt source that has the highest priority.

Table 3-1. FIFO Operating Mode (Bits 7 to 5)

Bits 7 to 5	FIFO Operating Mode
000	Non-FIFO mode (16450 mode)
110	16-byte FIFO mode (16550 mode)
111	64-byte FIFO mode

Table 3-2. Interrupt Indication and Prioritization of Interrupt Sources (Bits 3 to 0 of IIR)

IIR[3:0]	Priority	Interrupt Type	Interrupt Source	Interrupt Reset Method
0001 (1h)	None	None	None	None
0110 (6h)	1	Reception error (receiver line status)	When at least one of the following occurs: • Overrun • Parity error • Framing error • Break interrupt	When the line status register (LSR) is read
0100 (4h)	2	Reception completion (received data available)	• In non-FIFO mode When data reception in the receive buffer register is completed • In FIFO mode When the amount of data in the receive FIFO exceeds the trigger level	• In non-FIFO mode When the receive buffer register (RBR) is read • In FIFO mode When the receive FIFO is read and the amount of data in the receive FIFO becomes less than the trigger level
1100 (Ch)		Timeout	When data reception timed out while the receive FIFO was used	When the receive FIFO is read
0010 (2h)	3	Transmit buffer empty (transmit hold register (THR) empty)	Transmit hold register (THR) or transmit FIFO is empty	When the IIR register is read or data is written in the transmit hold register (THR) or transmit FIFO
0000 (0h)	4	Modem status	When at least one of the following occurs: • △CTS • △DSR (internal signal) • △DCD (internal signal) • Trailing edge RI (internal signal)	When the modem status register (MSR) is read

Caution A transmit buffer empty interrupt (bits 3 to 0 of IIR register = 0010) is canceled by reading the IIR register or writing data to the transmit hold register (THR) or transmit FIFO. Specifically, the following operation is performed for reading the IIR register.

If the transmit buffer is empty when the IIR register is read to check the interrupt source, the read operation masks the transmit buffer empty interrupt and this interrupt no longer occurs. This masking is canceled when data is written to the transmit buffer, and the subsequent transmit buffer empty interrupts are output.

3.2.4 FIFO control register

This register (FCR: 5000_000CH (UART0), 5001_000CH (UART1), 5002_000CH (UART2)) controls the transmit/receive FIFO.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Receiver Trigger		64 Byte FIFO Enabled	Reserved	DMA Mode Select	Transmitter FIFO Reset	Receiver FIFO Reset	FIFO Enable

Name	R/W	Bit	After Reset	Function
Reserved	R	15:8	0	Reserved. When these bits are read, 0 is returned for each bit.
Receiver Trigger *	R/W	7:6	00	Valid only in FIFO mode (bit 0 of FCR register = 1). Specifies the threshold (trigger level) of data stored in the receive FIFO in order to issue an interrupt request or a reception DMA request. • In 16-byte FIFO mode (bit 5 of FCR register = 0) 00: 1 byte 01: 4 bytes 10: 8 bytes 11: 14 bytes • In 64-byte FIFO mode (bit 5 of FCR register = 1) 00: 1 byte 01: 16 bytes 10: 32 bytes 11: 56 bytes
64 Byte FIFO Enable *	R/W	5	0	Valid only in FIFO mode (bit 0 of FCR register = 1). Specifies the FIFO capacity. 0: 16 bytes (16550 mode) 1: 64 bytes
Reserved	R/W	4	0	Reserved. Written data is ignored.
DMA Mode Select *	R/W	3	0	Specifies the DMA mode in FIFO mode. The DMA mode is specified by setting this bit with bits 3 and 2 of the HCR0 register.
Transmitter FIFO Reset	R/W	2	0	Setting this bit to 1 generates a synchronization reset pulse (1 VBCLK cycle) and resets the transmit FIFO and FIFO address counter. This bit is automatically reset to 0. **Caution The transmit shift register (TSR) is not reset. If a reset occurs during transmission, one frame that has only zeros might be transmitted after the data in the TSR register has been transmitted.**
Receiver FIFO Reset	R/W	1	0	Setting this bit to 1 generates a synchronization reset pulse (1 VBCLK cycle) and resets the receive FIFO and FIFO address counter. This bit is automatically reset to 0. **Caution The receive shift register (RSR) is not reset. If a reset occurs during reception, data being received is correctly stored in the receive FIFO after the reset.**
FIFO Enable *	R/W	0	0	Selects the FIFO operating mode. 0: Non-FIFO mode (16450 mode) 1: 16-/64-byte FIFO mode (selected by bit 5 of the FCR register)

*** If a register value is changed during operation, normal operation is not guaranteed. In this case, initialize the register.**

Table 3-3. Reception Trigger Level Settings (Bits 7 and 6 of FCR)

Bits 7 to 6 of IIR	16-byte FIFO Mode (Bit 5 of FCR Register = 0) Trigger Level (Bytes)	64-byte FIFO Mode (Bit 5 of FCR Register = 1) Trigger Level (Bytes)
00	01	01
01	04	16
10	08	32
11	14	56

Table 3-4. DMA Mode Settings (Bit 3 of FCR and Bits 3 and 2 of HCR0)

Bit 3 of FCR register	Bits 3 and 2 of HCR0	Receive DMA Request	Transmit DMA Request
0	00	Mode 0	
1	00	Mode 1	
0	01	Mode 0	Mode 1
1	10	Mode 1	Mode 0
Others (Setting prohibited)		–	–

Table 3-5. DMA Modes and DMA Request Generation Conditions

Mode		DMA Request Generation Condition	DMA Request Release Condition
When the DMA access data width is one byte (bit 5 of HCR0 = 0)			
Receive DMA request	Mode 0	The receive FIFO stores 1 or more bytes of data.	The receive FIFO is empty.
	Mode 1	The amount of data in the receive FIFO reached the trigger level or a timeout event occurred[Note 1].	The receive FIFO is empty.
Transmit DMA request	Mode 0	The transmit FIFO is empty.	The transmit FIFO stores 1 or more bytes of data.
	Mode 1	The transmit FIFO is empty.	The transmit FIFO is full.
When the DMA access data width is two bytes (bit 5 of HCR0 = 1).			
Receive DMA request	Mode 0	The receive FIFO stores 2 or more bytes of data.	The receive FIFO stores 1 or fewer bytes of data[Note 2].
	Mode 1	The trigger level is reached or a timeout event occurs[Note 1] when the receive FIFO stores 2 or more bytes of data.	The receive FIFO stores 1 or fewer bytes of data[Note 2].
Transmit DMA request	Mode 0	The transmit FIFO is empty.	The transmit FIFO stores 2 or more bytes of data.
	Mode 1	The transmit FIFO is empty.	The transmit FIFO full

Notes 1. The timeout event can be excluded from the reception DMA request issue conditions by setting bit 4 of the HCR0 register.

Bit 4 = 0: The timeout event is included in the reception DMA request issue conditions.

Bit 4 = 1: The timeout event is excluded from the reception DMA request issue conditions and added to the interrupt sources.

2. If an odd number of data bytes is received in the 2-byte access mode, the reception DMA request is canceled when the amount of data remaining in the receive FIFO becomes 1 byte. When receiving an odd number of data bytes, use 1-byte access or notify the timeout event by using an interrupt (bit 4 of HCR0 register = 1) and read the timeout data by servicing the interrupt.

Caution In the non-FIFO mode, operation equivalent to mode 0 is performed regardless of the settings of bit 3 in the FCR register and bits 3 and 2 in the HCR0 register.

- **A reception DMA request is issued when receiving 1-byte data in the receive buffer register is completed. The request is canceled when the receive buffer register is empty.**
- **A transmission DMA request is issued when the request transmit buffer is empty. The request is canceled when at least 1-byte data is stored in the transmit buffer.**

3.2.5 Line control register

This register (LCR: 5000_0010H (UART0), 5001_0010H (UART1), 5002_0010H (UART2)) specifies the transmission/reception data format and enables access to the divisor latch.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
DLAB	Break Control	Stick Parity	EPS	PEN	STB	WLS[1:0]	

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	15:8	0	Reserved. When these bits are read, 0 is returned for each bit.
DLAB *	R/W	7	0	Setting this bit to 1 enables specifying the divisor latch (DLM/DLL registers). When this bit is set to 0 after specifying the divisor latch, access to the divisor latch is prohibited and generation of the 16x clock according to the specified value is started by the baud rate generator. **Caution The 16x clock stops after a master reset. The baud rate generator starts generating the 16x clock when it detects the change of this bit setting (from 1 to 0). After generation starts, the 16x clock will not stop unless a master reset is input.**
Break Control	R/W	6	0	Controls break state generation and transmission. The serial output (UARTx_SOUT) is forcibly set to 0 while this bit is set to 1, and such output is canceled when this bit is set to 0. This bit directly controls the SOUT output level but does not affect the internal circuits. **Caution If this bit is set to 1 during transmission, only framing errors might be detectable on the reception side. To detect breaks for sure, this bit must be set when transmission has completed (the transmit buffer empty).**
Stick Parity *	R/W	5	0	Selects the type of parity bit used to verify transmitted/received data. The setting of this bit is valid only when a parity bit is used (bit 3 = 1). An even, odd, or fixed value (high or low) is set by using bit 4. 0: Parity check using an even or odd parity bit 1: Parity check using a stick parity bit
EPS *	R/W	4	0	Selects the odd or even parity when bit 3 is set to 1 and bit 5 is set to 0. Selects the level of the stick parity when bit 3 and bit 5 are set to 1. 0: Odd parity / Stick High (fixed to 1) 1: Even parity / Stick Low (fixed to 0)
PEN *	R/W	3	0	Specifies whether to enable the parity check. 0: No parity bit. 1: Adds a parity bit on the transmission side. The parity bit is checked on the reception side.

(2/2)

Name	R/W	Bit	After Reset	Function
STB *	R/W	2	0	Specifies the number of stop bits to add to data transferred via serial transmission. 0: 1 bit 1: 2 bits Only the first stop bit is checked on the reception side, regardless of this setting.
WLS[1:0] *	R/W	1:0	0	Specifies the length of data transferred via serial transmission and reception. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits

* If a register value is changed during operation, normal operation is not guaranteed. In this case, initialize the register.

Table 3-6. Parity Type Settings (Bits 5 to 3 of LCR)

Bits 5 to 3 of LCR	Parity Type
xx0	No parity
001	Odd parity
011	Even parity
101	Stick High (fixed to “1”)
111	Stick Low (fixed to “0”)

xx: Don’t Care

Table 3-7. Settings for Transmission/Reception Data Length (Bits 1 and 0 of LCR)

WLS[1:0] of LCR	Data Length
00	5 bits
01	6 bits
10	7 bits
11	8 bits

3.2.6 Modem control register

This register (MCR: 5000_0014H (UART0), 5001_0014H (UART1), 5002_0014H (UART2)) controls the interface with modems (and other peripheral devices).

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved		AFE	Reserved	OUT2	OUT1	RTS	DTR

Name	R/W	Bit	After Reset	Function
Reserved	R	15:8	0	Reserved. When these bits are read, 0 is returned for each bit.
Reserved	R	7:6	0	Reserved. Written data is ignored.
AFE *	R/W	5	0	Specifies whether to enable auto-flow control (auto-CTS and auto-RTS). 0: Disables auto-flow control. 1: Enables auto-flow control. Auto-flow operation is controlled in detail by using bit 1 of this register and bit 6 of the HCR0 register.
Reserved	R/W	4	0	Reserved.
OUT2	R/W	3	0	Selects the level of the general-purpose output OUT2Z (internal signal). 0: High (inactive). 1: Low (active) In local loopback mode, this bit controls DCDZ (internal signal) input.
OUT1	R/W	2	0	Selects the level of the general-purpose output OUT1Z (internal signal). 0: High (inactive) 1: Low (active) In local loopback mode, this bit controls RIZ (internal signal) input.
RTS	R/W	1	0	Selects the level of UARTx_RTSB pin output (transmission request) when auto-RTS is not used (bit 5 = 0). 0: High (inactive) 1: Low (active) In local loopback mode, this bit controls the UARTx_CTSB input pin.
DTR	R/W	0	0	Selects the level of DTRZ (communication link establishment ready, internal signal) output. 0: High (inactive) 1: Low (active) In local loopback mode, this bit controls DSRZ (internal signal) input.

* If a register value is changed during operation, normal operation is not guaranteed. In this case, initialize the register.

Table 3-8. Auto-Flow Settings (Bits 5 and 1 of MCR and Bit 6 of HCR0)

Bit 5 of MCR Register	Bit 1 of MCR Register	Bit 6 of HCR0 Register	Auto-CTS	Auto-RTS
1	1	0	○	○ (Auto-RTS mode 0)
		1	○	○ (Auto-RTS mode 1)
	0	×	○	– (RTSZ output is fixed to high level.)
0	×	×	–	–

Auto-CTS operation:

While the CTSZ pin is pulled low (requesting transmission), data in the transmit buffer (THR/transmit FIFO) is transmitted. The transmission stops when the pin is pulled high. If the CTSZ pin is pulled high during transmission, data being transmitted (the data that remains in the transmit shift register) is transmitted and transmission stops.

Auto-RTS operation (valid only in the FIFO mode):

Auto-RTS mode 0

When the amount of data in the receive FIFO reaches the trigger level, the RTSZ pin is pulled high (requesting that transmission be stopped). When the data in the receive FIFO is read and the FIFO empties, the pin is pulled low (requesting transmission).

Auto-RTS mode 1

- In the 16-byte FIFO mode, the RTSZ pin is pulled high when the amount of data in the receive FIFO reaches 14 bytes, and the pin is pulled low when the amount of data becomes 13 bytes or less.
- In the 64-byte FIFO mode, the RTSZ pin is pulled high when the amount of data in the receive FIFO reaches 56 bytes, and the pin is pulled low when the amount of data becomes 55 bytes or less.

Caution
- **When auto-flow control is not used, flow control is not performed by hardware. Therefore, CTS monitoring and RTS control must be performed by software to prevent a FIFO overrun.**
- **When auto-flow is not used (bit 5 of MCR register = 0): Bit 1 of the MCR register is used to control the RTSZ output (the value set to bit 1 is reversed and the reversed level is output to RTSZ).**
- **When both a modem status interrupt (bit 3 of IER register = 1) and auto-CTS are set, auto-CTS is disabled.**
- **In the non-FIFO mode, auto-RTS is disabled.**

3.2.7 Line status register

This register (LSR: 5000_0018H (UART0), 5001_0018H (UART1), 5002_0018H (UART2)) is used to check the status of transmission and reception.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Error in Receiver FIFO	TEMT	THRE	BI	FE	PE	OE	DR

(1/2)

Name	R/W	Bit	After Reset	Function
Reserved	R	15:8	0	Reserved. When these bits are read, 0 is returned for each bit.
Error in Receiver FIFO	R	7	0	A zero is always read from this bit in non-FIFO mode. This bit is set to "1" when a break interrupt error, parity error, or framing error occurs in data read from the receive FIFO in FIFO mode. Reading this register clears this bit to “0”.
TEMT	R	6	1	This bit is set to "1" when the transmit buffer (the THR register or transmit FIFO) and transmit shift register (TSR) empty. This bit is cleared to "0" when data is written to the transmit buffer or transmit shift register.
THRE	R	5	1	This bit is set to "1" when the transmit buffer (THR register or transmit FIFO) empties. This bit is cleared to "0" when at least 1 byte of data is written to the transmit buffer.
BI *	R	4	0	This bit is set to “1” when a break interrupt occurs. Reading this register clears this bit to “0”. A break interrupt is detected when a low level signal is received for 1 frame or longer (for the total of the start bit, data stop bit, and stop bit). When a start bit (low level) is detected, the receive block assumes that data has been sent, and receives the data. While a break interrupt is being acknowledged (a low level signal is being input), the receive block continues to receive all zeros. (Reception stops when an overrun occurs.) In FIFO mode, the break interrupt information is stored in the receive FIFO with all-0 data. A break interrupt is detected when the data is read. **Caution A framing error always occurs when a break interrupt is detected. A parity error might occur, depending on the settings of bits 5 to 3 of the LCR register.**

(2/2)

Name	R/W	Bit	After Reset	Function
FE *	R	3	0	This bit is set to “1” when a framing error is detected in received data. Reading this register clears this bit to “0”. A framing error occurs when the first stop bit following the data bit or parity bit of received data is checked and it is judged to be invalid (low level). In FIFO mode, the framing error information is stored in the receive FIFO with the receive data. A framing error is detected when the data is read.
PE *	R	2	0	This bit is set to “1” when a parity error is detected in received data. Reading this register clears this bit to “0”. In FIFO mode, the parity error information is stored in the receive FIFO with the received data. A parity error is detected when the data is read.
OE *	R	1	0	This bit is set to “1” when a receive overrun error is detected. Reading this register clears this bit to “0”. A receive overrun occurs when the receive buffer register (RBR) or receive FIFO is filled with received data, data is held in the receive shift register (RSR), and the start bit of the following data is detected. When a receive overrun error occurs, received data will no longer be stored in the receive buffer register or receive FIFO. Data held in the receive shift register is stored in the receive buffer when a vacancy becomes available.
DR	R	0	0	This bit is set to "1" when at least 1 byte of received data is stored in the receive buffer register (RBR) or receive FIFO. This bit is cleared to "0" when all of the received data is read and the receive buffer empties.

* Do not poll these bits to check the interrupt source. Instead, check the source after the interrupt is detected.

3.2.8 Modem status register

This register (MSR: 5000_001CH (UART0), 5001_001CH (UART1), 5002_001CH (UART2)) is used to check the control signals connected to modems (or other peripheral devices).

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
DCD	RI	DSR	CTS	⊿DCD	TERI	⊿DSR	⊿CTS

Name	R/W	Bit	After Reset	Function
Reserved	R	15:8	0	Reserved. When these bits are read, 0 is returned for each bit.
DCD *	R	7	Undefined	Indicates the inverted level of DCDZ (internal signal) input. 0: High (inactive) 1: Low (active) In local loopback mode, the value set to bit 3 (OUT2) of the MCR register is read.
RI *	R	6	Undefined	Indicates the inverted level of RIZ (internal signal) input. 0: High (inactive) 1: Low (active) In local loopback mode, the value set to bit 2 (OUT1) of the MCR register is read.
DSR *	R	5	Undefined	Indicates the inverted level of DSRZ (internal signal) input. 0: High (inactive) 1: Low (active) In local loopback mode, the value set to bit 0 (DTR : internal signal) of the MCR register is read.
CTS *	R	4	Undefined	Indicates the inverted level of UARTx_CTSB pin input. 0: High (inactive) 1: Low (active) In local loopback mode, the value set to bit 1 (RTS) of the MCR register is read.
⊿DCD *	R	3	Undefined	This bit is set to 1 when the level of the DCDZ (internal signal) input changes (from high to low or low to high). Reading this register clears this bit to “0”.
TERI *	R	2	Undefined	This bit is set to 1 when the RIZ (internal signal) input is pulled high (inactive). Reading this register clears this bit to “0”.
⊿DSR *	R	1	Undefined	This bit is set to 1 when the level of the DSRZ (internal signal) input changes (from high to low or low to high). Reading this register clears this bit to “0”.
⊿CTS *	R	0	Undefined	This bit is set to 1 when the level of the UARTx_CTSB pin input changes (from high to low or low to high). Reading this register clears this bit to “0”.

* Do not poll these bits to check the interrupt source. Instead, check the source after the interrupt is detected.

3.2.9 Scratch register

This register (SCR: 5000_0020H (UART0), 5001_0020H (UART1), 5002_0020H (UART2)) can be used freely during programming.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Scratch Register							

Name	R/W	Bit	After Reset	Function
Reserved	R	15:8	0	Reserved. When these bits are read, 0 is returned for each bit.
Scratch Register	R/W	7:0	0	These bits do not affect the UART operation and can be used freely during programming.

3.2.10 Divisor latch LS byte register

This register (DLL: 5000_0024H (UART0), 5001_0024H (UART1), 5002_0024H (UART2)) specifies the lower 8 bits of the divisor for the baud rate generator. Set up this register in combination with the DLM register that specifies the higher 8 bits.

The baud rate generator divides the reference clock (XIN) and generates a 16x baud rate clock for the transmit and receive blocks by using the value specified in this register.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Divisor[7:0]							

Name	R/W	Bit	After Reset	Function
Reserved	R	15:8	0	Reserved. When these bits are read, 0 is returned for each bit.
Divisor[7:0] *	R/W	7:0	0	Specifies the lower 8 bits of the divisor.

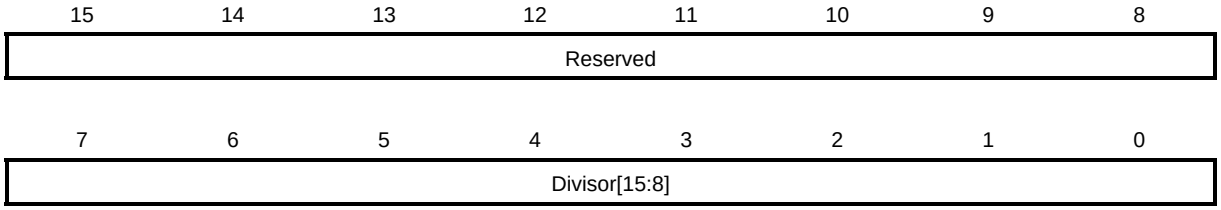
* If a register value is changed during operation, normal operation is not guaranteed. In this case, initialize the register.

Caution When the DLM and DLL registers are set up, bit 7 (DLAB) of the LCR register must be set to 1. The DLAB bit must be set to 0 after the DLM and DLL registers are written. For details, see 3.2.5 Line control register.

3.2.11 Divisor latch MS byte register

This register (DLM: 5000_0028H (UART0), 5001_0028H (UART1), 5002_0028H (UART2)) specifies the higher 8 bits of the divisor for the baud rate generator. Set up this register in combination with the DLL register that specifies the lower 8 bits.

The baud rate generator divides the reference clock (XIN) and generates a 16x baud rate clock for the transmit and receive blocks by using the value specified in this register.



Name	R/W	Bit	After Reset	Function
Reserved	R	15:8	0	Reserved. When these bits are read, 0 is returned for each bit.
Divisor[15:8] *	R/W	7:0	0	Specifies the higher 8 bits of the divisor.

* If a register value is changed during operation, normal operation is not guaranteed. In this case, initialize the register.

Caution When the DLM and DLL registers are set up, bit 7 (DLAB) of the LCR register must be set to 1. The DLAB bit must be set to 0 after the DLM and DLL registers are written. For details, see 3.2.5 Line control register.

3.2.12 Hardware control register

This additional register (HCR0: 5000_002CH (UART0), 5001_002CH (UART1), 5002_002CH (UART2)) controls the DMA controller and other hardware.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
SW Reset	RTS Mode	DMA 2Byte Access Enable	Receiver timeout DMA Disable	Receiver DMA Mode	Transmitter DMA Mode	Receiver DMA Enable	Transmitter DMA Enable

Name	R/W	Bit	After Reset	Function
Reserved	R	15:8	0	Reserved. When these bits are read, 0 is returned for each bit.
SW Reset	R/W	7	0	Setting this bit to 1 resets internal UART registers, except for registers for the transmit and receive FIFOs and baud rate generator (RBR/THR, DLL, and DLM). Setting this bit to 0 cancels the reset. **Caution Before executing a software reset, reset the transmit and receive FIFOs (bits 2 and 1 of FCR register). After that, registers other than the DLL and DLM registers must be set up again.**
RTS Mode	R/W	6	0	Selects the RTS mode when auto-RTS is used. 0: Auto-RTS mode 0 1: Auto-RTS mode 1
DMA 2Byte Access Enable	R/W	5	0	Selects the width of data to transfer to the transmit and receive FIFOs via DMA. 0: 1 byte 1: 2 bytes This setting affects the conditions for generating DMA request signals.
Receiver timeout DMA Disable	R/W	4	0	Specifies whether to include the timeout event in the reception DMA transfer request sources. 0: Includes the timeout event in the reception DMA transfer request sources. 1: Excludes the timeout event from the reception DMA transfer request sources (and automatically adds it to the interrupt sources).
Receiver DMA Mode	R/W	3	0	Specifies the DMA request mode separately for transmission and reception. These bits are used with bit 3 of the FCR register.
Transmitter DMA Mode	R/W	2	0	
Receiver DMA Enable	R/W	1	0	Specifies whether to enable the reception DMA request output. 0: Disables reception DMA requests. 1: Enables reception DMA requests.
Transmitter DMA Enable	R/W	0	0	Specifies whether to enable the transmission DMA request output. 0: Disables transmission DMA requests. 1: Enables transmission DMA requests.

3.2.13 Hardware status register 2

This additional register (HCR2: 5000_0030H (UART0), 5001_0030H (UART1), 5002_0030H (UART2)) is used to check the receive FIFO status.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Receiver FIFO Underrun	Receiver FIFO Data Count[6:0]						

Name	R/W	Bit	After Reset	Function
Reserved	R	15:8	0	Reserved. When these bits are read, 0 is returned for each bit.
Receiver FIFO Underrun	R	7	0	When data is read from the receive FIFO when it is empty or when reading of 2-byte data from the receive FIFO is attempted when only 1 byte is stored, an underrun error occurs and this bit is set to 1. Reading this register clears this bit to “0”. **Caution If an underrun error occurs, the receive FIFO is no longer read and all zeros are output to the host bus interface. No interrupt request is caused by an underrun error.**
Receiver FIFO Data Count[6:0]	R	6:0	0	Indicates the number of data items remaining in the receive FIFO.

3.2.14 Hardware status register 3

This additional register (HCR3: 5000_0034H (UART0), 5001_0034H (UART1), 5002_0034H (UART2)) is used to check the transmit FIFO status.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Transmitter FIFO Overrun	Transmitter FIFO Data Count[6:0]						

Name	R/W	Bit	After Reset	Function
Reserved	R	15:8	0	Reserved. When these bits are read, 0 is returned for each bit.
Transmitter FIFO Overrun	R	7	0	When data is written to the transmit FIFO when it is full or when 2-byte data is written to the transmit FIFO when only 1 free byte space is available, an overrun error occurs and this bit is set to 1. Reading this register clears this bit to “0”. **Caution If an overrun error occurs, the transmit FIFO is no longer written. No interrupt request is caused by an overrun error.**
Transmitter FIFO Data Count[6:0]	R	6:0	0	Indicates the number of data items remaining in the transmit FIFO.

3.3 IR Encoder/Decoder Registers

3.3.1 IR control register 0

This register (IRCR0: 5000_0040H (UART0), 5001_0040H (UART1), 5002_0040H (UART2)) controls the IrDA SIR (2.4 to 115.2 kbps) encoder/decoder.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved	IR_MASK_OFF	IR_RXPSEL	IR_RXEN	Reserved		IR_TXPSEL	IR_MODE

Name	R/W	Bit	After Reset	Function
Reserved	R	15:8	0	Reserved. When these bits are read, 0 is returned for each bit.
Reserved	R/W	7	0	Reserved. Written data is ignored.
IR_MASK_OFF	R/W	6	0	Specifies whether to enable masking of received data (stopping pulse detection) for echo cancellation. 0: Enables masking of received data. 1: Disables masking of received data.
IR_RXPSEL	R/W	5	0	Specifies the polarity of reception pulses. 0: Low 1: High
IR_RXEN	R/W	4	0	Specifies whether to enable reception. 0: Stops reception. 1: Enables reception
Reserved	R/W	3:2	0	Reserved. Written data is ignored.
IR_TXPSEL	R/W	1	0	Specifies the polarity of transmission pulses. 0: Low 1: High
IR_MODE	R/W	0	0	Specifies the operating mode. 0: UART mode 1: IR transmission/reception mode

3.3.2 IR control register 1

This register (IRCR1: 5000_0044H (UART0), 5001_0044H (UART1), 5002_0044H (UART2)) specifies the valid reception pulse width.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
PULSE_WIDTH[7:0]							

Name	R/W	Bit	After Reset	Function
Reserved	R	15:8	0	Reserved. When these bits are read, 0 is returned for each bit.
PULSE_WIDTH[7:0]	R/W	7:0	02H	Specifies the valid reception pulse width. Valid width: "Value set to this bit + 1" × 1 / f_{XIN} or longer Settable range: 02H to FFH (The settings 00H and 01H are prohibited.)

Cautions 1. The valid reception pulse width is expressed by using the following expression:

Valid reception pulse width (μs) ≥ (PULSE_WIDTH[7:0] + 1) × 1/f_{XIN} (MHz)

2. Valid reception pulses are detected by sampling reception pulses based on the XIN clock cycles. When the pulse level (specified by the IR_RXPSEL bit of the IRCR0 register) is successively detected the number of times specified for this register, the pulse is modulated as a valid pulse.

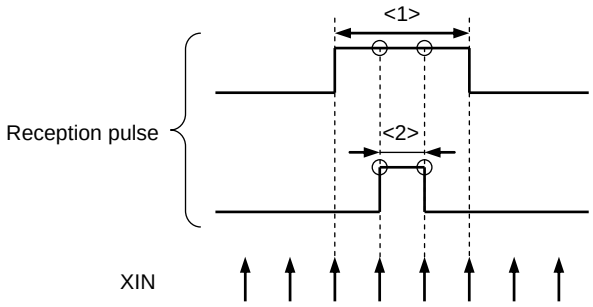
Depending on the phase of the reception pulse and XIN clock, a pulse that does not satisfy the above expression might be modulated as a valid pulse. The following shows the condition under which the reception pulse is always judged to be invalid:

Invalid reception pulse width (μs) < Approx. (PULSE_WIDTH[7:0] – 1) × 1/f_{XIN} (MHz)

Example When the PULSE_WIDTH field is set to 02H

<1> Valid reception pulse width (μs) ≥ 3 × 1/f_{XIN} (MHz)

<2> Invalid reception pulse width (μs) < 1 × 1/f_{XIN} (MHz)



3.3.3 IR control register 2

This register (IRCR2: 5000_0048H (UART0), 5001_0048H (UART1), 5002_0048H (UART2)) specifies the receive data mask period to add at the end of IR transmission.

The IRCR2, IRCR3, and IRCR4 register bits (MASK_PERIOD[19:0], 20 bits in total) are used for specification.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
MASK_PERIOD[7:0]							

Name	R/W	Bit	After Reset	Function
Reserved	R	15:8	0	Reserved. When these bits are read, 0 is returned for each bit.
MASK_PERIOD[7:0]	R/W	7:0	00H	Specifies the receive data mask period to add at the end of IR transmission. The lower 8 bits are specified.

3.3.4 IR control register 3

This register (IRCR3: 5000_004CH (UART0), 5001_004CH (UART1), 5002_004CH (UART2)) specifies the receive data mask period to add at the end of IR transmission.

The IRCR2, IRCR3, and IRCR4 register bits (MASK_PERIOD[19:0], 20 bits in total) are used for specification.

15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
MASK_PERIOD[15:8]							

Name	R/W	Bit	After Reset	Function
Reserved	R	15:8	0	Reserved. When these bits are read, 0 is returned for each bit.
MASK_PERIOD[15:8]	R/W	7:0	00H	Specifies the receive data mask period to add at the end of IR transmission. The middle 8 bits are specified.

3.3.5 IR control register 4

This register (IRCR4: 5000_0050H (UART0), 5001_0050H (UART1), 5002_0050H (UART2)) specifies the receive data mask period to add at the end of IR transmission.

The IRCR2, IRCR3, and IRCR4 register bits (MASK_PERIOD[19:0], 20 bits in total) are used for specification.

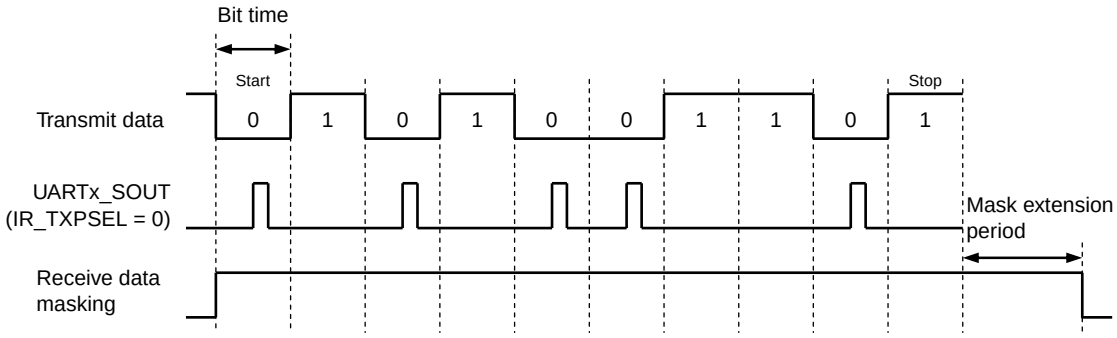
15	14	13	12	11	10	9	8
Reserved							

7	6	5	4	3	2	1	0
Reserved				MASK_PERIOD[19:16]			

Name	R/W	Bit	After Reset	Function
Reserved	R	15:4	0	Reserved. When these bits are read, 0 is returned for each bit.
MASK_PERIOD[19:16]	R/W	3:0	00H	Specifies the receive data mask period to add at the end of IR transmission. The higher 4 bits are specified.

Caution The mask extension period is expressed by using the following equation:

Mask extension period [μs) = (MASK_PERIOD[19:0] + 2) × 1/f_{XIN} (MHz)



CHAPTER 4 DESCRIPTION OF FUNCTIONS

4.1 Auto-Flow Mode

In auto-flow mode, the connected devices are also assumed to operate in auto-flow mode. If a connected device does not stop transmission by pulling RTSZ high, an overrun error occurs.

(1) HCR0 software reset

Almost all UART interface registers are initialized by setting bit 7 of the HCR0 register to 1, except for the FIFOs.

(2) Error detection when a FIFO is used

A parity error, framing error, and break interrupt are detected during reception and error information is concurrently stored in the FIFO with the data. Next, an interrupt is reported when data 1 byte or 2 bytes before the data that caused the error is read out. No break interrupt occurs when no start bit is detected (such as during frame data reception). However, the break interrupt can be detected in the non-FIFO mode. If the above errors are detected while a FIFO is used, the receive FIFO must be reset by using bit 1 of the FCR register to clear error information in the FIFO.

(3) Interrupt signal (INTRPT)

After the INTRPT signal related to data transfer is pulled high, it stays at high level until the interrupt source is cleared. However, the transmit buffer empty interrupt is masked by reading the IIR register. The mask is disabled by writing data to transmit. After the transmit buffer empty interrupt is masked, it does not occur even if the transmit buffer is empty, as long as data to transmit is not written.

(4) Serial clock generation

A serial clock is masked after a reset. The mask is disabled by setting up the baud rate registers (DLL and DLM) and then setting bit 7 (DLAB) of the LCR register to 0. Because the mask is disabled at the falling edge of the output of the DLAB bit setting, disabling the mask is valid only once after a reset. The masking can be specified only when hardware is reset.

(5) Auto-flow mode is disabled when bit 3 of the IER register is set to 1

When the modem status interrupt is enabled,
auto-CTS : disabled
auto-RTS : enabled
To enable auto-flow mode, the modem status interrupt must therefore be disabled.

4.2 FIFOs

4.2.1 Operation in FIFO interrupt mode

The following interrupts occur while the receive FIFO interrupt is enabled (when bit 0 of the FCR register, bit 0 of the IER register, and bit 2 of the IER register are set to 1).

- When the amount of data in the receive FIFO reaches the trigger level, a receive data enable interrupt is issued. When the amount of data in the receive FIFO becomes less than the trigger level, the interrupt is cleared.
- The received data available interrupt is indicated in the IIR register when the receive FIFO reaches the trigger level.
- A receiver line status interrupt (IIR = 06H) has a higher priority than the received data available interrupt (IIR = 04H).
- When a character is transmitted to the receive FIFO from the receive shift register (RSR), bit 0 (DR) of the LSR register is set to 1. When the receive FIFO empties, the DR bit is cleared.

4.2.2 Operation in FIFO polled mode

When the FIFO is enabled (bit 0 of the FCR register = 1), bits 3 to 0 of the IER register are set to 0 in FIFO polled mode. Transmission and reception can then be set to FIFO polled mod separately.

In this mode, the user program checks the transmission and reception status by using the LSR register.

The immediately preceding statuses are:

Bit 0 of the LSR register is set to 1 when at least 1 byte is stored in the receive FIFO.

Bits 4 to 1 of the LSR register indicate details about the error occurrence.

Bit 5 of the LSR register indicates that the THR is empty.

Bit 6 of the LSR register indicates that both THR and TSR are empty.

Bit 7 of the LSR register indicates whether the receive FIFO contains some errors.

4.2.3 Read when the receive FIFO is empty

If the receive FIFO is read while it is empty, the read counter is not incremented.

In this case, a receive FIFO underrun error is detected (bit 7 of HCR2 register).

4.3 Interrupt Sources

The UART interface uses four interrupts.

Table 4-1. Interrupt Sources

Interrupt Name	Bit Assignment
Modem status interrupt	Bit 3 (EDSSI) of the IER register
Reception error (receiver line status) interrupt	Bit 2 (ELSI) of the IER register
Transmit buffer empty (transmit hold register (THR) empty) interrupt	Bit 1 (ETBEI) of the IER register
Reception error (received data available)/timeout interrupt	Bit 0 (ERBI) of the IER register

4.4 Clock and Reset

The following clock is used for the UART interface:

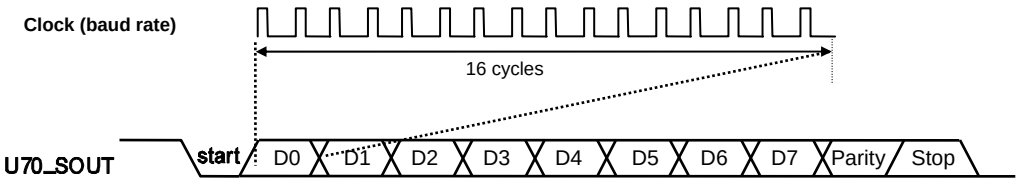
- U70_SCLK

  Used for accessing the APB bus.

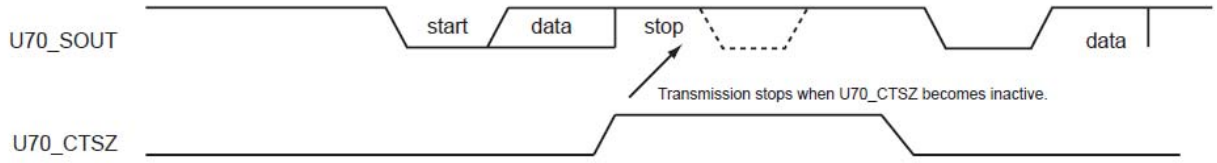
  For details about clock/reset settings, see the **Multimedia Processor for Mobile Applications - System Control/General-Purpose I/O Interface User's Manual (S19265E)**.

4.5 I/O Timing

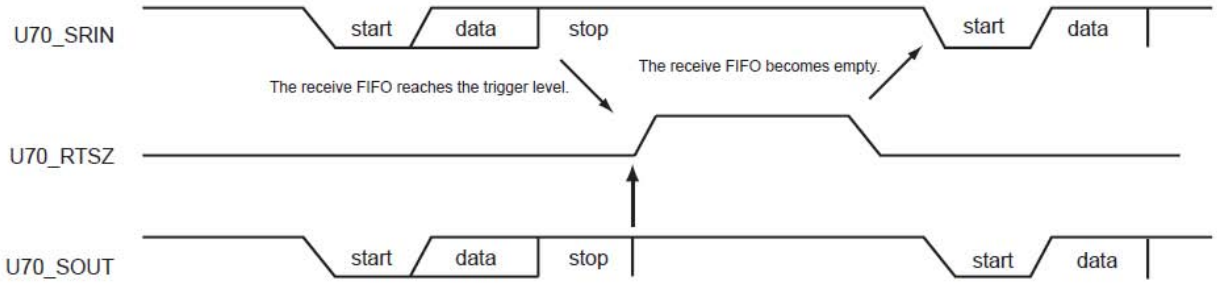
4.5.1 Serial data



4.5.2 Timing of auto-flow CTS control



4.5.3 Timing of auto-flow RTS control

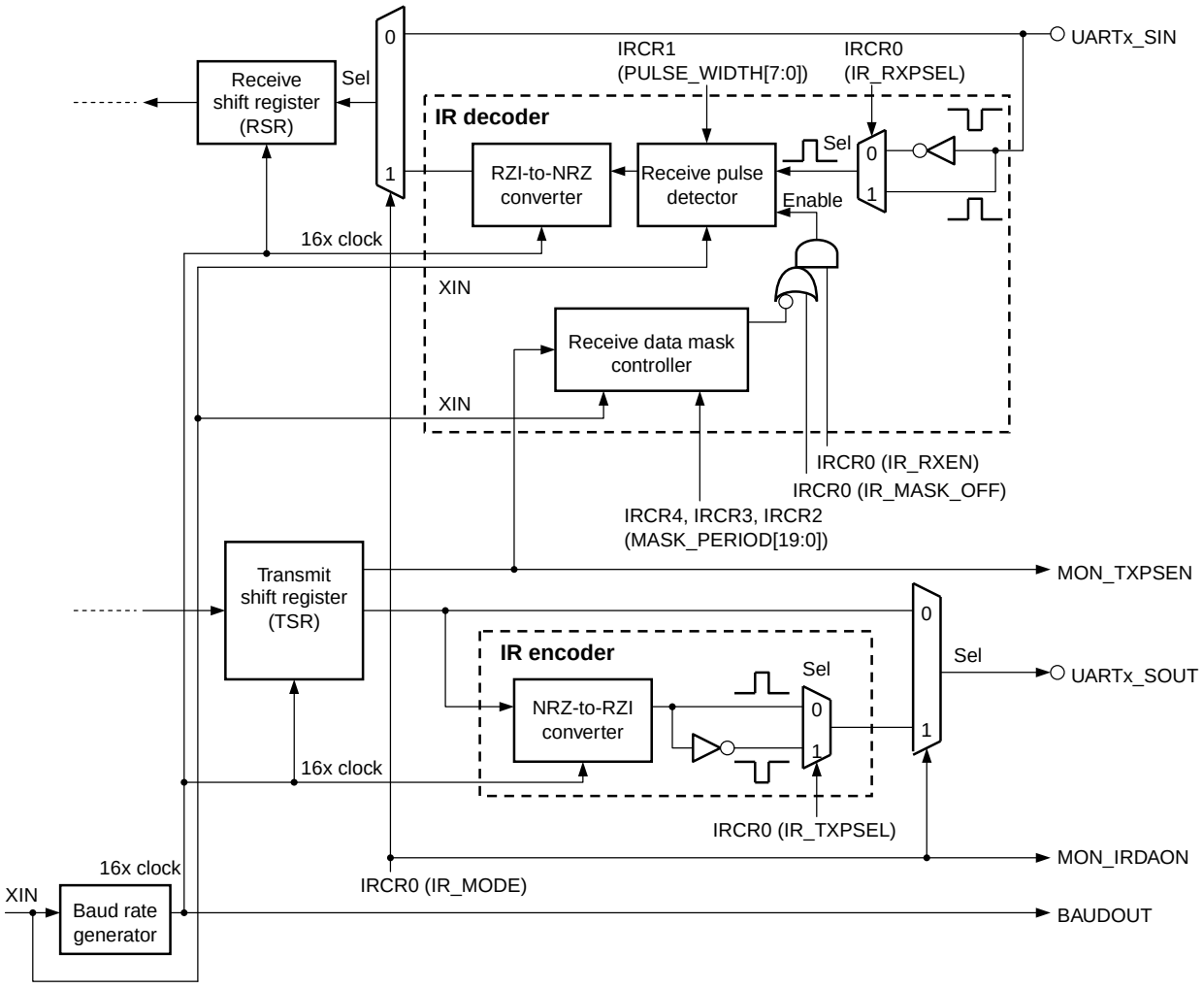


4.6 IR Encoder/Decoder Functions

EM1 incorporates an IrDA SIR (2.4 to 115.2 kbps) encoder/decoder (IR encoder/decoder). Figure 4-1 shows a block diagram of the IR encoder/decoder.

The IR transmission/reception mode is entered when bit 0 (IR_MODE) of the IRCR0 register is set to 1. (The IR encoder/decoder is inserted into the data path used for transmission and reception via the UARTx_SIN and UARTx_SOUT pins.)

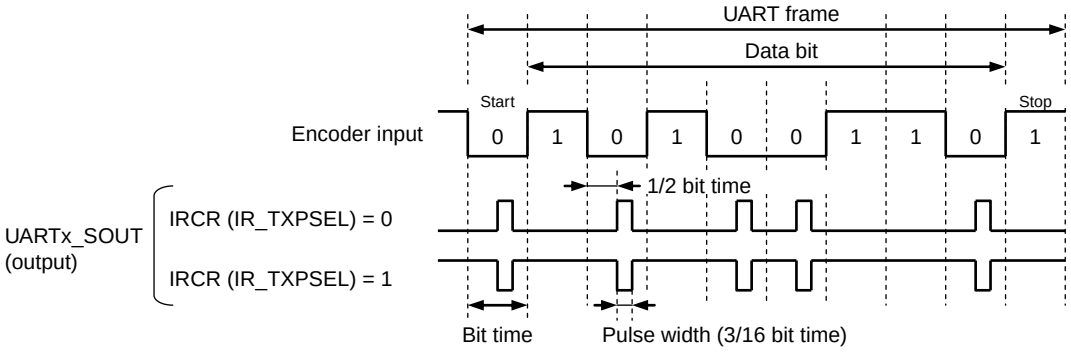
Figure 4-1. IR Encoder/Decoder Block Diagram



4.6.1 Transmission data modulation by IR encoder

When the transmitted data value is 0, a pulse with the width of the baud rate cycle multiplied by 3/16 is output. The polarity of transmission pulses can be selected by using bit 1 (IR_TXPSEL) of the IRCR0 register.

Figure 4-2. Transmission Data Modulation Example



4.6.2 Reception data demodulation by IR decoder

The IR decoder outputs 0 if the input pulse width is valid (value set to the PULSE_WIDTH[7:0] bits of IRCR1 register) or longer; otherwise it outputs 1. The polarity of reception pulses can be selected by using bit 5 (IR_RXPSEL) of the IRCR0 register.

Figure 4-3. Reception Data Demodulation Example

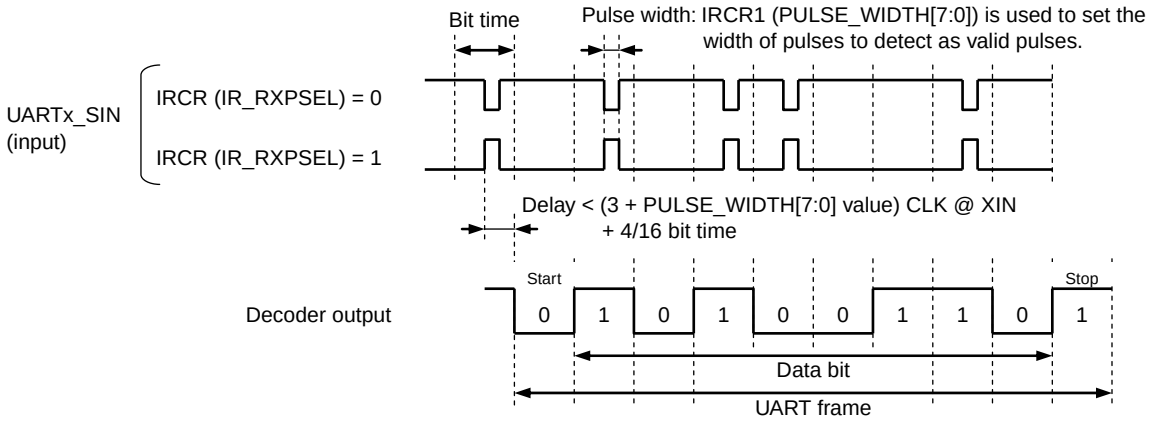


Table 4-2 lists examples of valid pulse width settings (PULSE_WIDTH[7:0] of the IRCR1 register). In this table, the values of PULSE_WIDTH[7:0] are expressed in decimal notation. This table only presents some examples of the desired valid reception pulse width and XIN clock frequency values. Change the values according to the user system.

Table 4-2. PULSE_WIDTH[7:0] Setting Examples

Desired Valid Reception Pulse Width (μs)	f_{XIN} = 1.8432 MHz		f_{XIN} = 3.072 MHz		f_{XIN} = 14.7456 MHz		f_{XIN} = 50 MHz	
	PULSE_ WIDTH[7:0]	Measured Valid Reception Pulse Width (μs)	PULSE_ WIDTH[7:0]	Measured Valid Reception Pulse Width (μs)	PULSE_ WIDTH[7:0]	Measured Valid Reception Pulse Width (μs)	PULSE_ WIDTH[7:0]	Measured Valid Reception Pulse Width (μs)
1.0	_Note	_Note	2	0.98	13	0.95	49	1.0
1.41	_Note	_Note	3	1.30	19	1.36	69	1.41
2.0	2	1.63	5	1.95	28	1.97	99	2.0
3.0	4	2.71	8	2.93	43	2.98	149	3.0

Note The desired pulse width cannot be detected because the XIN clock frequency is low.
The lower limit of the XIN clock frequency for the desired valid reception pulse width is obtained using the following expression, by assigning the PULSE_WIDTH[7:0] value (= 2, the minimum setting) to the valid reception pulse width expression.

f_{XIN} (MHz) $\geq$ 1 /(desired valid reception pulse width (μs) / 3)

Remark f_{XIN}: Frequency of reference clock (XIN)

4.6.3 Masking of reception data for IR decoder echo cancellation

The IR decoder can mask reception data (stop pulse detection) during transmission for echo cancellation. The mask period can be extended for the transmission period plus the period specified by the IRCR2 to IRCR4 registers (MASK_PERIOD[19:0]). Whether to enable masking of the reception data can be specified by using bit 6 (IR_MASK_OFF) of the IRCR0 register.

Table 4-3. MASK_PERIOD[19:0] Setting Examples

Desired Mask Extension Period (μs)	f_{XIN} = 1.8432 MHz		f_{XIN} = 3.072 MHz		f_{XIN} = 14.7456 MHz		f_{XIN} = 50 MHz	
	MASK_ PERIOD [19:0]	Measured Mask Extension Period (μs)	MASK_ PERIOD [19:0]	Measured Mask Extension Period (μs)	MASK_ PERIOD [19:0]	Measured Mask Extension Period (μs)	MASK_ PERIOD [19:0]	Measured Mask Extension Period (μs)
50	91	50.46	152	50.13	736	50.05	2,498	50
100	183	100.37	306	100.26	1,473	100.03	4,998	100
1,000	1,842	1000.43	3,070	1,000	14,744	1,000.03	49,998	1,000
5,000	9,214	5,000	15,358	5,000	73,726	5,000	249,998	5,000
10,000	18,430	10,000	30,718	10,000	147,454	10,000	499,998	10,000

4.6.4 Cautions on using IR encoder/decoder

(1) Cautions on changing the IR control register settings

Be sure to set bit 4 (IR_RXEN) of the IRCR0 register to 0 (to stop reception) before changing the register settings that specify the reception by the IR decoder. If this bit is not set to 0, invalid data might be received due to a sudden signal variation.

The following registers are affected:

Bit 6 (IR_MASK_OFF) and bit 5 (IR_RXPSEL) of IRCR0 register

IRCR1 to IRCR4 registers

(2) Restriction on the XIN clock frequency minimum

The IR decoder uses the XIN clock to sample reception pulses. Therefore, the minimum valid reception pulse width depends on the XIN clock frequency.

(3) Supported IrDA specifications

The interface protocol prescribed by IrDA concerns the infrared (IR) interface, and the electrical interface (<1> and <2> in Figure 4-4) is not prescribed. When using the IR encoder/decoder, thoroughly evaluate the connectivity with the connected devices (such as IR transceivers).

Figure 4-4. IrPHY Ver. 1.4 Block Configuration Example

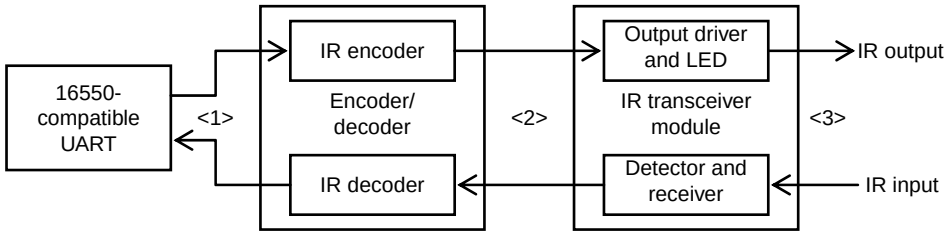


Table 4-4. IrPHY Ver. 1.4 SIR Ratings Related to Data Transfer Speed and Pulse Width

Transfer Speed (kbps)	Modulation Mode	Allowable Transfer Speed Error (% of Rate)	Minimum Pulse Width (μs)	Pulse Width x3/16 Nominal Value (μs)	Maximum Pulse Width (μs)
2.4	RZI	± 0.87	1.41	78.13	88.55
9.6	RZI	± 0.87	1.41	19.53	22.13
19.2	RZI	± 0.87	1.41	9.77	11.07
38.4	RZI	± 0.87	1.41	4.88	5.96
57.6	RZI	± 0.87	1.41	3.26	4.34
115.2	RZI	± 0.87	1.41	1.63	2.23

Remark The pulse widths are defined for the IR output (<3> in Figure 4-4).

CHAPTER 5 USAGE

5.1 Initialization Method

5.1.1 Initialization

This section describes initial settings necessary for operating the UART interface.

(1) Baud rate settings and enabling 64-byte FIFO mode

Set bit 7 (DLAB) of the LCR register to 1 and specify a baud rate in the DLM and DLL registers.
After the above settings, LCR [7] is to set it in = 0, and generation of 16x clock is begun.

(2) FIFO mode settings

Specify whether to enable FIFO by using bit 0 of the FCR register.
Select a DMA mode by using bit 3 of the FCR register.
Select the 16- or 64-byte FIFO mode by using bit 5 of the FCR register.
Select the trigger level of the receive FIFO by using bits 7 and 6 of the FCR register. (This setting is not required for the non-FIFO mode.)

(3) Serial interface settings

Specify the length of frame data in bits by using bits 1 and 0 (WLS) of the LCR register.
Specify the number of stop bits by using bit 2 of the LCR register.
Select no parity, even parity, odd parity, or stick parity by using bits 5 to 3 of the LCR register.

(4) Modem interface settings

Set up flow control by using bits 5 and 1 of the MCR register.
When auto-flow control is not used, set bit 1 of the MCR register to 1 to assert the RTSZ output.
Next, set up the IER and HCR0 registers to enable the interrupt and DMA functions.

- Set bits 3 and 2 of the IER register to 1
  Enable the receiver line interrupt.
  Enable the modem status interrupt. (Read the MSR register before enabling this interrupt or the interrupt might be issued immediately.)

- When data is transferred with an interrupt
  Bit 6 of HCR0 = 0 or 1 Set the auto-RTS mode.
  Bits 1 and 0 of IER = 1 Enable the transmit buffer empty interrupt and received data available interrupt.

- When data is transferred by DMA
  Bit 6 of HCR0 = 0 or 1 Set the auto-RTS mode.
  Bits 5 to 2 of HCR0 Specify the settings for the DMA mode.
  Bits 1 and 0 of HCR0 = 1 Enable the transmission/reception DMA request.

5.2 Baud Rate Setting

A baud rate is determined according to the settings for serial clock input and the DLM and DLL registers. EM1 assumes that the serial clocks below are input.

Clock frequencies can be set individually. For details about clock settings, see the **Multimedia Processor for Mobile Applications - System Control/General-Purpose I/O Interface User's Manual (S19265E)**.

Clock Frequency	[Hz]	Clock Source	Baud Rate (bps)	Error Range	DLMR	DLLR	Actual Baud Rate (bps)	Error (%)
229.376	M	PLL3	2400	±4	23	85	2400.13394	0.0055807
			4800		11	171	4799.46435	–0.011159
			9600		5	213	9602.14334	0.0223264
			19200		2	235	19191.4324	–0.044623
			38400		1	117	38434.3164	0.0893655
			57600		0	249	57574.2972	–0.044623
			115200		0	124	115612.903	0.3584229

Clock Frequency	[Hz]	Clock Source	Baud Rate (bps)	Error Range	DLMR	DLLR	Actual Baud Rate (bps)	Error (%)
7.168	M	PLL3/32	2400	±4	0	187	2395.72193	–0.178253
			4800		0	93	4817.2043	0.3584229
			9600		0	47	9531.91489	–0.70922
			19200		0	23	19478.2609	1.4492754
			38400		0	12	37333.3333	–2.777778
			57600		0	8	56000	–2.777778
			115200		0	4	112000	–2.777778

5.3 Notes on Use of FIFOs

UART and the internal bus communicate via a 2-byte interface, so the FIFOs can be read or written at the same time in 2-byte units, but note the following:

(1) An overrun error occurs when 2-byte data is written in response to a DMA request when only 1 byte of space is available in the transmit FIFO in the DMA mode 1.

(2) When a reception timeout event occurs in DMA mode 1 while the timeout interrupt is enabled (bit 4 of the IER register = 0), the host cannot determine whether the request is issued due to a timeout event or the trigger level. As a result, if 2 bytes are read in response to a DMA request, a FIFO underrun error occurs.

Revision History

Date	Revision	Comments
February 10, 2009	1.0	–
April 27, 2009	2.0	Incremental update from comments to the 1.0..
September 30, 2009	3.0	Incremental update from comments to the 2.0..

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