Mobile Multimedia Processor Technical Information

EMMA Mobile ™ 1 (MC-10118A、μPD77630A) Usage Restrictions		Document No.	IMB – YB2 – 000585	1/13
		Date issued	Oct 23rd. ,2009	
		Issued by	Mobile Platform Group SoC Systems Division 2nd SoC Operations Unit NEC Electronics Corporation	
Related documents	User's Manual : S19598E, S19687E Data Sheet : S19657E, S19686E	Notification classification	✓	Usage restriction
				Upgrade
				Document modification
				Other notification

1. Affected products

   MC-10118A, μPD77630A

2. New restrictions

[Restriction 5] DDR-SDRAM memory can be used with uPD77630A (only for uPD77630A)

[Description]

Please use DDR-SDRAM, whose AC spec tXSR (Exit self refresh to first valid command) smaller than 132ns.

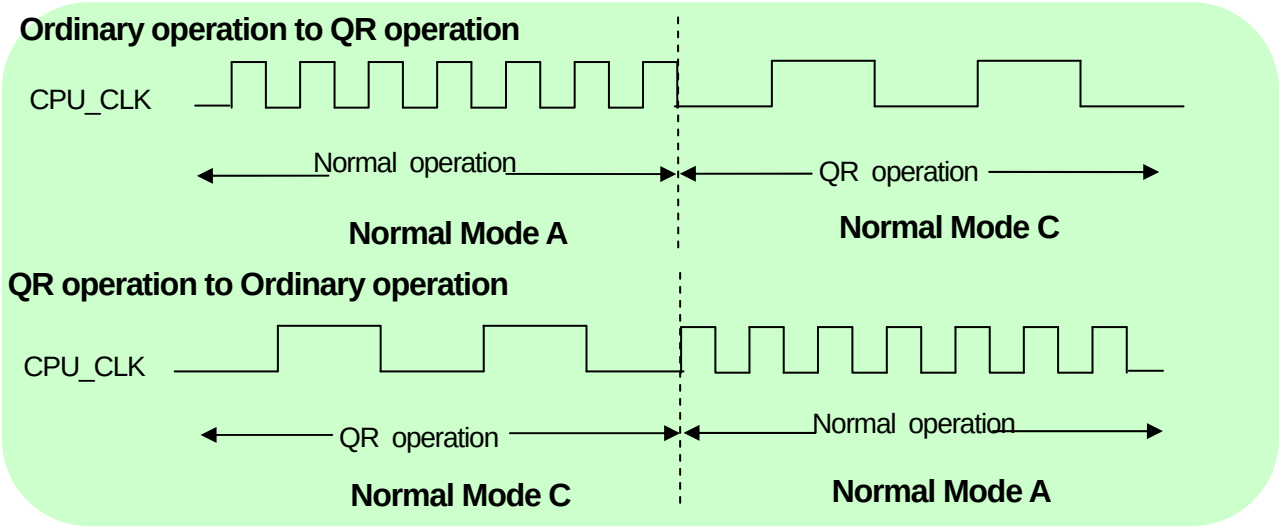
The products NEC Electronics checked on the data sheet are shown below

Vendor	Product name	tXSR(ns)
Hynix	512Mb_(16Mx32bit) Mobile DDR SDRAM H5MS5122DKA(J3M)	120（min）
Samsung	32Mx32 Mobile DDR SDRAM K4X1G323PE - 8GD6(8)	120（min）
	32Mx32 Mobile DDR SDRAM K4X1G323PC - L(F)E/G	120（min）
ELPIDA	1G bits DDR Mobile RAM EDD10323BBH-LS (32M words × 32 bits)	120（min）
	512M bits DDR Mobile RAM EDD51323DBH-LS (16M words × 32 bits)	120（min）

[Restriction 6] Clock setting at QR (Quick Recovery) operation of ACPU

[Description]

Using QR (Quick Recovery) operation, the division setting of ACPU clock is just the same as HBUS clock just before entering QR operation. To change the division setting, please use mode transition of Normal Mode A,B,C,D(see P.221 of EMMA Mobile 1 User's Manual System Control/General-Purpose I/O Interface). The example below shows Normal Mode A for normal operation and Normal Mode C for QR operation.



[Restriction 7] Write buffer control in the L2 Cache Controller of ACPU

[Description]

There is the write buffer (256bit x 2slot) in the L2 Cache controller of ACPU. Before cutting off the power switch of ACPU, please drain the data in the write buffer to DRAM (call this operation as Write Buffer Drain). Sample program for restriction 6 & 7 is shown below.

```
ENTRY(cpu_v6_do_idle)
        ldr     r2, =IO_ADDRESS(MP200_SMU_BASE)
        ldr     r0, =0x00244202         @ modify CPU div rate
        str     r0, [r2, #0xf8]
        ldr     r3, [r2, #0x80]         @ backup current div slot
        mov     r0, #3                  @ change with Normal-C slot
        str     r0, [r2, #0x80]
2:      ldr     r0, [r2, #0x80]
        lsr     r0, #8
        cmp     r0, #3
        bne     2b

        ldr     r2, =IO_ADDRESS(MP200_L220_BASE)
        ldr     r0, =1f
        mcr     p15, 0, r0, c7, c13, 1  @ prefetch I cache
        ldr     r0, =3f
        mcr     p15, 0, r0, c7, c13, 1  @ prefetch I cache

        mov     r0, #0
        mcr     p15, 0, r0, c7, c10, 4  @ drain write buffer

        mov     r0, #0x1
        str     r0, [r2, #0x730]        @ L2 Sync
L2_sync_loop:
        ldr     r0, [r2, #0x730]
        cmp     r0, #0
        bne     L2_sync_loop

1:      mcr     p15, 0, r1, c7, c0, 4   @ wait for interrupt

        b       2f
2:      ldr     r2, =IO_ADDRESS(MP200_SMU_BASE)
        str     r3, [r2, #0x80]         @ restore CPU div rate
        mov     pc, lr
3:
```

WFI

No.6

Transition from normal operation (Normal A) to QR operation (Normal C). The division setting of ACPU clock is just the same as that of HBUS clock. Before executing this, the interrupts should be disable.

No.7

Prefetch the I-Cache to avoid fetching I-Cache data after Write Buffer Drain Operation and then execute Write Buffer Drain.

No.6

After recovering from WFI, transition from QR operation (Normal C) to normal operation (Normal A).

[Restriction 8] Power switch (L1, L2, L3) control

[Description]

Power switch of the power domain L1, L2 and L3 should be controlled by setting the registers of each power switch and burrier gate control respectively.

- L1&L2 should be controlled by PMU. Please implement the sequence below.
- L3 should be controlled by ACPU. Please implement the sequence below.

【L1 Power Off】

Execute below sequence on PMU

PMU code	PMU command	Macro Select	Register name	Write Data	Count	
0x000A0268, 0x00000000,	REG_WRITE	ASMU	L1_BUZ	0x00000000		L1 burrier gate valid
0x000A026C, 0x00000000,	REG_WRITE	ASMU	L1_BUZ2	0x00000000		↑
0x000A0244, 0x00000F0F,	REG_WRITE	ASMU	L1_POWERSW	0x00000F0F		All of the L1 power switch OFF

【L1 Power On】

Execute below sequence on PMU

PMU code	PMU command	Macro Select	Register name	Write Data	Count	
0x000A0244, 0x00000F07,	REG_WRITE	ASMU	L1_POWERSW	0x00000F07		One of the L1 power switch ON
0x4C000050,	CYCLE_WAIT				0x50	Wait
0x000A0244, 0x00000F03,	REG_WRITE	ASMU	L1_POWERSW	0x00000F03		↑
0x4C000050,	CYCLE_WAIT				0x50	↑
0x000A0244, 0x00000F01,	REG_WRITE	ASMU	L1_POWERSW	0x00000F01		↑
0x4C000050,	CYCLE_WAIT				0x50	↑
0x000A0244, 0x00000F00,	REG_WRITE	ASMU	L1_POWERSW	0x00000F00		↑
0x4C000050,	CYCLE_WAIT				0x50	↑
0x000A0244, 0x00000700,	REG_WRITE	ASMU	L1_POWERSW	0x00000700		↑
0x4C000050,	CYCLE_WAIT				0x50	↑
0x000A0244, 0x00000300,	REG_WRITE	ASMU	L1_POWERSW	0x00000300		↑
0x4C000050,	CYCLE_WAIT				0x50	↑
0x000A0244, 0x00000100,	REG_WRITE	ASMU	L1_POWERSW	0x00000100		↑
0x4C000050,	CYCLE_WAIT				0x50	↑
0x000A0244, 0x00000000,	REG_WRITE	ASMU	L1_POWERSW	0x00000000		↑(All of the L1 power switch ON)
0x4C000050,	CYCLE_WAIT				0x50	↑
0x000A0208, 0x01000000,	REG_WRITE	ASMU	ASMU_BGCTRL	0x01000000		L1 burrier gate invalid
0x000A0268, 0x00001111,	REG_WRITE	ASMU	L1_BUZ	0x00001111		↑
0x000A026C, 0x00000011,	REG_WRITE	ASMU	L1_BUZ2	0x00000011		↑
0x000A0208, 0x00000000,	REG_WRITE	ASMU	ASMU_BGCTRL	0x00000000		↑

【L2 Power Off】

Execute below sequence on PMU

PMU code	PMU command	MacroSelect	Register name	Write Data	Count	
0x000A0500, 0x00000000,	REG_WRITE	ASMU	L2_POWERSW	0x00000000		L2 burrier gate valid
0x000A0500, 0x000000FF,	REG_WRITE	ASMU	L2_POWERSW	0x000000FF		All of the L2 power switch ON

【L2 Power On】

Execute below sequence on PMU

PMU code	PMU command	MacroSelect	Register name	Write Data	Count	
0x000A0500, 0x0000007F,	REG_WRITE	ASMU	L2_POWERSW	0x0000007F		One of the L2 power switch ON
0x4C000010,	CYCLE_WAIT				0x10	Wait
0x000A0500, 0x0000003F,	REG_WRITE	ASMU	L2_POWERSW	0x0000003F		↑
0x4C000010,	CYCLE_WAIT				0x10	↑
0x000A0500, 0x0000001F,	REG_WRITE	ASMU	L2_POWERSW	0x0000001F		↑
0x4C000010,	CYCLE_WAIT				0x10	↑
0x000A0500, 0x0000000F,	REG_WRITE	ASMU	L2_POWERSW	0x0000000F		↑
0x4C000010,	CYCLE_WAIT				0x10	↑
0x000A0500, 0x00000007,	REG_WRITE	ASMU	L2_POWERSW	0x00000007		↑
0x4C000010,	CYCLE_WAIT				0x10	↑
0x000A0500, 0x00000003,	REG_WRITE	ASMU	L2_POWERSW	0x00000003		↑
0x4C000010,	CYCLE_WAIT				0x10	↑
0x000A0500, 0x00000001,	REG_WRITE	ASMU	L2_POWERSW	0x00000001		↑
0x4C000010,	CYCLE_WAIT				0x10	↑
0x000A0500, 0x00000000,	REG_WRITE	ASMU	L2_POWERSW	0x00000000		↑(All of the L2 power switch ON)
0x4C000010,	CYCLE_WAIT				0x10	↑
0x000A0500, 0x00010100,	REG_WRITE	ASMU	L2_POWERSW	0x00010100		L2 burrier gate invalid

【L3 Power Off】

Execute below sequence on ACPU

Register Name	Write Data	
ASMU_L3_POWERSW_BUZ	0x00000000	L3 burrier Valid
ASMU_L3_POWERSW_BUZ	0x000000FF	All of L3 power switch Off

【L3 Power On】

Execute below sequence on ACPU

Register Name	Write Data	
ASMU_L3_POWERSW_BUZ	0x0000007F	One of L3 power Switch On
ASMU_L3_POWERSW_BUZ	0x0000003F	↑
ASMU_L3_POWERSW_BUZ	0x0000001F	↑
ASMU_L3_POWERSW_BUZ	0x0000000F	↑
ASMU_L3_POWERSW_BUZ	0x00000007	↑
ASMU_L3_POWERSW_BUZ	0x00000003	↑
ASMU_L3_POWERSW_BUZ	0x00000001	↑
ASMU_L3_POWERSW_BUZ	0x00000000	↑
ASMU_L3_POWERSW_BUZ	0x00010100	L3 burrier gate invalid

[Restriction 9] USB D- pin pull-down control

[Description]

USB D- pin in EM1 is always pull-down with 15kohm when device mode is used. To use USB without D- pin pull-down, after Initializing, please RUN(=USBCMD register, bit0(R/S)=1), then set the value=0x600e0001 to USBViewport register.

3. List of restrictions

See Appendix

4. History

EMMA Mobile1 restrictions documents

Document number	Issue date	Note
IMB-YB2-000509	July 3rd. 2009	1st. edition

<Appendix: List of restrictions>

1. Detail of restrictions

No.	Item	Outline	MC-10118A	uPD77630A
1	AXI bus	After a bus master of AXI(except ACPU) bus reads SRC, the bus master can not read other slave.	✓	✓
2	GPIO	The FIQ interrupts of GPIO[96:117] do not work.	✓	✓
3	DTV	After stopping DMA transfer to DTV module, DTV module continues to send transfer request to AHB bus under the specific conditions.	✓	✓
4	NTSC	Indication of 1st FIELD (even field) and 2nd FIELD (odd field) reverses NTSC output.	✓	✓
5	DRAM	The AC spec(TXSR: Exit self refresh to first valid command) of DDR-SDRAM restriction		✓
6	ACPU	Clock setting at QR(Quick Recovery) operation of ACPU	✓	✓
7	ACPU	Write buffer control in the L2 Cache Controller	✓	✓
8	Power SW	Power switch(L1,L2,L3) control	✓	✓
9	USB	D- pin pull-down control	✓	✓

[Restriction 1] AXI bus

[Description]

When a bus master of AXI (except ACPU) bus reads SRC (ISRAM 128KB), the bus master can not read other slave after read access to SRC..

[Conditions]

- The bus master can read SRC continuously..
- Bus masters can read/write other slaves except SRC.
- ACPU (one of the bus master) can read/write SRC without problem.
- Bus masters can write slaves including SRC..

[Workaround]

- Bus masters which access to SDRAM (one of bus slaves) shall not read SRC .
- Bus master (PDMA) which access to SRC shall not read SDRAM.

[Restriction 2] FIQ interruption of GPIO

[Description]

The FIQ interrupts of GPIO[96:117] do not work.

GPIO[96:117] can be used as IRQ interrupt.

[Workaround]

Use GPIO[0-95] as FIQ interrupt.

[Restriction 3] DMA transmission of DTV

[Description]

After stopping DMA transfer to DTV module, DTV module continues to send transfer request to AHB bus under the specific conditions.

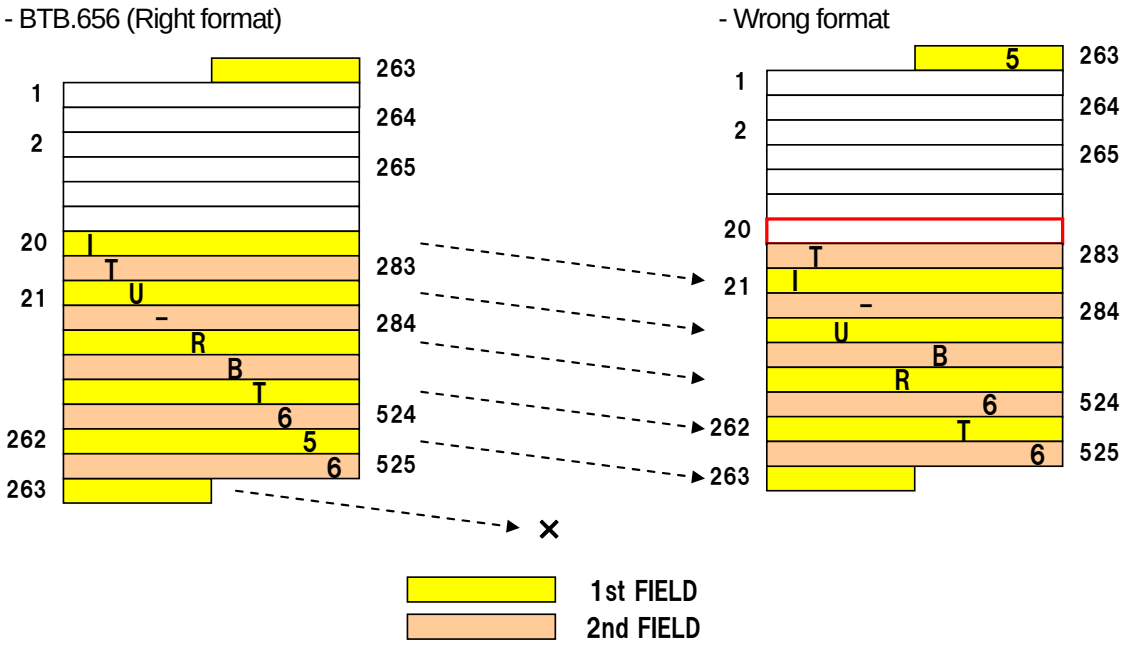
[Workaround]

When DTV module user wants to stop DMA transfer to DTV module, use HW_RSTZ of DT_MODULECONT register (4015_0040H) instead of using DTVSTOP of_DT_STATUS register (4015_0000H).
After stopping DMA transfer, reset (HW reset) DTV module if DTVSTOPRAW of DT_RAWSTATUS register (4015_0004H) is 1 and DMAREQ of DT_DMAREQ register (4015_0024H) is 1. (This workaround is supported in NEC EL device driver for Linux)

[Restriction 4] Indication abnormality of NTSC output

[Description]

Indication of 1st FIELD (even field) and 2nd FIELD (odd field) reverses NTSC output.



[Workaround]

1stFIELD (even field) and 2ndFIELD (odd field) are exchanged by software (This workaround is supported in NEC EL device driver for Linux).

[Restriction 5] DDR-SDRAM memory can be used with uPD77630A (only for uPD77630A)

[Description]

Please use DDR-SDRAM, whose AC spec tXSR (Exit self refresh to first valid command) smaller than 132ns.

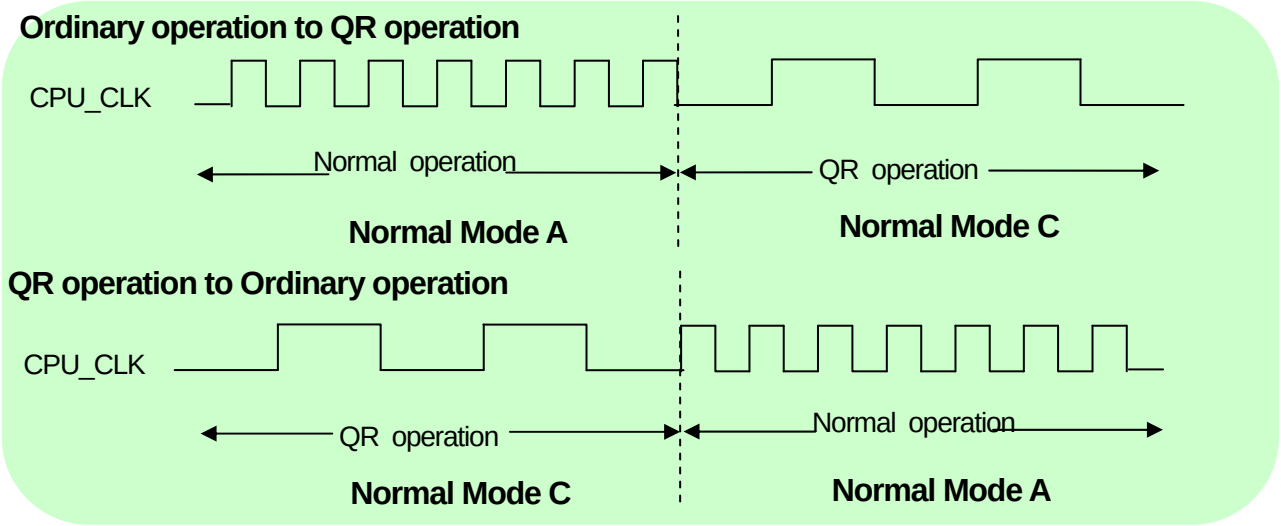
The products NEC Electronics checked on the data sheet are shown below

Vendor	Product name	tXSR(ns)
Hynix	512Mb_(16Mx32bit) Mobile DDR SDRAM H5MS5122DKA(J3M)	120（min）
Samsung	32Mx32 Mobile DDR SDRAM K4X1G323PE - 8GD6(8)	120（min）
	32Mx32 Mobile DDR SDRAM K4X1G323PC - L(F)E/G	120（min）
ELPIDA	1G bits DDR Mobile RAM EDD10323BBH-LS (32M words × 32 bits)	120（min）
	512M bits DDR Mobile RAM EDD51323DBH-LS (16M words × 32 bits)	120（min）

[Restriction 6] Clock setting at QR(Quick Recovery) operation of ACPU

[Description]

Using QR(Quick Recovery) operation, the division setting of ACPU clock is just the same as HBUS clock just before entering QR operation. To change the division setting, please use mode transition of Normal Mode A,B,C,D(see P.221 of EMMA Mobile 1 User's Manual System Control/General-Purpose I/O Interface). The example below shows Normal Mode A for normal operation and Normal Mode C for QR operation.



[Restriction 7] Write buffer control in the L2 Cache Controller of ACPU

[Description]

There is the write buffer(256bit x 2slot) in the L2 Cache controller of ACPU. Before cutting off the power switch of ACPU, please drain the data in the write buffer to DRAM(call this operation as Write Buffer Drain). Sample program for restriction 6 & 7 is shown below.

```
ENTRY(cpu_v6_do_idle)
        ldr     r2, =IO_ADDRESS(MP200_SMU_BASE)
        ldr     r0, =0x00244202         @ modify CPU div rate
        str     r0, [r2, #0xf8]
        ldr     r3, [r2, #0x80]         @ backup current div slot
        mov     r0, #3                  @ change with Normal-C slot
        str     r0, [r2, #0x80]
2:      ldr     r0, [r2, #0x80]
        lsr     r0, #8
        cmp     r0, #3
        bne     2b

        ldr     r2, =IO_ADDRESS(MP200_L220_BASE)
        ldr     r0, =1f
        mcr     p15, 0, r0, c7, c13, 1  @ prefetch I cache
        ldr     r0, =3f
        mcr     p15, 0, r0, c7, c13, 1  @ prefetch I cache

        mov     r0, #0
        mcr     p15, 0, r0, c7, c10, 4  @ drain write buffer

        mov     r0, #0x1
        str     r0, [r2, #0x730]        @ L2 Sync
L2_sync_loop:
        ldr     r0, [r2, #0x730]
        cmp     r0, #0
        bne     L2_sync_loop

1:      mcr     p15, 0, r1, c7, c0, 4   @ wait for interrupt

        b       2f
2:      ldr     r2, =IO_ADDRESS(MP200_SMU_BASE)
        str     r3, [r2, #0x80]         @ restore CPU div rate
        mov     pc, lr
3:
```

WFI

No.6

Transition from normal operation (Normal A) to QR operation (Normal C). The division setting of ACPU clock is just the same as that of HBUS clock. Before executing this, the interrupts should be disable.

No.7

Prefetch the I-Cache to avoid fetching I-Cache data after Write Buffer Drain Operation and then execute Write Buffer Drain.

No.6

After recovering from WFI, transition from QR operation (Normal C) to normal operation (Normal A).

[Restriction 8] Power switch (L1,L2,L3) control

[Description]

Power switch of the power domain L1,L2 and L3 should be controlled by setting the registers of each power switch and burrier gate control respectively.

- L1&L2 should be controlled by PMU. Please implement the sequence below.
- L3 should be controlled by ACPU. Please implement the sequence below.

【L1 Power Off】

Execute below sequence on PMU

PMU code	PMU command	Macro Select	Register name	Write Data	Count	
0x000A0268, 0x00000000,	REG_WRITE	ASMU	L1_BUZ	0x00000000		L1 burrier gate valid
0x000A026C, 0x00000000,	REG_WRITE	ASMU	L1_BUZ2	0x00000000		↑
0x000A0244, 0x00000F0F,	REG_WRITE	ASMU	L1_POWERSW	0x00000F0F		All of the L1 power switch OFF

【L1 Power On】

Execute below sequence on PMU

PMU code	PMU command	Macro Select	Register name	Write Data	Count	
0x000A0244, 0x00000F07,	REG_WRITE	ASMU	L1_POWERSW	0x00000F07		One of the L1 power switch ON
0x4C000050,	CYCLE_WAIT				0x50	Wait
0x000A0244, 0x00000F03,	REG_WRITE	ASMU	L1_POWERSW	0x00000F03		↑
0x4C000050,	CYCLE_WAIT				0x50	↑
0x000A0244, 0x00000F01,	REG_WRITE	ASMU	L1_POWERSW	0x00000F01		↑
0x4C000050,	CYCLE_WAIT				0x50	↑
0x000A0244, 0x00000F00,	REG_WRITE	ASMU	L1_POWERSW	0x00000F00		↑
0x4C000050,	CYCLE_WAIT				0x50	↑
0x000A0244, 0x00000700,	REG_WRITE	ASMU	L1_POWERSW	0x00000700		↑
0x4C000050,	CYCLE_WAIT				0x50	↑
0x000A0244, 0x00000300,	REG_WRITE	ASMU	L1_POWERSW	0x00000300		↑
0x4C000050,	CYCLE_WAIT				0x50	↑
0x000A0244, 0x00000100,	REG_WRITE	ASMU	L1_POWERSW	0x00000100		↑
0x4C000050,	CYCLE_WAIT				0x50	↑
0x000A0244, 0x00000000,	REG_WRITE	ASMU	L1_POWERSW	0x00000000		↑(All of the L1 power switch ON)
0x4C000050,	CYCLE_WAIT				0x50	↑
0x000A0208, 0x01000000,	REG_WRITE	ASMU	ASMU_BGCTRL	0x01000000		L1 burrier gate invalid
0x000A0268, 0x00001111,	REG_WRITE	ASMU	L1_BUZ	0x00001111		↑
0x000A026C, 0x00000011,	REG_WRITE	ASMU	L1_BUZ2	0x00000011		↑
0x000A0208, 0x00000000,	REG_WRITE	ASMU	ASMU_BGCTRL	0x00000000		↑

【L2 Power Off】

Execute below sequence on PMU

PMU code	PMU command	MacroSelect	Register name	Write Data	Count	
0x000A0500, 0x00000000,	REG_WRITE	ASMU	L2_POWERSW	0x00000000		L2 burrier gate valid
0x000A0500, 0x000000FF,	REG_WRITE	ASMU	L2_POWERSW	0x000000FF		All of the L2 power switch ON

【L2 Power On】

Execute below sequence on PMU

PMU code	PMU command	MacroSelect	Register name	Write Data	Count	
0x000A0500, 0x0000007F,	REG_WRITE	ASMU	L2_POWERSW	0x0000007F		One of the L2 power switch ON
0x4C000010,	CYCLE_WAIT				0x10	Wait
0x000A0500, 0x0000003F,	REG_WRITE	ASMU	L2_POWERSW	0x0000003F		↑
0x4C000010,	CYCLE_WAIT				0x10	↑
0x000A0500, 0x0000001F,	REG_WRITE	ASMU	L2_POWERSW	0x0000001F		↑
0x4C000010,	CYCLE_WAIT				0x10	↑
0x000A0500, 0x0000000F,	REG_WRITE	ASMU	L2_POWERSW	0x0000000F		↑
0x4C000010,	CYCLE_WAIT				0x10	↑
0x000A0500, 0x00000007,	REG_WRITE	ASMU	L2_POWERSW	0x00000007		↑
0x4C000010,	CYCLE_WAIT				0x10	↑
0x000A0500, 0x00000003,	REG_WRITE	ASMU	L2_POWERSW	0x00000003		↑
0x4C000010,	CYCLE_WAIT				0x10	↑
0x000A0500, 0x00000001,	REG_WRITE	ASMU	L2_POWERSW	0x00000001		↑
0x4C000010,	CYCLE_WAIT				0x10	↑
0x000A0500, 0x00000000,	REG_WRITE	ASMU	L2_POWERSW	0x00000000		↑(All of the L2 power switch ON)
0x4C000010,	CYCLE_WAIT				0x10	↑
0x000A0500, 0x00010100,	REG_WRITE	ASMU	L2_POWERSW	0x00010100		L2 burrier gate invalid

【L3 Power Off】

Execute below sequence on ACPU

Register Name	Write Data	
ASMU_L3_POWERSW_BUZ	0x00000000	L3 burrier Valid
ASMU_L3_POWERSW_BUZ	0x000000FF	All of L3 power switch Off

【L3 Power On】

Execute below sequence on ACPU

Register Name	Write Data	
ASMU_L3_POWERSW_BUZ	0x0000007F	One of L3 power Switch On
ASMU_L3_POWERSW_BUZ	0x0000003F	↑
ASMU_L3_POWERSW_BUZ	0x0000001F	↑
ASMU_L3_POWERSW_BUZ	0x0000000F	↑
ASMU_L3_POWERSW_BUZ	0x00000007	↑
ASMU_L3_POWERSW_BUZ	0x00000003	↑
ASMU_L3_POWERSW_BUZ	0x00000001	↑
ASMU_L3_POWERSW_BUZ	0x00000000	↑
ASMU_L3_POWERSW_BUZ	0x00010100	L3 burrier gate invalid

[Restriction 9] USB D- pin pull-down control

[Description]

USB D- pin in EM1 is always pull-down with 15kohm when device mode is used. To use USB without D- pin pull-down, after Initializing, please RUN(=USBCMD register, bit0(R/S)=1), then set the value=0x600e0001 to USBViewport register.