DOCUMENT NUMBER AND REVISION

VL-PS- COG-T180MLH-03 REV. A

(COG-T180MLH-03)

DOCUMENT TITLE:

PRELIMINARY SPECIFICATION

OF

LCD MODULE TYPE

MODEL NUMBER: COG-T180MLH-03

DEPARTMENT	NAME	SIGNATURE	DATE
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CONTENTS

VARITRONIX LIMITED

Preliminary Specification
of
LCD Module Type
Model No.: COG-T180MLH-03

1. General Description

- 128 x RGB x 160 dots 65 K TFT positive transmissive Dot Matrix LCD module.
- Amorphous Silicon TFT active matrix.
- 1.8" (COG type).
- "RENESAS" HD66773R LCD Controller Driver or equivalent.
- Driving scheme: 1/160 duty.
- Viewing angle: 12 o'clock.
- White color LED backlight.
- Normally white.
- Low power.
- Thin thickness.
- With FPC Connection.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	43.4(W) x 60.0(H) x 4.4(D)(Including component)	mm
Active area	28.416(W) x 35.52(H)	mm
Display format	128 x RGB x 160	dots
Color configuration	R.G.B. stripes	-
Dot size	0.218(RGB)(W) x 0.214(H)	mm
Dot spacing	0.004(W) x 0.008(H)	mm
Dot pitch	0.222(RGB)(W) x 0.222(H)	mm
Weight	TBD	gram

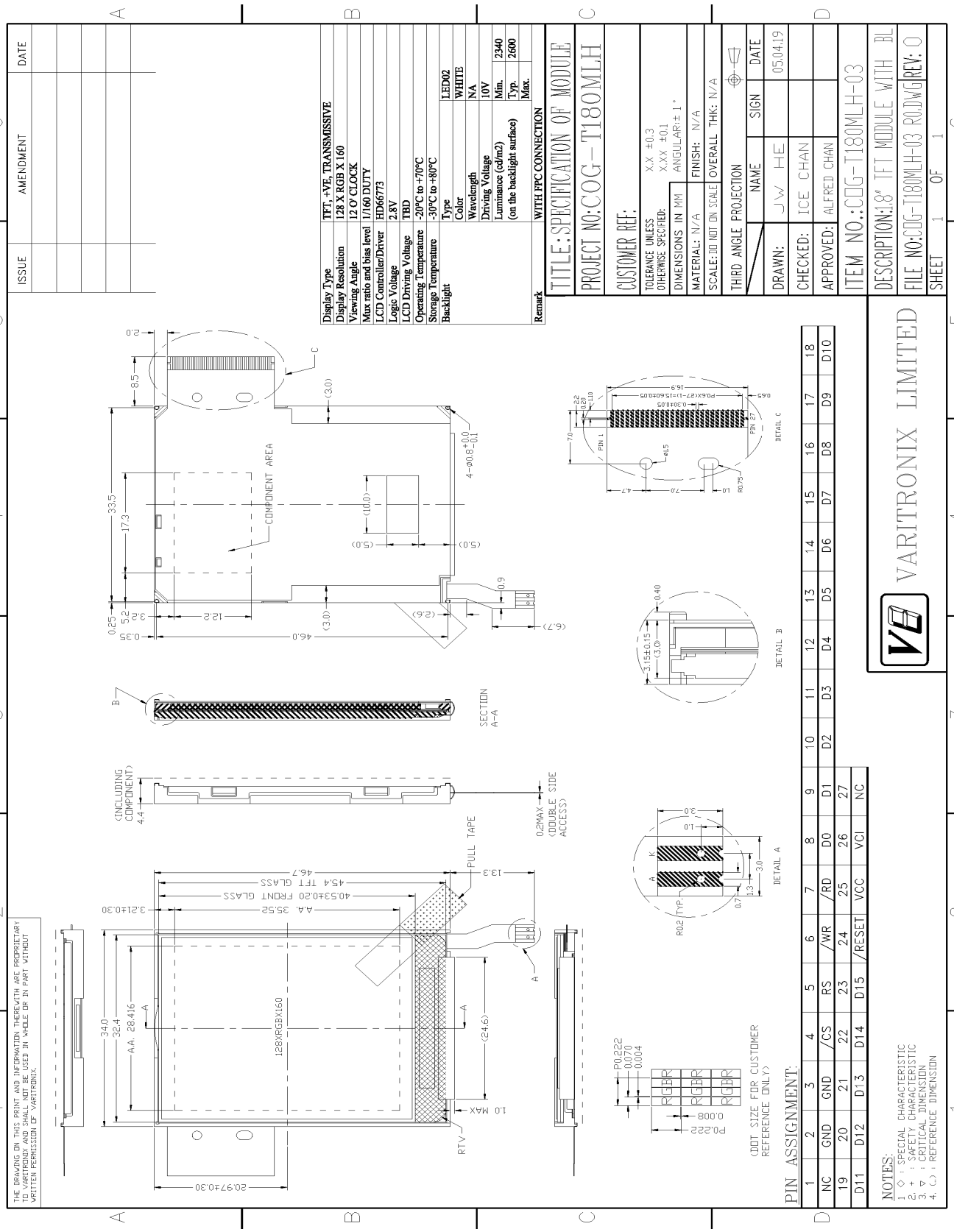


Figure 1: Module Specification

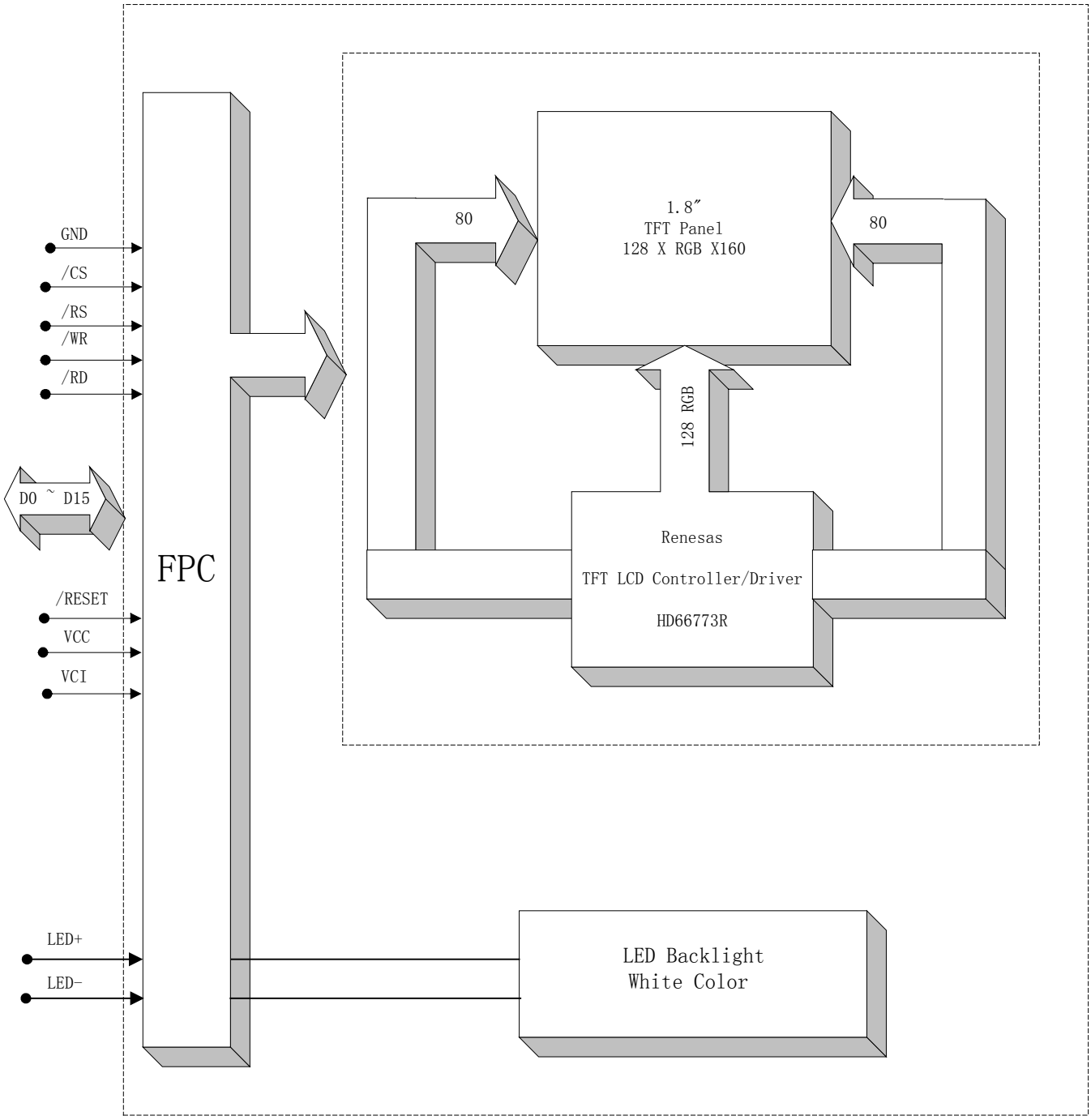


Figure 2: Block Diagram

3. Interface signals

3.1 Interface signals for Module Unit

Table 2

Pin No.	Symbol	Description
1	NC	No Connection.
2	GND	Logic ground GND:0V.
3	GND	Logic ground GND:0V.
4	/CS	Chip selection signal. Low: Select HD66773R and accessible. High: Not select HD66773R and inaccessible.
5	RS	Register selection signal. Low: Index/status. High: Control.
6	/WR	Write strobe signal in 80-system bus interface, write data at low.
7	/RD	Read strobe signal in 80-system bus interface, read data at low.
8	D0	Data 0
9	D1	Data 1
10	D2	Data 2
11	D3	Data 3
12	D4	Data 4
13	D5	Data 5
14	D6	Data 6
15	D7	Data 7
16	D8	Data 8
17	D9	Data 9
18	D10	Data 10
19	D11	Data 11
20	D12	Data 12
21	D13	Data 13
22	D14	Data 14
23	D15	Data 15
24	/RESET	Reset pin. Initialize the LSI at low. Power-on reset required when turning on the power supply. Supply with either one of RESET and the unused pins open.
25	VCC	Logic V_{CC}: +2.2V to +3.3V.
26	VCI	Power supply for analogue circuits. Connect to an external power supply of 2.5V~3.3V.
27	NC	No Connection.

3.2 Backlight Unit (2 Pin FPC Solder Type)

Symbol	Description
A	Anode. LED Input Terminal.
K	Cathode. Ground

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings – For IC Only

Table 3

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VCC-GND	-0.3	+4.6	V
Power Supply voltage (VCI-GND)	VCI-GND	-0.3	+4.6	V
Power Supply voltage (DDVDH)	DDVDH-GND	-0.3	+6.0	V
Power Supply voltage (GND-VCL)	GND-VCL	-0.3	+4.6	V
Power Supply voltage (DDVDH-VCL)	DDVDH-VCL	-0.3	+9.0	V
Power Supply voltage (VGH-GND)	VGH-GND	-0.3	+18.5	V
Power Supply voltage (GND-VGL)	GND-VGL	-0.3	+18.5	V
Input voltage	Vin	-0.3	VCC+0.3	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to GND = 0V.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	-20°C	+70°C	-30°C	+80°C	Dry
Humidity	92% max. RH for Ta ≤ 40°C < 92% RH for Ta > 40°C				No condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration: 11 ms Peak acceleration: 981 m/s^2 = 100 g Number of shocks: 3 shocks in 3 mutually perpendicular axes.				3 directions

5. Electro-Optical Characteristics

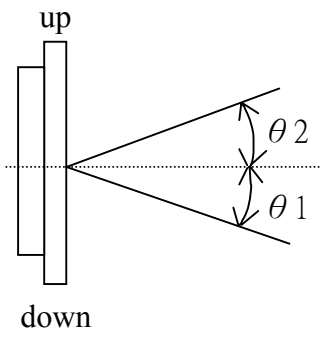
Table 5

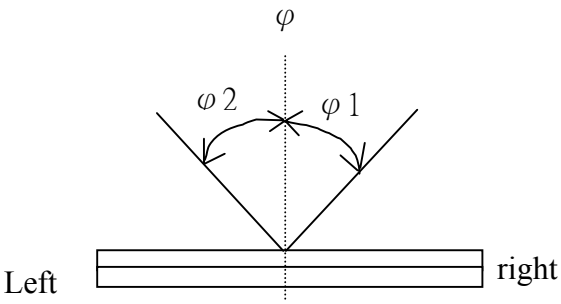
Item	Symbol	Temp. °C	Value			Unit	Condition	
			Min.	Typ.	Max.			
Response Time	τ r + τ d	+25	-	40	-	msec	θ = 0 °, ϕ = 0°, Note 1	
Optimum Viewing Area	θ 1	+25	-	45	-	DEG	ϕ = 0 °	C/R>10.
	θ 2		-	45	-			
	ϕ 1		-	35	-		θ = 0°	
	ϕ 2		-	15	-			
Color Gamut	S(%)	+25	-	45	-	%	Note 2	
CIE Color coordinate	Rx	+25	0.576	0.596	0.616		Note 3	
	Ry	+25	0.312	0.332	0.352			
	Gx	+25	0.285	0.305	0.325			
	Gy	+25	0.521	0.541	0.561			
	Bx	+25	0.125	0.145	0.165			
	By	+25	0.153	0.173	0.193			
	Wx	+25	0.283	0.298	0.313			
	Wy	+25	0.305	0.320	0.335			
Contrast Ratio	Cr	+25	-	250	-	-	Vop = Optimum voltage θ = 0 °, ϕ = 0°.	
Panel Transmittance		+25	-	24	-	%	Note 2	
Dot Aperture Ratio		+25	-	67	-	%		
Luminance		+25	-	200	-	cd/m^2	B/L= 2500 cd/m^2	

Note (1): Response time depends on the temperature.
(In lower temperature, it becomes longer.).
(2): Without polarizer.
(3): Color Filter glass.

6. Optical Characteristics Definition

a.) Viewing Angle θ

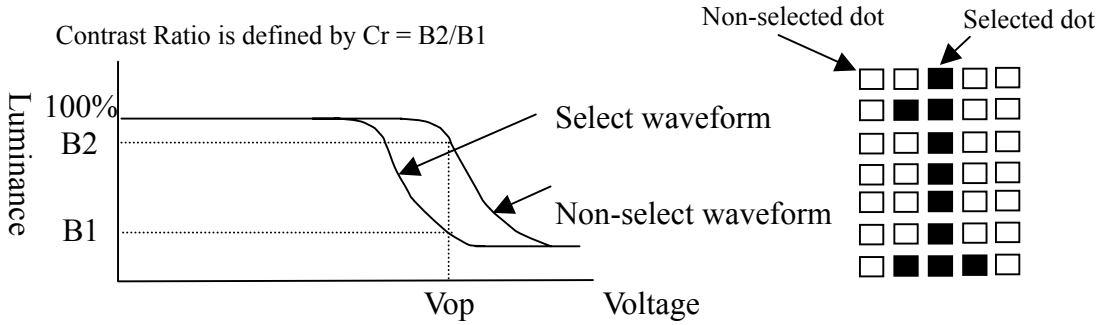




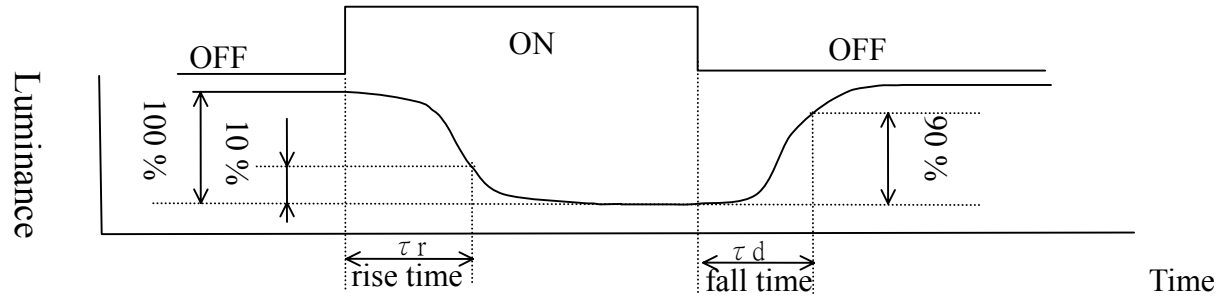
b.) Contrast Ratio

B1 = segments luminance in case of non-selected waveform

B2 = segments luminance in case of selected waveform

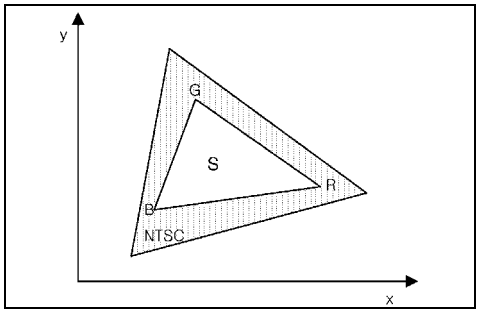


c.) Response Time



d.) Color Gamut

Color Gamut: S(%)=(RGB triangle Area/NTSC Triangle Area)x100



7. Electrical Specifications

7.1 Typical Electrical Characteristics

At Ta = 25 °C, VCC = 2.2V to 3.3V, GND=0V.

Table 6

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VCC-GND		2.2	2.8	3.3	V
DC/DC supply voltage	VCI		2.5	2.8	3.3	V
TFT Gate ON Voltage	VGH (Note 1)	At Ta=25°C±5°C (Note 3)	12	-	20	V
TFT Gate OFF Voltage	VGL (Note 2)		-10	-	-4	V
TFT Common Electrode Voltage	Vcom		-2	-	4	V
Input signal voltage	V_{IH}	"H" level, VCC=2.2 to 3.3V	0.7VCC	-	VCC	V
	V_{IL1}	"L" level VCC=2.2 to 3.3V (For OSC1 pin)	-0.3	-	0.15VCC	V
	V_{IL2}	"L" level VCC=2.2 to 2.4V (Except OSC1 pin)	-0.3	-	0.15VCC	V
		"L" level VCC=2.4 to 3.3V (Except OSC1 pin)	-0.3	-	0.2VCC	V
Supply Current (Logic & LCD)	ICC+ICI	Standard mode, VCC=3V	-	1.32	-	mA
Supply voltage of white LED backlight	VLED	Forward current =15 mA Number of LED dies =3	-	10	-	V
Luminance of white LED backlight (on the backlight surface)			2340	2600	-	cd/m^2

Note (1): VGH is TFT Gate operating voltage.

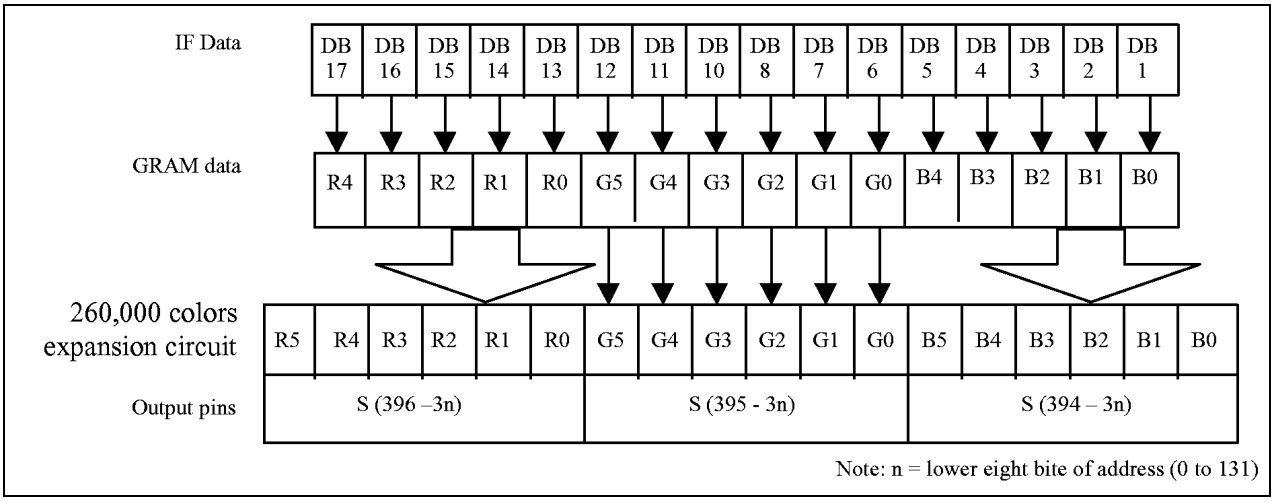
(2): VGL is TFT Gate operating voltage, VGL signal must be fluctuated with same phase as Vcom when Storage on Gate structure.

(3): Vcom must be adjusted to optimize display performance such as: crosstalk, contrast ratio and etc.

7.2 Register Selection

80-system		RS	Operation
WR*	RD*		
0	1	0	Writes indexes into IR
1	0	0	Reads internal status
0	1	1	Writes into control registers and GRAM through WDR
1	0	1	Reads from GRAM through RDR

7.3 16-bit interface



7.4 Reset Function

The HD66773R makes internal initial settings with RESET input. During the RESET, the HD66773R is in a busy state, and no instructions from the MPU AND ACCESS TO gram are accepted. The time required for the RESET input is at least 1ms. In case of power-on reset, wait at least 10ms after the power is turned on until the R-C oscillation frequency becomes stabilized. While waiting, do not make initial settings for the instruction set, nor access to GRAM.

7.5 Initial State of Instructions

a. Start oscillation
b. Driver output control (NL4–0 = "10101", SS = "0", CS = "0")
c. Liquid crystal AC drive control (FLD1-0 = "01", B/C = "0", EOR = "0", NW5–0 = "00000")
d. Power control 1 (BT2-0 = "000", DC2–0 = "000", AP2–0 = "000": liquid crystal power supply off, SLP = "0", STB = "0" : Standby mode off)
e. Power control 2 (CAD = "0")
f. Entry mode set (DIT = "0", BGR = "0", HWM = "0", I/D1-0 = "11": Increment by 1, AM = "0": Horizontal direction, LG2–0 = "000": Replace mode)
g. Compare register (CP15–0 : "0000 0000 0000 0000")
h. Display control (PT1-0 = "00", VLE2-1 = "00": No vertical scroll, SPT = "0", GON = "0", DTE = "0", CL = "0": 262,144 colors, REV = "0", D1-0 = "00": Display OFF)
i. Power control 3 (VC2-0 = "000")
j. Power control 4 (VRL3-0 = "0000", PON = "0", VRH3-0 = "0000")
k. Power control 5 (VDV4-0 = "00000", VCOMG = "0", VCM4-0 = "00000")
l. Frame cycle control (NO1-0 = "00", SDT1-0 = "00", EQ1-0 = "00" : No equalization, DIV1-0 = "00": clock/1, RTN3-0 = "0000" : 16 clocks in 1H period)
m. Gate scan starting position (SCN4-0 = "00000")
n. Vertical scroll (VL7–0 = "00000000")
o. 1st split-screen (SE17-10 = "11111111", SS17-10 = "00000000")
p. 2nd split-screen (SE27-20 = "11111111", SS27-20 = "00000000")
q. Horizontal RAM address position (HEA7-0 = "10000011", HSA7-0 = "00000000")
r. Vertical RAM address position (VEA7-0 = "10101111", VSA7-0 = "00000000")
s. RAM write data mask (WM15–0 = "0000"H: No mask)
t. RAM address set (AD15–0 = "0000"H)
u. γ control
(PKP02-00 = "000", PKP12-10 = "000", PKP22-20 = "000", PKP32-30 = "000", PKP42-40 = "000", PKP52-50 = "000", PRP02-00 = "000", PRP12-10 = "000")
(PKN02-00 = "000", PKN12-10 = "000", PKN22-20 = "000", PKN32-30 = "000", PKN42-40 = "000", PKN52-50 = "000", PRN02-00 = "000", PRN12-10 = "000")
(VRP14-10 = "00000", VRP03-00 = "0000", VRN14-10 = "00000", VRN12-10 = "000")

7.6 GRAM Data Initialization

The data in GRAM are not initialized with the RESET input. Initialize through software during the display OFF (D1–0 = "00").

7.7 Initial State of Output Pin

a. Liquid crystal driver output pins (source outputs): Output GND level
Liquid crystal driver output pins (gate outputs): Output VGH level

b. Oscillator output pin (OSC2): Output oscillation signal

7.8 Timing Characteristics

At Ta=-20°C to +70°C

80-system Bus Interface Timing Characteristics

Normal Write Mode (HWM=0) (Vcc = 2.2 to 2.4 V)

Item		Symbol	Unit	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	600	—	—
	Read	t_{CYCR}	ns	800	—	—
Write low-level pulse width		PW_{LW}	ns	90	—	—
Read low-level pulse width		PW_{LR}	ns	350	—	—
Write high-level pulse width		PW_{HW}	ns	300	—	—
Read high-level pulse width		PW_{HR}	ns	400	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	—	—	25
Setup time (RS to CS*, WR*, RD*)		t_{AS}	ns	10	—	—
Address hold time		t_{AH}	ns	5	—	—
Write data set up time		t_{DSW}	ns	60	—	—
Write data hold time		t_{H}	ns	15	—	—
Read data delay time		t_{DDR}	ns	—	—	200
Read data hold time		t_{DHR}	ns	5	—	—

High-Speed Write Mode (HWM=1) (Vcc = 2.2 to 2.4 V)

Item		Symbol	Unit	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	200	—	—
	Read	t_{CYCR}	ns	800	—	—
Write low-level pulse width		PW_{LW}	ns	90	—	—
Read low-level pulse width		PW_{LR}	ns	350	—	—
Write high-level pulse width		PW_{HW}	ns	90	—	—
Read high-level pulse width		PW_{HR}	ns	400	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	—	—	25
Set up time (RS to CS*, WR*, RD*)		t_{AS}	ns	10	—	—
Address hold time		t_{AH}	ns	5	—	—
Write data set up time		t_{DSW}	ns	60	—	—
Write data hold time		t_{H}	ns	15	—	—
Read data delay time		t_{DDR}	ns	—	—	200
Read data hold time		t_{DHR}	ns	5	—	—

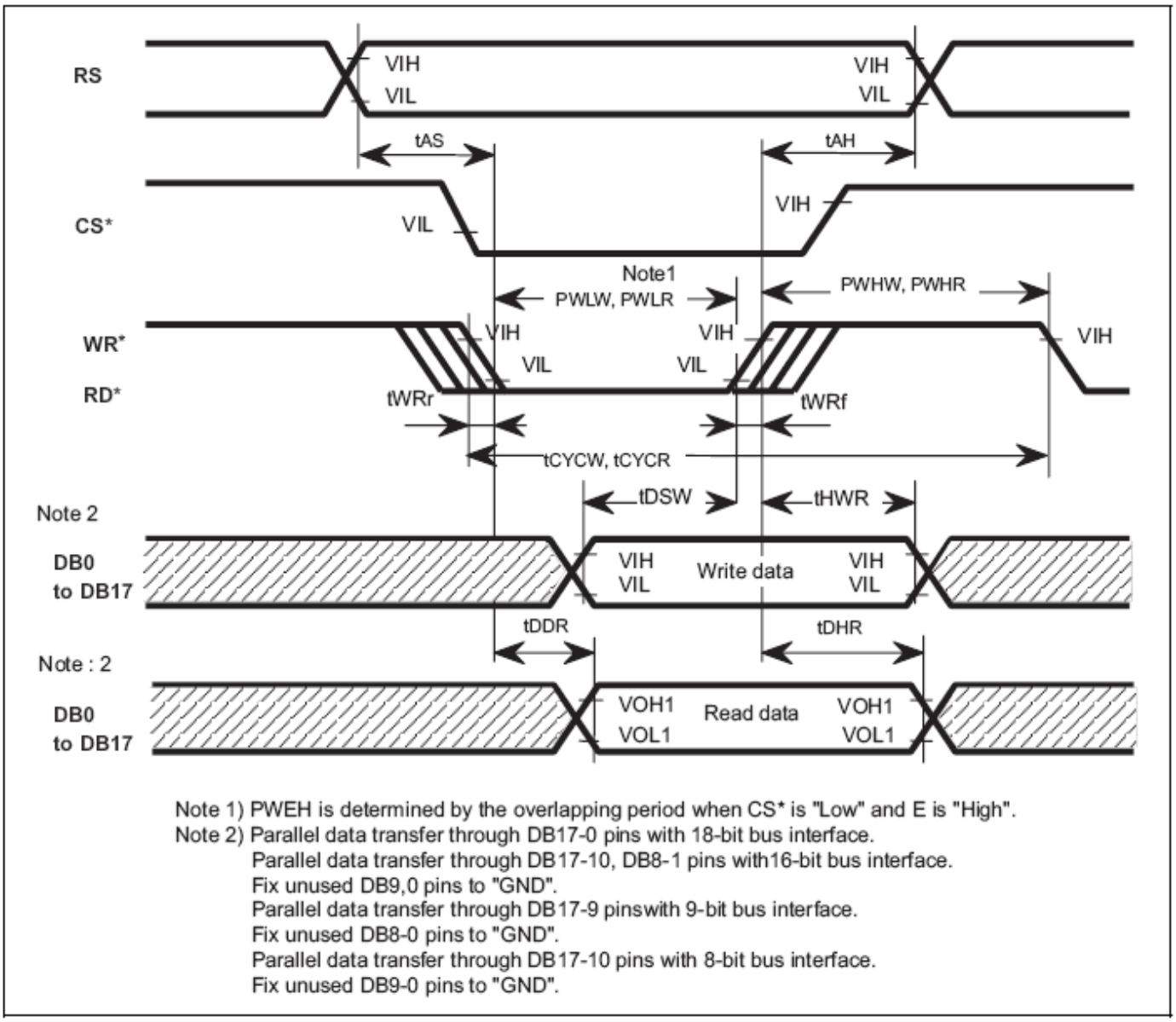
Normal Write Mode (HWM=0)
(Vcc = 2.4 to 3.3 V)

Item		Symbol	Unit	Min	Typ	Max	Note
Bus cycle time	Write	t_{CYCW}	ns	200	—	—	
	Read	t_{CYCR}	ns	300	—	—	
Write low-level pulse width		PW_{LW}	ns	40	—	—	
Read low-level pulse width		PW_{LR}	ns	150	—	—	
Write high-level pulse width		PW_{HW}	ns	100	—	—	
Read high-level pulse width		PW_{HR}	ns	100	—	—	
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	—	—	25	
Set up time (RS to CS*, WR*, RD*)		t_{AS}	ns	10	—	—	When using status read
				0	—	—	When not using status read
Address hold time		t_{AH}	ns	2	—	—	
Write data setup time		t_{DSW}	ns	60	—	—	
Write data hold time		t_{H}	ns	2	—	—	
Read data delay time		t_{DDR}	ns	—	—	100	
Read data hold time		t_{DHR}	ns	5	—	—	

High-Speed Write Mode (HWM=1)

(Vcc = 2.4 to 3.3 V)

Item		Symbol	Unit	Min	Typ	Max	Note
Bus cycle time	Write	t_{CYCW}	ns	100	—	—	
	Read	t_{CYCR}	ns	300	—	—	
Write low-level pulse width		PW_{Lw}	ns	40	—	—	
Read low-level pulse width		PW_{LR}	ns	150	—	—	
Write high -level pulse width		PW_{HW}	ns	40	—	—	
Read high -level pulse width		PW_{HR}	ns	100	—	—	
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	—	—	25	
Set up time (RS to CS*, WR*, RD*)		t_{AS}	ns	10	—	—	When using status read
				0			When not using status read
Address hold time		t_{AH}	ns	2	—	—	
Write data set up time		t_{DSW}	ns	60	—	—	
Write data hold time		t_{H}	ns	2	—	—	
Read data delay time		t_{DDR}	ns	—	—	100	
Read data hold time		t_{DHR}	ns	5	—	—	



Note 1) PWEH is determined by the overlapping period when CS* is "Low" and E is "High".
Note 2) Parallel data transfer through DB17-0 pins with 18-bit bus interface.
Parallel data transfer through DB17-10, DB8-1 pins with16-bit bus interface.
Fix unused DB9,0 pins to "GND".
Parallel data transfer through DB17-9 pinswith 9-bit bus interface.
Fix unused DB8-0 pins to "GND".
Parallel data transfer through DB17-10 pins with 8-bit bus interface.
Fix unused DB9-0 pins to "GND".

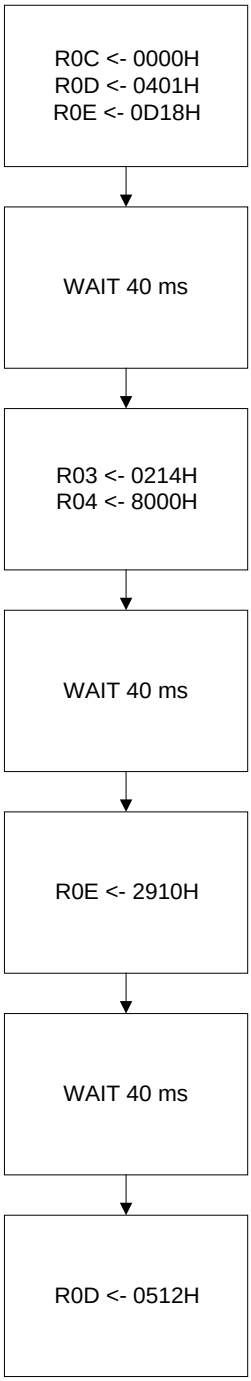
Figure 3: 80-system Bus Timing Diagram

8. Programming Reference

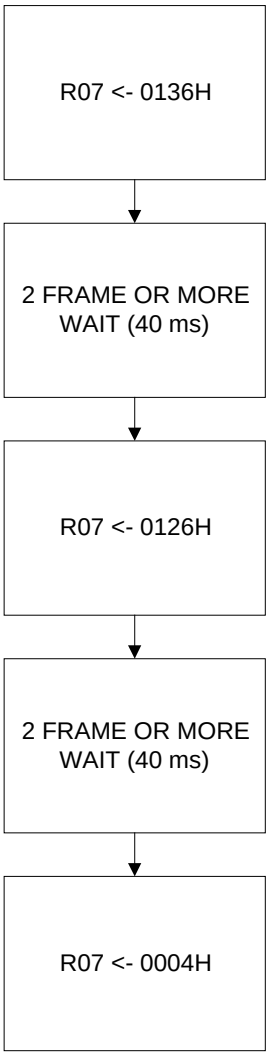
Initialization function 1
R01←0115h
R02←0700h
R05←0230h
R06←0000h
R07←0104h
R0B←0000h

Initialization function 2
R21←0100h
R30←0000h
R31←0000h
R32←0000h
R33←0000h
R34←0000h
R35←0707h
R36←0707h
R37←0000h
R0F←0000h
R11←0000h
R14←5C00h
R15←A05Dh
R16←7F00h
R17←A000h
R3A←0000h
R3B←0000h

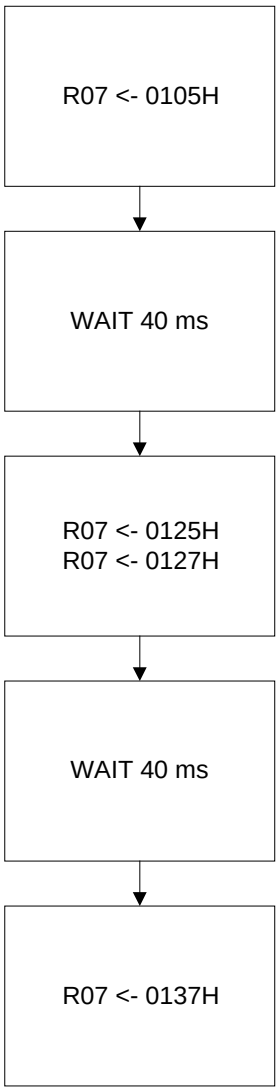
Power Setting Function



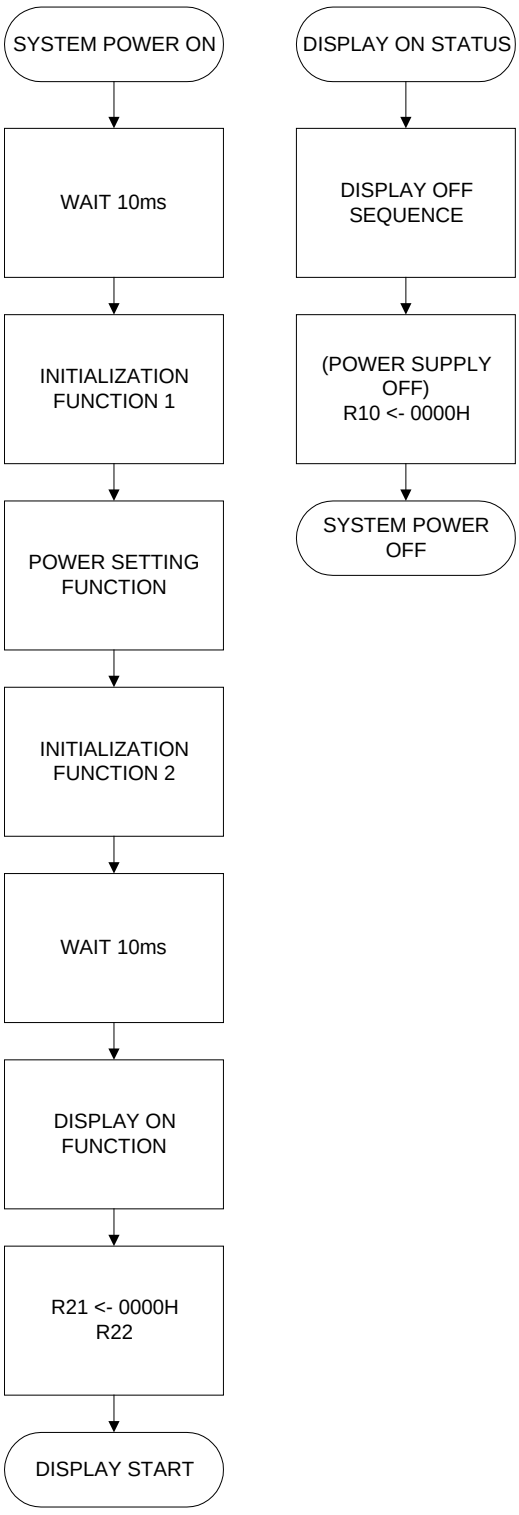
Display Off Function



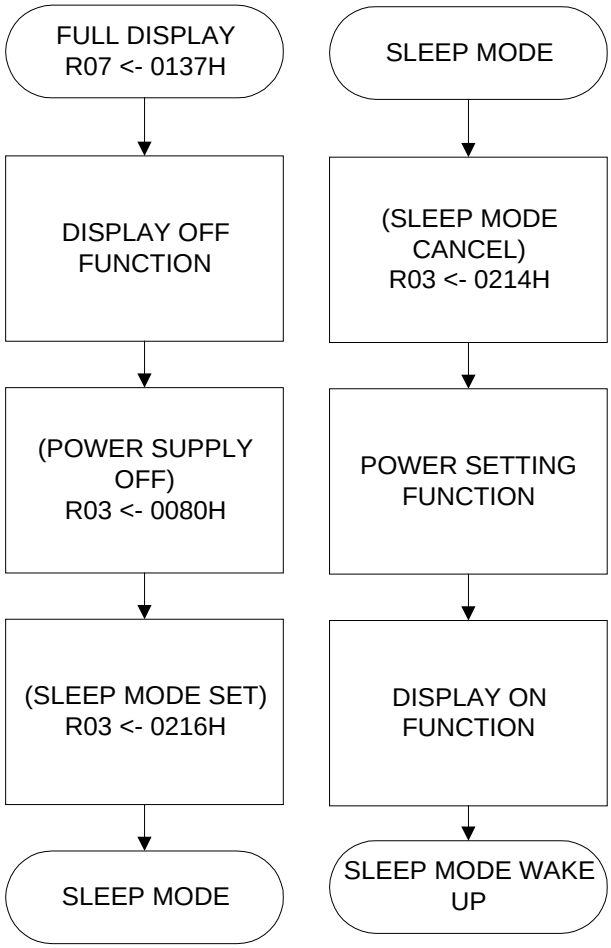
Display On Function



Power On/Off Sequence



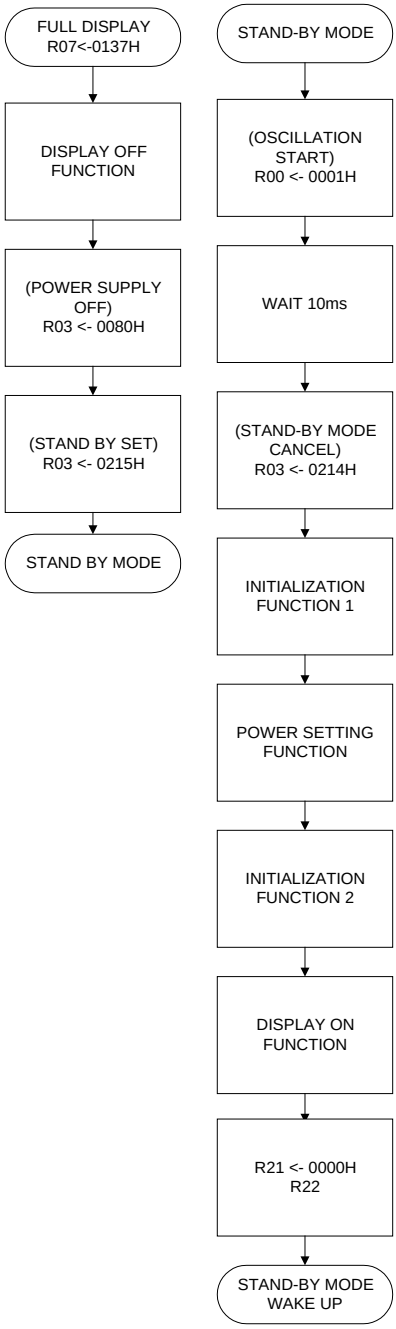
Sleep Mode/ Wake Up Sequence (Oscillator is ON)



Note: 1) During sleep mode, GRAM data and instructions are retained.

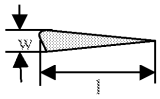
2.) In the sleep mode, the system must stop sending CPU I/F signals.

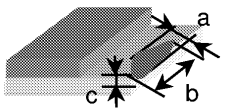
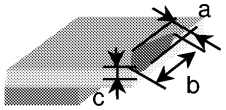
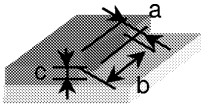
Stand By Mode / Wake Up Sequence (Oscillator is OFF)

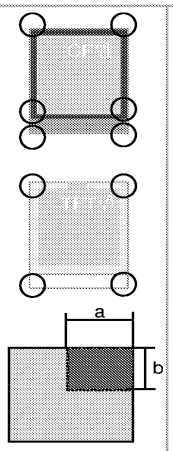


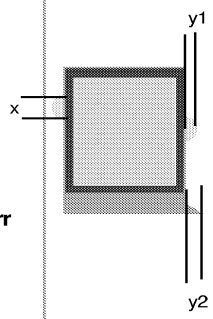
9. Incoming Inspection Standard

9.1 Inspection Criteria

Item	Criterion for Defects	Defect Type	Remark
Non Display	Non Display is not allowed	Major	
Line Defect	All Kinds of Line defects Such as Vertical,Horizontal,Cross are not allowed	Major	
Dot	Item: Bright Dot — Acceptable No: 0; Dark Dot — 1	Minor	
[Spot] **Black Spot** **White Spot** **Bright Spot** **Pinhole** **Foreign Particle** **Scratch**	 Size Φ (mm) / Acceptable Number: Φ ≤ 0.1 — Ignore; 0.1 < Φ ≤ 0.2 — 1; Φ > 0.2 — 0	Minor	
[Line] **Black Line** **White Line** **Foreign Particle** **Scratch**	 * If we cannot see any Scratch through Backside of scratched area, It is Acceptable Width (mm) / Length (mm): W≤ 0.03 — Ignore; 0.03< W ≤ 0.05 — L ≤ 3.0; 0.05 < W ≤ 0.1 — L ≤ 2.0	Minor	

Item	Criterion for Defects	Defect Type	Remark
Glass Chipping **[Pad Area]**	 Size (mm): a ≤ 0.5; b : Ignore; c ≤ 0.45	Minor	
Glass Chipping **[Rear of** **Pad Area]**	 Size (mm): a ≤ 0.5; b : Ignore; c ≤ 0.45	Minor	
Glass Chipping **[Except Pad** **Area]**	 Size (mm): a ≤ 0.5; b : Ignore; c ≤ 0.45	Minor	

<table>
<tr><th>Item</th><th>Criterion for Defects</th><th>Defect Type</th><th>Remark</th></tr>
<tr><td>Glass Chipping
[Corner]</td><td> 

<table>
<tr><th>Size (mm)</th></tr>
<tr><td>a ≤ 3.0</td></tr>
<tr><td>b ≤ 3.0</td></tr>
</table>
No Touch Sealant and Gate Line
No Touch Signal line
No Touch Customer's Align Mark</td><td>Minor</td><td></td></tr>
<tr><td>Glass burr</td><td> 

<table>
<tr><th>Size (mm)</th><th>Acceptable Number</th></tr>
<tr><td>x : Ignore</td><td></td></tr>
<tr><td>y ≤ 0.2</td><td>4</td></tr>
</table>
If y1 > y2 then y = y1</td><td>Minor</td><td></td></tr>
</table>

9.2 Inspection Method

9.2.1 Ambient conditions

a. Temperature : **25±5°C**

b. Humidity : **65±10% RH**

c. Illumination : **Single fluorescent lamp non-directive (300 to 700 Lux)**

d. LCM Brightness : **Minimum 120 cd/m^2 (with Polarizer)**

9.2.2 Viewing distance

The distance between the LCD and the inspector's eyes shall be at least 30-50 cm.

9.2.3 Viewing Angle

Display Quality: The inspection shall be conducted within normal viewing angle range.

9.3 Classification of defects

Defects are classified as either a major defect or a minor defect based on the degree of defect defined herein.

9.3.1 Major defect

The major defect is a defect that is likely to result in product failure, or reduction in the product's intended usage.

9.3.2 Minor defect

The minor defect is a defect that has little bearing on the effective use or operation of the product.

The Customer shall return the rejected LCD to the place to be designated by the Supplier and the Supplier shall screen all of the products in the lot and repair or replace the defective LCDs.

9.4 Incoming inspection Right

The Customer shall have the right to conduct at its own cost and expense, an incoming inspection of the LCDs at the destination specified in the relevant B/L(Bills of Lading) in accordance with the LCD's specifications separately agreed upon and the inspection criteria set forth in this article.

The Customer shall notify the Supplier in writing of the inspection results(acceptance or rejectance) in accordance with the said Incoming Inspection Standard within 40 days from the date of the B/L.

Should the Customer fail to notify the results to Supplier within 40 days period, the right to reject the LCDs shall then lapse, and the said LCDs shall be deemed to have been accepted by the Customer.

9.5 Handling Precautions

- LCD Devices are made of fragile material such as Glass and may be broken or cracked if dropped it, so **PLEASE** handle them with care.
- Please **DO NOT** touch the surface of the Glass.
- **PLEASE** wear the Wrist Strap when handling.
  Semiconductive devices are included in the LCD and they should be handled with care to prevent any electrostatic discharge(ESD).
- **PLEASE** keep the LCDs in the specified, original packing boxes when storage.
- Before use the LCDs, **PLEASE** check the Engineering specification.
- LCDs contain a small amount of Liquid Crystal. **PLEASE** follow local ordinances or regulations for disposal.

"Varitronix Limited reserves the right to change this specification."

URL:http://www.varitronix.com

- END -