Easy Radio LV24230

Application Note

DS2423S03

PRELIMINARY

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Revision History

V00.0 Initial Version

V01.0 2006/08/03

6. The setting of FM Frequency Target Value Calculation Method collect

V02.0 2006/08/24

register RADIO_CTRL3

V03.0 2006/09/25

ES4

FS5Db add Seek Stop level from 8 step to 16 step

If frequency selection 130KHz or 150KHz

FLL and Smooth bit separate

Change the measurement time of frequency

V03.1 2006/10/04

Change the gate time for SD_OSC setting

Add the initial stable time of self oscillation

V03.2 2006/10/13

Add interrupt explanation <Supplement>

V03.3 2007/02/26

Add command sequence of seek

V03.3 2007/04/13

Reserved register 1Dh value change 1 to 0

FLL mode setting after Frequency setting or Scan mode

■Table of content

Basic Information

LV24230 is space-saving, a small and low power consumption FM stereo radio IC. Interface is based on an I2C bus.

Feature

A standard clock can connect the input from a host or crystal of 32.768KHz directly

Also it is equipped with an automatic frequency setting function, automatic search feature.

I2C Interface

This IC is based on I2C.

The device address of I2C is 0xC0(write register) and 0xC1(read register)

The sub address is shown on register map of Table1.

Software control specification

At the time of power up, LV24230 move stand-by mode automatically. The PW_RAD of RADIO_CTRL3(Register 0Fh ,Bit0) is set 0. The other register becomes unsettled.

Please set the register value by following table 2. After initial setting, FM station setting, the seek of radio station is possible by using simple command via I2C.

This application note explains the setting method and recommend value for each parameter.

Table 1 LV24230 Register Map

Following is Sub address map of LV24230. Each register becomes 8bit constitution.

Address	Register Name	Mode	Remark
00h	CHIP_ID	R/W	Chip ID
02h	RADIO_STAT	R	Status of Radio Station
0Bh	RFCAP	R/W	RF Cap bank
0Dh	RADIO_CTRL1	R/W	Radio Control 1
0Eh	RADIO_CTRL2	R/W	Radio Control 2
0Fh	RADIO_CTRL3	R/W	Radio Control 3
10h	TNPL	R	Tune Position Low
11h	TNPH_STAT	R	Tune Position High and Status
19h	REF_CLK_PRS	R/W	Reference clock pre-scalar
1Ah	REF_CLK_DIV	R/W	Reference clock divider
1Bh	REF_CLK_OFF	R/W	Reference clock offset
1Dh	SCN_CTRL	R/W	Scan control
1Eh	TARGET_VAL_L	R/W	Target value Low
1Fh	TARGET_VAL_H	R/W	Target value High

R --- Read only register R/W --- Read and Write register

Each Sequence

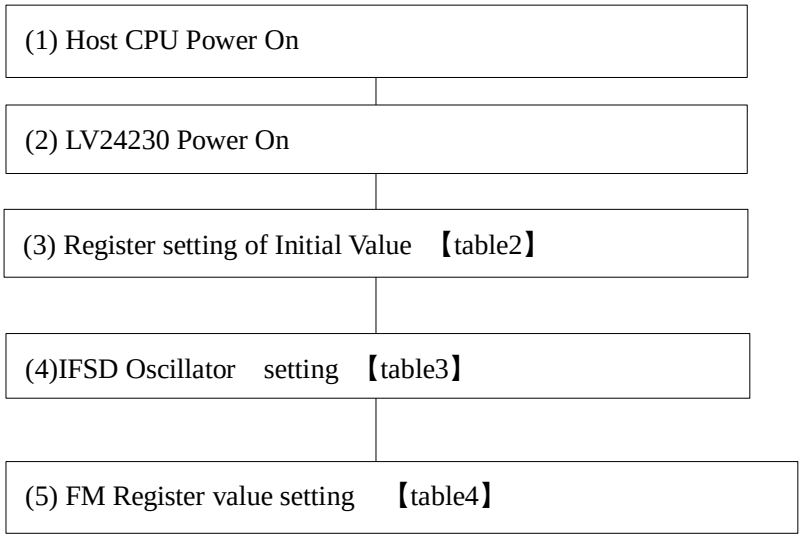
1. Power On

At the time of power on, LV24230 move stand-by mode automatically. The PW_RAD of RADIO_CTRL3 (Register 0Fh ,Bit0) is set 0. The other register becomes unsettled.

Please set the register value by following table 2 and fix the value of register.

Also the initial setting of an oscillator is necessary after power supply injection once.

The following is the sequence of after power on



・(1) & (2) same timing is acceptable.

・Between (2) and (4), more than 200msec need

・Between (4) and (5), wait time more than 200msec is necessary.

・In case of self oscillation crystal, more than 300msec is necessary for as oscillation stability time.

Table 2: Register value for initial setting

No	Address	register name (Write)	Bit		Initial Value		Explanation
					BIN	HEX	
1	0Bh	RF_CAP	Bit7:0			FF	RF
2	0Dh	RADIO_CTRL1	Bit7	IF_SEL	0	61	IF130K
			Bit6	IFBWSEL	1		IFBW100%
			Bit5	AGC_SPD	1		HIGH
			Bit4	DEEM	(0)		(50us) Depend on Area.[1]
			Bit3	ST_M	0		Stereo
			Bit2	nMUTE	0		Mute
			Bit1:0	VOL	1		0-3
3	0Eh	RADIO_CTRL2	Bit7:5	SOFTST	2	50	L1
			Bit4:2	SOFTMT	4		L2
			Bit1	Reserved	0		-
			Bit0	STABI_BP	0		Enable
4	19h	REF_CLK_PRS	Bit7:5	REFPRE	4	80	SD PRE
			Bit4:0	REFMOD	0		SD mod
5	1Ah	REF_CLK_DIV	Bit7:0	REFDIV		82	SD Divider
6	1Bh	REF_CLK_OFF	Bit7:0	REFOFF		0	
7	1Dh	SCN_CTRL	Bit7:6	GRID	0	02	Calibration
			Bit5	FLL_ON	0		OFF
			Bit4	Reserved	0		
			Bit3:1	FS	1		Calibrate SD oscillator
			Bit0	SHFS5DB	(0)		FS + 5dBuV
8	0Fh	RADIO_CTRL3	Bit7	IPOL	0	13	IRQ High
			Bit6	SM_IE	0		Command end IRQ
			Bit5	RAD_IE	0		RIRQ Disable
			Bit4	SD_PM	1		Calibration mode
			Bit3	nIF_PM	0		Calibration mode
			Bit2:1	EXT_CLK_CFG	(1)		32K crystal osc
			Bit1:0	PW_RAD	1		Power On

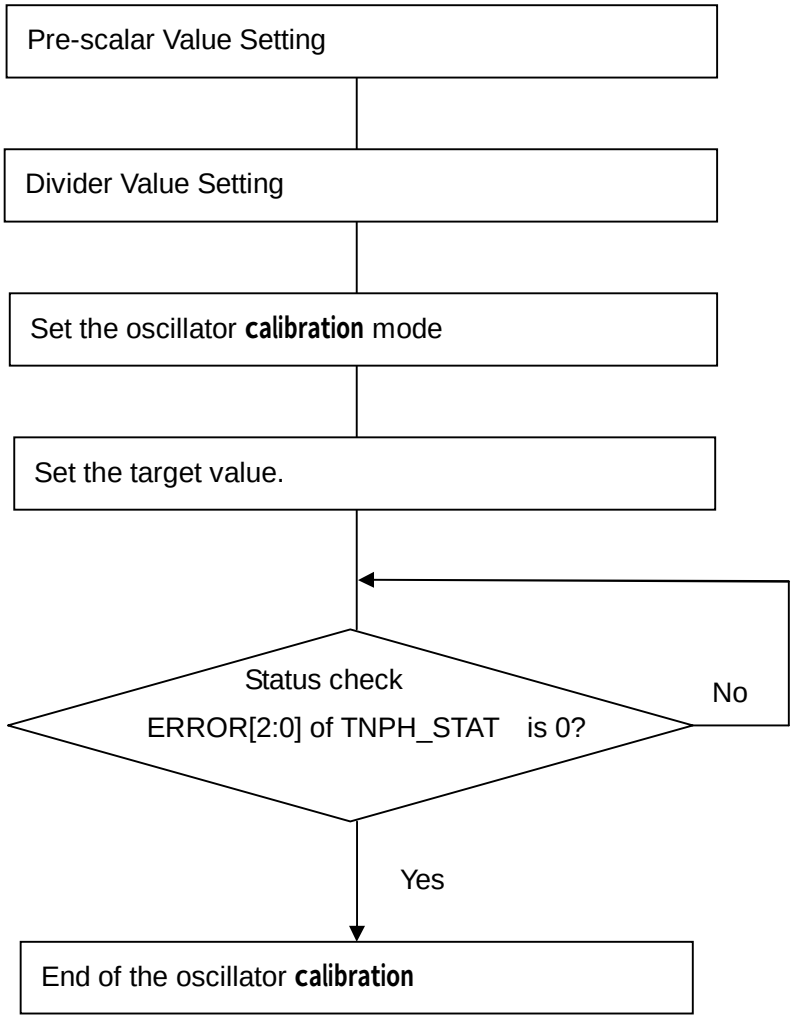
[1] De-emphasis 50us :CHINA, Republic of KOREA, JAPAN, EUROPE
75 us: USA

2. IF/SD Oscillator Setting

After initialization of register <table2> the calibration of IF/SD oscillator is necessary once
To set up this oscillator, the reference clock for frequency measurement is necessary.
The reference clock frequency is acceptable from 32.768K to 20M Hz.

After setting PRESCALER value and **DIVIDER value, at the write timing of target value, calibration of oscillator start automatically.**
During the calibration of oscillator, the status <ERROR[2:0] of TNPN_STAT> is busy.
When the calibration of oscillator was finished, the status change to OK.
The time of oscillator calibration is around 500～600msec.
Please check the status <ERROR[2:0] of TNPN_STAT>

Following is the sequence of oscillator setting.



***During the calibration of oscillator and seek mode, LV24230 is set mute mode automatically.**

After setting PRESCALER value and **DIVIDER value, at the write timing of target value, calibration of oscillator start automatically.**
During the calibration of oscillator, the status <ERROR[2:0] of TNPN_STAT> is busy.
When the calibration of oscillator was finished , the status change to OK.
The time of oscillator calibration is around 500～600msec.
Please check the status <ERROR[2:0] of TNPN_STAT>

Following is the command sequence of oscillator calibration.

Table 3 Command Sequence of SD Oscillator Setting

No	Address	Register name	Bit		HEX	
1	1E	TARGET_VAL_L	bit7:0		06	Target Value LOW Byte
2	1F	TARGET_VAL_H	Bit6:0		13	Target Value HIGH Byte
3	11	TNPH_STAT	bit5:7	ERROR	Not 7	If status is busy, continue Wait
4	0F	RADIO_CTRL3	bit4		0	SD PLL Locking
			bit3		1	IF PLL Locking

TNPH_STAT is read only register

3. Register Setting for FM mode

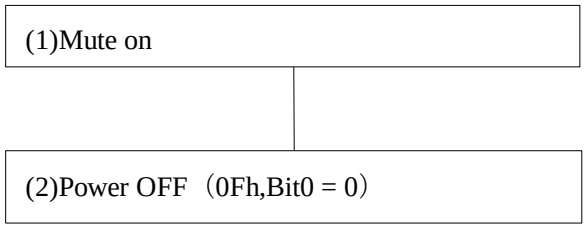
After Oscillator calibration, the register of Pre-scaler and Divider setting is needed for FM setting. Also for seek search, seek step and seek stop level setting is needed.

Table 4: Register value for FM mode

No	Address	register name (Write)	Bit		Initial Value		Explanation
					BIN	HEX	
1	19h	REF_CLK_PRS	Bit7:5	REFPRE	2	43	FM PRE
			Bit4:0	REFMOD	3		FM mod
2	1Ah	REF_CLK_DIV	Bit7:0	REFDIV		14	FM Divider
3	1Bh	REF_CLK_OFF	Bit7:0	REFOFF		C0	FM Offset
4	1Dh	SCN_CTRL	Bit7:6	GRID	(2)	88	FM Frequency (Step = 100KHz)
			Bit5	FLL_ON	0		FLL OFF
			Bit4	Reserved	0		
			Bit3:1	FS	(4)		SEEK STOP Level
			Bit0	SHFS5DB	(0)		Seek Stop level + 5db

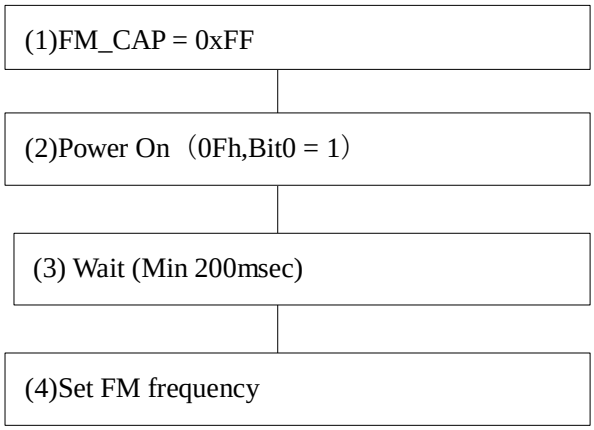
4. Stand-by On

Following is the sequence for standby mode



5. Stand-by Off

Following is the sequence for standby off mode



6. The setting of FM Frequency

In Fm frequency setting mode, firstly PRESCALAR value ,DIVIDER value ,OFFSET、MOD is set to each register.

After target value is wrote in **TARGET_VAL_L register and TARGET_VAL_H register, FM setting start.**

When the setting is finished, the status will change no busy.

So please check the status. the FM setting time is about **100～200msec.**

Fix the target value

When the target value is wrote, FM setting start. Target value is fixed by following calculation.

Target Value = (Target frequency *100 – 6400 <FIX>) ÷ 5

< Example of 90MHz >

Target Value = : (9000 – 6400) ÷ 5 = 520 = 0208h

TARGET_VAL_L register = 08h and TARGET_VAL_H register = 02h

The following is the command sequence of FM frequency setting.

Table 5 Command Sequence of FM frequency setting

	Address	register name	Bit		Setting Value		Explanation
					BIN	HEX	
1	1Eh	TARGET_VAL_L	Bit7:0		*		Target Value Low Byte
2	1Fh	TARGET_VAL_H	Bit7		0		Setting FM frequency
			Bit6:0		*		Target Value High Byte
3	11h	TNPH_STAT	Bit7:5	ERROR		Not 7	Wait without BUSY Time Out :400msec
4	1Dh	SCN_CTRL	Bit5	FLL_ON	1		FLL ON after Frequency setting

Note: Please set the FLL ON mode after FM frequency setting by register SCN_CTRL bit5 FLL_ON = 1.

7. Seek mode

LV24230 support world wide FM frequency.

The step of frequency is selectable. < 50KHz, 100KHz, 200KHz> 【Table6】

Table 6 : Seek Step

GRID[1:0]		Seek Step	AREA
BIT	HEX		
01	1	50KHz	EUROPE
10	2	100KHz	CHINA RPK JPN
11	3	200KHz	USA

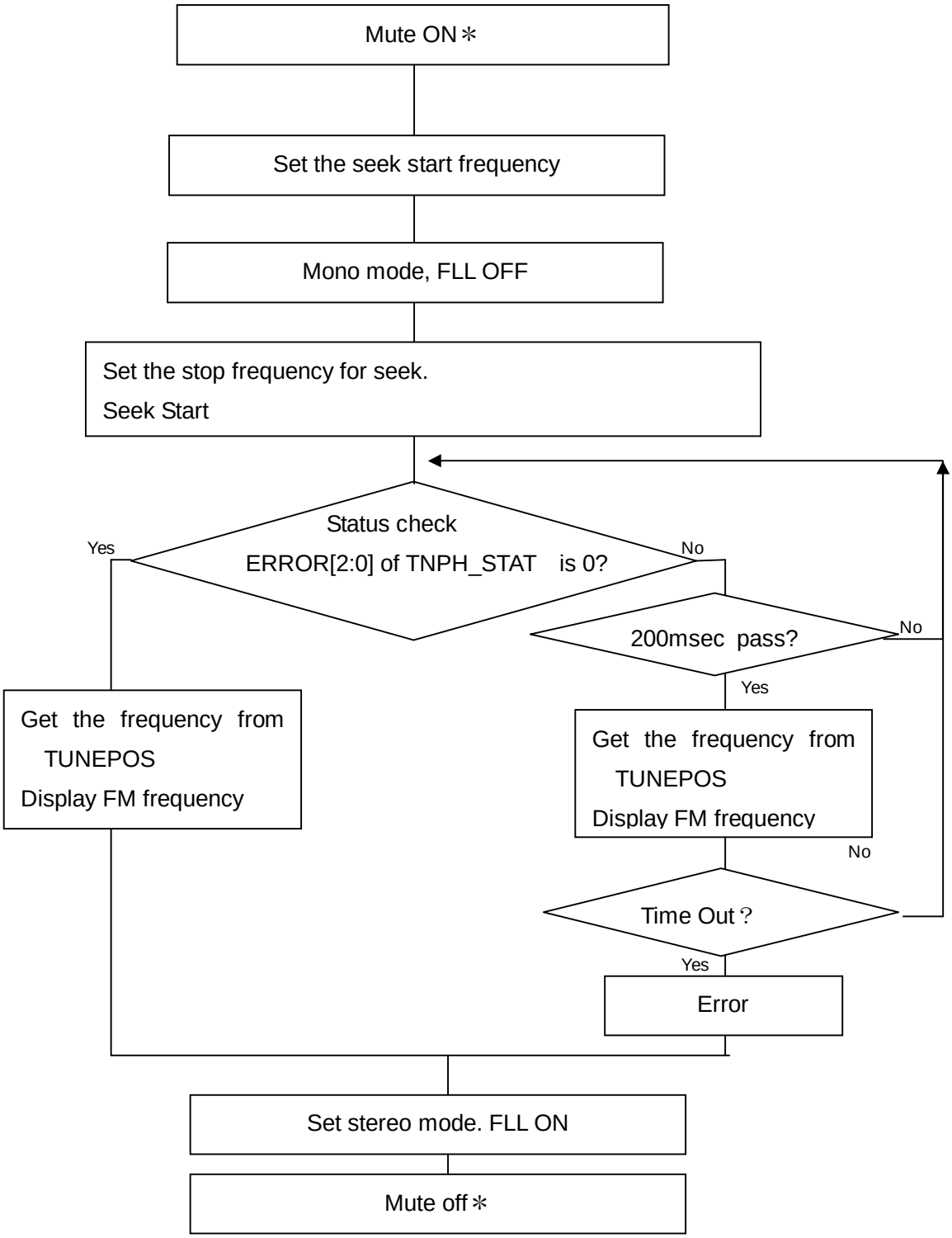
Also you can choose Stop sensitivity by using filed strength level of antenna input【Table7】

Table 7 The antenna input level of seek stop

FS[3:1]		SHF5DB	Antenna input level
BIT	HEX	BIT	
000 …	0 …	0 …	**Stop at almost station** …
011	3	0	Stop only over around 30dBuV
011	3	1	Stop only over around 35dBuV
100	4	0	Stop only over around 40dBuV
100	4	1	Stop only over around 45dBuV
… 111	… 7	… 1	… Stop only over around 75dBuV

＊an antenna input level as reference value.

Following shows the flow of seek mode.



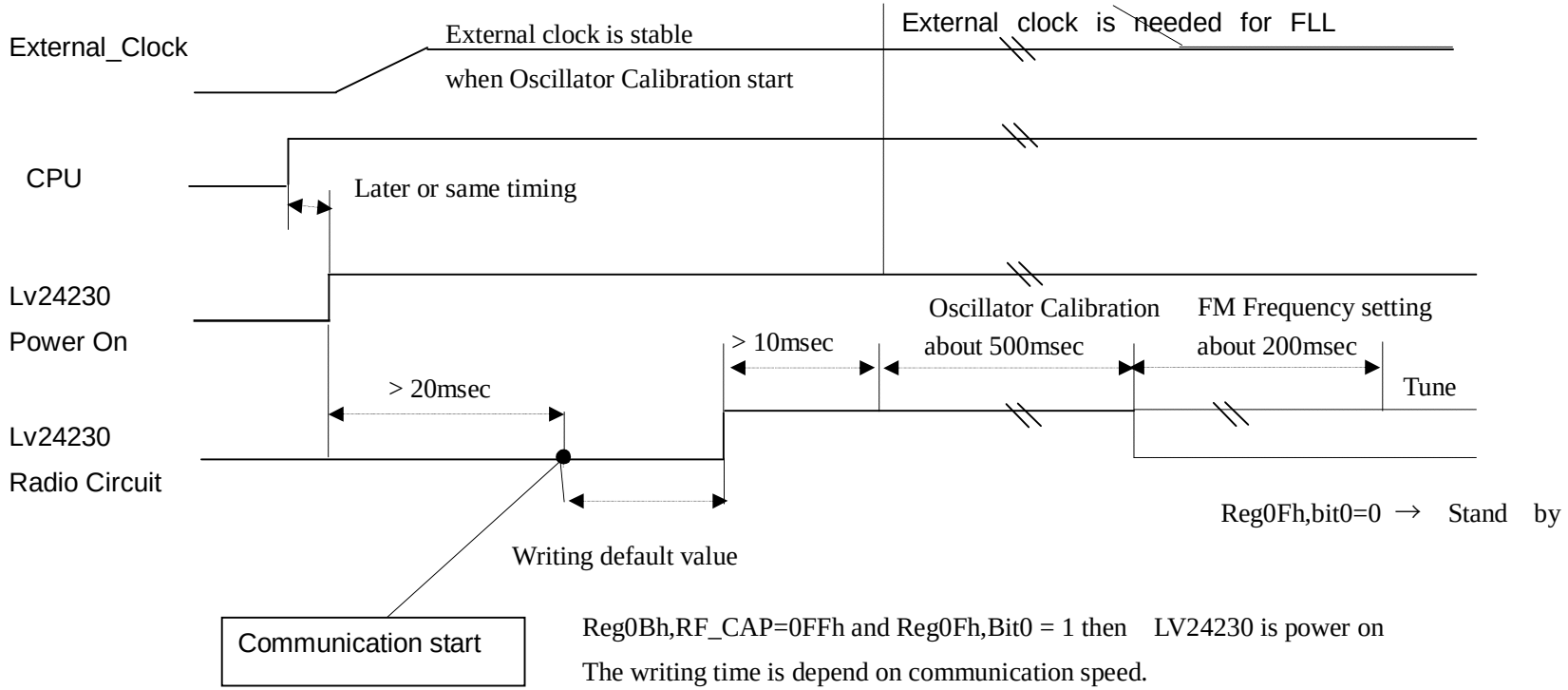
Command Sequence of Seek

**Seek Up command from 76MHz to 108MHz（ No Interrupt use）

No	Address	register name	Bit		Setting Value		Explanation
					BIN	HEX	
1	0Dh	RADIO_CTRL1	Bit2	nMUTE	0		Mute
			Bit3	ST_M	1		Forced Mono mode
2	1Dh	SCN_CTRL	Bit7:6 Bit 5	GRID FLL_ON	10 0		Step = 100KHz FLL OFF
3	1Fh	TARGET_VAL_H	Bit7	TARGET[15]	0		FM Frequency Setting
			Bit6:0			00	Start Frequency Setting
4	1Eh	TARGET_VAL_L	Bit7:0			EE	(7590-6400)/5 = 00EEh
5	11h	TNPH_STAT	Bit7:5	ERROR	!7		Non Busy or wait until Time Out
6	1Fh	TARGET_VAL_H	Bit7	TARGET[15]	1		SEEK UP
			Bit6	TARGET[14]	1		
			Bit6:0			03	End Frequency Setting
7	1Eh	TARGET_VAL_L	Bit7:0			72	(10810-6400)/5 = 0372h
8	11h	TNPH_STAT	Bit7:5	ERROR	!7		Non Busy or wait until Time Out
			Bit1:0	TPOS[9:8]			Get display frequency
9	10h	TNPL	Bit7:0	TPOS[7:0]			Freq = (TPOS*5)+6400
‘9	00h	CHIP_ID	Bit7:0			01	(!!) In case of SEEK stop
10	11h	TNPH_STAT	Bit7:5	ERROR	0		SEEK Normal end
			Bit1:0	TPOS[9:8]			Get seeked frequency
11	10h	TNPL	Bit7:0	TPOS[7:0]			Freq = (TPOS*5)+6400
12	1Dh	SCN_CTRL	Bit5	FLL_ON	1		FLL ON
13	0Dh	RADIO_CTRL1	Bit3	ST_M	0		Forced Mono Mode OFF
			Bit2	nMute	1		Mute off

TIMING CHART

Power On－External clock mode

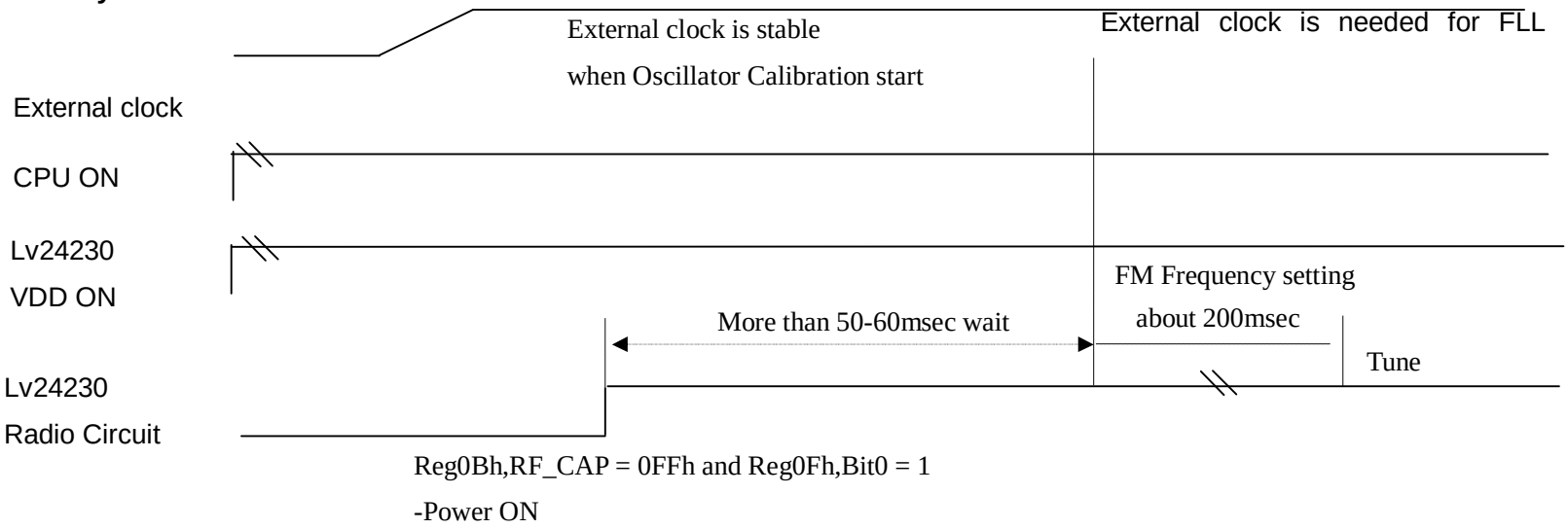


The external clock is stable when Oscillator calibration start.

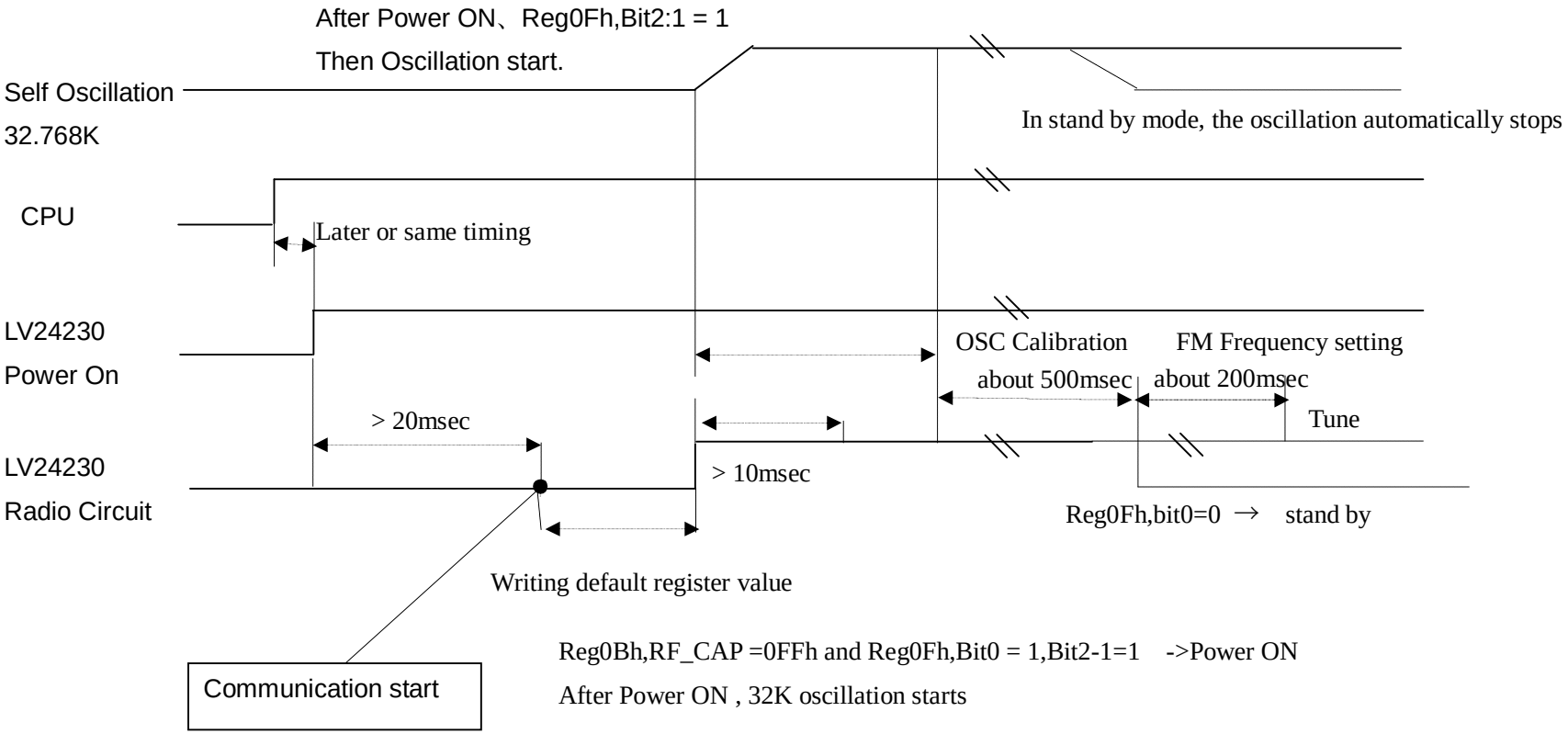
After tuning, the external clock is needed for FLL function.

The oscillator calibration time is shortened , when the value <0FFh> is wrote in RF_CAP register before Power On.

Stand by off－External clock mode



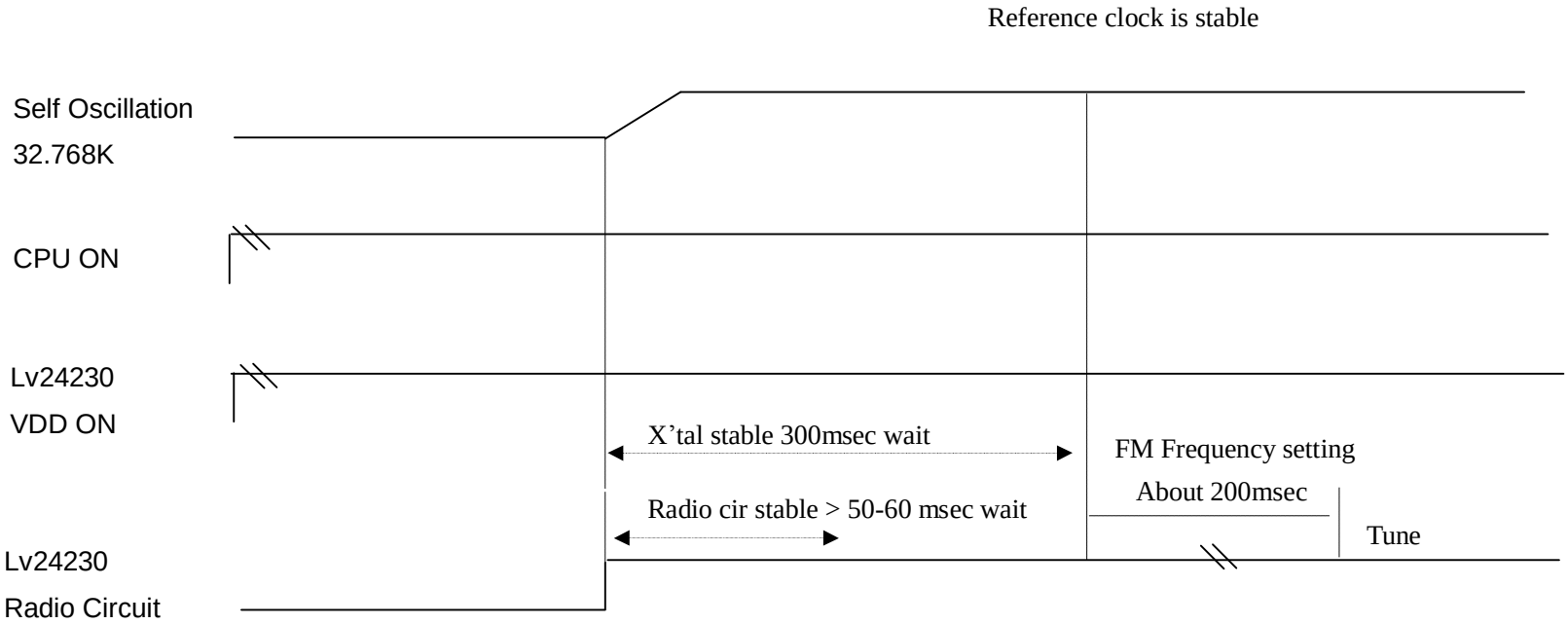
Power On－Self Oscillation Mode



After tuning, the clock is needed for FLL function.

The oscillator calibration time is shortened , when the value <0FFh> is wrote in RF_CAP register before Power On.

Standby off – Self Oscillation Mode



Reg0Bh,RF_CAP = 0FFh and Reg0Fh,Bit0 = 1,Bit2-1=1 ->Power ON

After Power ON, the oscillation starts.

The detail information of register

Register 00h – CHIP_ID – Chip identify register (Read/Write)

7	6	5	4	3	2	1	0
ID[7:0]							

Bit 7-0: **ID[7:0]:** 8-bit chip ID.
LV24230：12h

Note :If you abort the command ,write any value in this register.

Register 02h – RADIO_STAT – Radio station status (Read-Only)

7	6	5	4	3	2	1	0
RAD_IF	N/A	N/A	MO_ST	FS[2:0]			SF5DB

Bit 7: **RAD_IF:** Radio interrupt flag.
0 = no interrupt
1 = interrupt
Note:
When status (field strength, stereo/mono). changed, this bit is set.
If Interrupt of IRQ pin is enable, Interrupt pin is set by following IPOL register condition.
This bit is cleared by register read. In stand-by mode(PW_RAD = 0) , this bit is 1

Bit 6-5: **NA[6:5]:** NA
0

Bit 4: **MO_ST:** Mono/stereo indicator
0 = Mono
1 = Stereo

Bit 3-1: **FS[3:1]:** Field strength:
0: Field strength < 10 dBμV
1: Field strength 10 - 20 dBμV
2: Field strength 20 - 30 dBμV
3: Field strength 30 - 40 dBμV
4: Field strength 40 - 50 dBμV
5: Field strength 50 - 60 dBμV
6: Field strength 60 - 70 dBμV
7: Field strength >70 dBμV

Bit 0: **FS5DB:** Field strength +5dB
0 = normal
1 = +5dB

Register 0Bh – RFCAP – RF Cap bank (Read/Write)

7	6	5	4	3	2	1	0
RFCAP[7:0]							

Bit 7-0: **RFCAP[7:0]:** RF Oscillator CAP bank

Register 0Dh – RADIO_CTRL1 – Radio control 1 (Read/Write)

7	6	5	4	3	2	1	0
IF_SEL	IFBWSEL	AGC_SPD	DEEM	ST_M	nMUTE	VOL[1:0]	

Bit 7: **IF_SEL:** IF Frequency Setting
0 = 130 kHz
1 = 150 kHz

Bit 6: **IFBWSEL:** IF band width setting
0 = 50%
1 = 100%

Bit 5: **AGC_SPD:** AGC Speed setting
0 = Normal
1 = High

Bit 4: **DEEM:** de-emphasis
0 = 50 µs:Korea,China,Europe,Japan
1 = 75 µs:USA

Bit 3: **ST_M:** Stereo/mono setting
0 = Stereo enabled
1 = Stereo disabled (mono mode)

Bit 2: **nMUTE:** Audio Mute
0 = Mute On
1 = Mute Off

Bit 1-0: **VOL[1:0]:** Volume Setting
0: Min
…
3: Max

Register 0Eh – RADIO_CTRL2 – Radio control 2 (Read/Write)

7	6	5	4	3	2	1	0
SOFTST[2:0]			SOFTMU[2:0]			N/A	STABI_BP

Bit 7-5: **SOFTST[2:0]:** Soft Stereo setting
000b = Soft stereo level 3
001b = Disable soft stereo
010b = Soft stereo level 1 (*)
100b = Soft stereo level 2
Note: do not use without these value.
(*): recommending setting

Bit 4-2: **SOFTMU[2:0]:** Soft audio mute setting
000b = Soft audio mute level 3
001b = Disable soft audio mute
010b = Soft audio mute level 1
100b = Soft audio mute level 2 (*)
Note: do not use without these value。
(*):recommending setting

Bit 1: Reserved**:** 0(Fix)

Bit 0: **STABI_BP:** Internal regulator by-pass bit
0 = Internal regulator operate (normal)
1 = Internal regulator by-pass

LV24230 has a soft mute function and a soft stereo function. Both function has 4 level.
When noises increased, a soft mute function decreases the output and the purpose of soft mute is decrease a noise of hearing relatively. At weak signal level of reception, a soft stereo function improve an S / N characteristic by changing it to a monaural mode .

Register 0Fh – RADIO_CTRL3 – Radio control 3 (Read/Write)

7	6	5	4	3	2	1	0
IPOL	SM_IE	RAD_IE	SD_PM	nIF_PM	EXT_CLK_CFG[1:0]		PW_RAD

Bit 7: **IPOL:** Interrupt（IRQ） Polarity
0 = IRQ active high
1 = IRQ active low

Bit 6: **SM_IE:** Command end interrupt
0 = Disable
1 = Enable

Bit 5: **RAD_IE:** Radio Interrupt (field strength/stereo changes)
0 = Disable
1 = Enable

Bit 4: **SD_PM:** Stereo decoder clock PLL mute
0 = SD PLL On (Normal Operation)
1 = SD PLL Off (Adjustment)

Bit 3: **nIF_PM:** IF PLL mute
0 = IF PLL Off (Adjustment)
1 = IF PLL On (Normal Operation)

Bit 2-1: **EXT_CLK_CFG[1:0]:** External Clock Setting

EXT_CLK_CFG[1:0]	**Reference clock**
00	Off
01	32768 Hz crystal oscillator
10	Oscillator clock source / 32 (for high frequency source)
11	Oscillator clock source (for low frequency source)

Bit 0: **PW_RAD:** Radio Circuit Power
0 = Power Off（ Stand-by）.
1 = Power On
Note: At the time of start, PW_RAD becomes 0(Stand-by)

Register 10h – TNPL – Tune position low (Read-Only)

7	6	5	4	3	2	1	0
TUNEPOS[7:0]							
Bit 7-0:	**TUNEPOS[7:0]:** Current RF Frequency（Low 8bit）						

Register 11h – TNPH_STAT – Tune position high/status (Read-Only)

7	6	5	4	3	2	1	0
ERROR[2:0]			SM_IF	TUNED	NA	TUNEPOS[9:8]	

Bit 7-5: **ERROR[2:0]:** Error Code

ERROR [2:0]	Remark
0	OK, Command end（No Error）
1	Default value after or during reset
2	Band Limit Error
3	DAC Limit Error
6	Command forced End
7	Command busy

Bit 4: **SM_IF:** Command End interrupt flag
Once read this register , flag is cleared
0 = No Interrupt
1 = Interrupt

Bit 3: **TUNED:** Radio tuning Flag
0 = No tune
1 = Tuned
Note: This flag is set when Tuned or a station search succeeded.
This flag is cleared under 3 conditions as below.
1. PW_RAD=0
2. Tuning Frequency
3. FM station searching

Bit 1:0: **TUNEPOS[9:8]:** Current RF frequency（High 2 bit）

Register 19h – REF_CLK_PRS – Reference clock pre-scaler (Read/Write)

7	6	5	4	3	2	1	0
REFPRE[2:0]			REFMOD[4:0]				

Bit [7:5]: **REFPRE[2:0]:**Reference Clock pre - scaler
0 = 1:1
1 = 1:2
…
7 = 1:128

Bit [4:0]: **REFMOD[4:0]:** 5-bit slope correction

Register 1Ah – REF_CLK_DIV – Reference clock divider (Read/Write)

7	6	5	4	3	2	1	0
REFDIV[7:0]							

Bit 7-0: **REFDIV[7:0]:** Reference Clock Divider
0: Divider Value ＝1
1: Divider Value＝ 2
…
255: Divider Value＝256

Register 1Bh –REF_CLK_OFF – Reference clock offset (Read/Write)

7	6	5	4	3	2	1	0
REFOFFS[7:0]							

Bit 7-0: **REFOFFS[7:0]:** Offset register for the spread of reference clock

Register 1Dh – SCN_CTRL – Scan control (Read/Write)

7	6	5	4	3	2	1	0
GRID[1:0]		FLL_ON	FLL_MODE	FS[2:0]			SHF5DB

Bit 7-6: **GRID[1:0]:** FM station search frequency interval
0 = the frequency measurement and adjustment
1 = 50 kHz grid
2 = 100 kHz grid
3 = 200 kHz grid

Bit 5: **FLL_ON:** FLL Control
0 = FLL OFF(During FM frequency setting or during seek mode)
1 = FLL ON(After FM frequency setting or after seek mode)

Bit 4: Reserved 0:FIX

Bit 3-1: **FS[3:1]:** Field strength setting at the time of FM station search and a frequency adjustment bit

Bit 0: **SHF5DB:** Field Strength +5dB
0 = Normal
1 = +5dB

Register1Eh – TARGET_VAL_L – Target Value Low Register (Read/Write)

7	6	5	4	3	2	1	0
TARGET[7:0]							
Bit 7-0: **TARGET[7:0]:** Target frequency low 8 bit: Tuning frequency or Limit Frequency for FM Station Search							

Register 1Fh – TARGET_VAL_H – Target Value High Register (Read/Write)

7	6	5	4	3	2	1	0
TARGET[15:8]							
Bit 7-0: **TARGET[15:8]:** Target frequency High 8 bit: Target value of oscillator calibration, Tuning frequency value or limit frequency value for station search **Note:** GRID[1:0] is not 0 TARGET[15:14] has different definition During power on, after set target low and high value, command start.							

□ Diagram 2-2 Reference Clock Parameter

No	Reference Clock			Value
1	32.768 KHz	Oscillator calibration.	PRESCALER	0x04
			DIVIDER	0x82
			Target Value	0x1306
		FM setting (& Seek mode)	PRESCALER	0x02
			DIVIDER	0x14
			MOD	0x03
			OFFSET	0xCD

*The relation ship GRID value and TARGET value

<table>
<tr><th>Command</th><th>Reg1D
GRID
[1:0]</th><th>Reg1D
FS
[3:1]</th><th>Reg1F
TARGET
[15]</th><th>Reg1F
TARGET
[14]</th><th>Reg1F
TARGET
[13:0]</th></tr>
<tr><td>OSC calibration
SD・IF</td><td>00</td><td>001</td><td>Don’t care</td><td>Don’t care</td><td>Ref. Diagram 2-2</td></tr>
<tr><td>FM frequency setting</td><td rowspan="3">SEEK STEP と AREA
<table><tr><th>GRID</th><th>Step KHz</th><th>AREA</th></tr><tr><td>01</td><td>50</td><td>EUROPE</td></tr><tr><td>10</td><td>100</td><td>JPN etc</td></tr><tr><td>11</td><td>200</td><td>USA</td></tr></table></td><td rowspan="3">Seek stop level and Antenna level
<table><tr><th rowspan="2">Seek Stop Level</th><th rowspan="2">FS</th><th colspan="2">Reg1D Bit0 SF5DB [dBuV]</th></tr><tr><th>0</th><th>1</th></tr><tr><td>0</td><td>0</td><td><10</td><td></td></tr><tr><td>1</td><td>0</td><td></td><td><15</td></tr><tr><td>2</td><td>1</td><td>10-20</td><td></td></tr><tr><td>3</td><td>1</td><td></td><td>15-25</td></tr><tr><td>4</td><td>2</td><td>20-30</td><td></td></tr><tr><td>5</td><td>2</td><td></td><td>25-35</td></tr><tr><td>6</td><td>3</td><td>30-40</td><td></td></tr><tr><td>7</td><td>3</td><td></td><td>35-45</td></tr><tr><td>8</td><td>4</td><td>40-50</td><td></td></tr><tr><td>9</td><td>4</td><td></td><td>45-55</td></tr><tr><td>10</td><td>5</td><td>50-60</td><td></td></tr><tr><td>11</td><td>5</td><td></td><td>55-65</td></tr><tr><td>12</td><td>6</td><td>60-70</td><td></td></tr><tr><td>13</td><td>6</td><td></td><td>65-75</td></tr><tr><td>14</td><td>7</td><td>>70</td><td></td></tr><tr><td>15</td><td>7</td><td></td><td>>75</td></tr></table></td><td>0</td><td>Don’t care</td><td>(FM Frequency −6400)/5</td></tr>
<tr><td>DOWN SEEK</td><td>1</td><td>0</td><td>(Lower limit frequency −6400)/5</td></tr>
<tr><td>UP SEEK</td><td></td><td>1</td><td>(Upper limit frequency −6400)/5</td></tr>
</table>

Supplement

1. Interrupt 【IRQ】

The interrupt of LV24230 notice the change of status to host CPU by changing the output level. The interrupt polarity is fixed by IPOL register(Register 0Fh bit 7) [2].

In case of IRQ active high, after interrupt enable the interrupt pin change from low to high when interrupt occurs. In case of IRQ active low, after interrupt enable the interrupt pin change from high to low when interrupt occurs.

After setting to interrupt enable by Radio control 3 register, the interrupt pin change when the internal status changed following 3 situations.

After interrupt occurs, LV24230 keeps the interrupt status until register read.

After register read, LV24230 clear interrupt status.

Host CPU can know following 3 status change by interrupt.

① Command End

② Change stereo/mono during FM receiving

③ Change of Field strength level during FM receiving

Following is the register table for each interrupt.

	① IRQ for Command End	②③ IRQ for Radio status change of tuning
IRQ Enable bit	RADIO_CTRL3 (Reg 0Fh) SM_IE(Bit 6)	RADIO_CTRL3 (Reg 0Fh) RADIO_IE(Bit 5)
Read Bit	TNPH_STAT（Reg 11h） SM_IF (Bit 4)	RADIO_STAT (Reg 11h) RADIO_IF (Bit 7)
IRQ clear	TNPH_STAT register Read	RADIO_STAT register Read

＊Recommend: Before setting command end interrupt to enable ,please set radio interrupt to disable.

[2] Reg0Fh,Bit7 IPOL